Rockchip
PX3 SE
Technical Reference Manual
Part1

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Chapter 1 System Overview

1.1 Address Mapping

PX3 SE support to boot from internal Boot ROM and support remap function by software programming.

Addr	IP
	Reserved
1013e000	Reserved
1013d000	Reserved 4K
1013c000	Reserved 8k
10138000	GIC 16K
10130000	Reserved 32K
10128000	CPU BUS 32K
10118000	Reserved 64K
10114000	EBC 16k
10112000	Reserved 8K
10110000	MIPI_ctrl 8K
1010e000	VOP 8K
1010c000	RGA 8K
1010a000	CIF 8K
10108000	IEP 8K
10104000	VCODEC 16K
10100000	ROM 16K
100fc000	crypto 16K
100b0000	Reserved 304K
100a0000	PMU 64K
10090000	GPU 64K
10082000	Reserved 56K

Addr	IP
20038000	MIPI-ANA 16K
20034000	HDMI-ANA 16K
20030000	ACODEC-ANA 16K
20020000	Reserved 64K
20010000	Reserved 64K
2000a000	DDR_PHY 24K
20008000	GRF 8K
20004000	DDR_PCTL 16K
20000000	CRU 16K
	before remap
10080000	IMEM 8k

Addr	IP
10504000	Reserved
10500000	NANDC 16K
10400000	GPS 1024K
10300000	PERI BUS 1024k
1023C000	Reserved 784K
10234000	Reserved 32K
10224000	Reserved 64K
10220000	I2S_2ch 16K
1021C000	eMMC 16K
10218000	SDIO 16K
10214000	SDMMC 16K
1020c000	SFC 32k
10208000	TSP 16k
10204000	SPDIF 16k
10200000	I2S_8ch 16k
101E0000	USB HOST OHCI 128K
101C0000	USB HOST ECHI 128K
10180000	USB OTG 256K
	after remap
10080000/ 00000000	IMEM 8k

Addr	IP
20094000	Reserved
20090000	eFuse 16K
2008C000	GMAC 16K
20088000	GPIO3 16K
20084000	GPIO2 16K
20080000	GPIO1 16K
2007C000	GPIO 16K
20078000	DMAC 16K
20074000	SPI 16K
20072000	I2C0 8K
2006C000	SARADC 24K
20068000	UART2 16K
20064000	UART1 16K
20060000	UART0 16K
2005e000	I2C3 8K
2005a000	I2C2 16K
20056000	I2C1 16K
20050000	PWM0 24K
2004C000	WDT 16K
20048000	SCR 16K
20044000	TIMER0-5 16K
60000000	DDR 2G

Fig. 1-1 Address Mapping

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1.2 System Boot

This chip provides system boot from off-chip devices such as SDMMC card, 8bits async nand flash or toggle nand flash, SPI and eMMC memory. When boot code is not ready in these devices, also provide system code download into them by USB OTG interface. All of the boot code will be stored in internal Boot ROM. The following is the whole boot procedure for boot code, which will be stored in Boot ROM in advance.
The following features are supports.

- Support secure boot mode and non-secure boot mode
- Support system boot from the following device:
  - 8bits Async Nand Flash
  - 8bits Toggle Nand Flash
  - SPI interface
  - eMMC interface
  - SDMMC Card
- Support system code download by USB OTG

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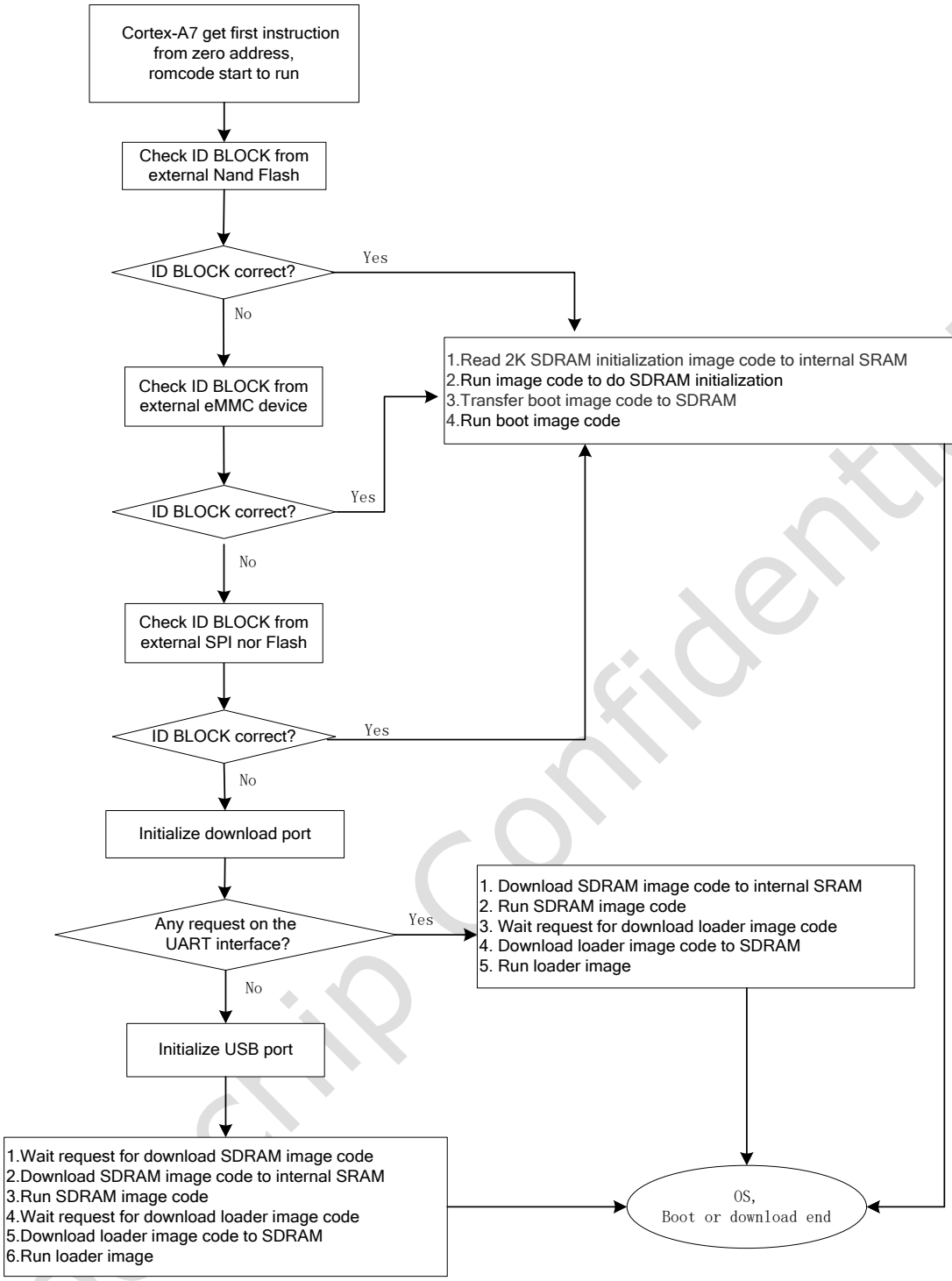


Fig. 1-2 boot procedure flow

1.3 System Interrupt connection

This chip provides an general interrupt controller(GIC) for Cortex-A7 MPCore processor, which has 112 SPI(shared peripheral interrupts) interrupt sources and 3 PPI(Private peripheral interrupt) interrupt source and separately generates one nIRQ and one nFIQ to CPU. The triggered type for each interrupts is high level sensitive, not programmable. The detailed interrupt sources connection is in the following table.

Table 1-1 PX3 SE Interrupt connection list

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	IRQ ID	Source	Polarity
Source(spi)	32	DMAC2(0)	High level
	33	DMAC2(1)	High level
	34	DDR_PCTL	High level
	35	gpu_irqgp	High level
	36	gpu_irqmmu	High level
	37	gpu_irqpp	High level
	38	Video encoder	High level
	39	Video decoder	High level
	40	CIF	High level
	41	VOP	High level
	42	USB OTG	High level
	43	USB Host EHCI	High level
	44	gps_irq	High level
	45	gps_timer_irq	High level
	46	SD/MMC0	High level
	47	SDIO	High level
	48	eMMC	High level
	49	SAR-ADC	High level
	50	NandC	High level
	51	I2S_2ch	High level
	52	UART0	High level
	53	UART1	High level
	54	UART2	High level
	55	SPI0	High level
	56	I2C0	High level
	57	I2C1	High level
	58	I2C2	High level
	59	I2C3	High level
	60	Timer0	High level
	61	Timer1	High level
	62	PWM	High level
	63	PMU	High level
	64	USB Host OHCI	High level
	65	MIPI_controller	High level
	66	WDT	High level
	67	otg_bvalid_irq	High level
	68	GPIO0	High level
	69	GPIO1	High level
	70	GPIO2	High level
	71	GPIO3	High level
	72	CRYPTO	High level

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IRQ ID	Source	Polarity
73	reserved	High level
74	peri_ahb_usb arbiter	High level
75	reserved	High level
76	RGA	High level
77	hdmi	High level
78	SD/MMC detect	High level
79	SDIO detect	High level
80	IEP	High level
81	EBC	High level
82	sfc	High level
83	otg0_id_irq	High level
84	otg0_linestate_irq	High level
85	otg1_linestate_irq	High level
86	sd_detectn_irq	High level
87	spdif	High level
88	gmac	High level
89	gmac_tmc	High level
90	tsp	High level
91	timer2	High level
92	timer3	High level
93	timer4	High level
94	timer5	High level
95	sim_card	High level
96	acodec_detectn_irq	High level
97	hevc_mmu_irq	High level
98	hevc_dec_irq	High level
99	vpu_mmu_irq	High level
100	i2s_8ch	High level
101	Reserved	High level
102	Reserved	High level
103	Reserved	High level
104	Reserved	High level
105	Reserved	High level
106	Reserved	High level
107	Reserved	High level
108	pmuirq_a7_0	High level
109	pmuirq_a7_1	High level
110	pmuirq_a7_2	High level
111	pmuirq_a7_3	High level
112	axierrirq	High level

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1.4 System DMA hardware request connection

This chip provides one DMA controller: DMAC inside peripheral system. 16 hardware request ports are used in DMAC, and the trigger type for each of them is high level, not programmable.

Table 1-2 DMAC Hardware request connection list

Req Number	Source	Polarity
0	I2S_2ch tx	High level
1	I2S_2ch rx	High level
2	Uart0 tx	High level
3	Uart0 rx	High level
4	Uart1 tx	High level
5	Uart1 rx	High level
6	Uart2 tx	High level
7	Uart2 rx	High level
8	SPI tx	High level
9	SPI rx	High level
10	SD/MMC	High level
11	SDIO	High level
12	eMMC	High level
13	SPDIF	High level
14	I2S_8ch tx	High level
15	I2S_8ch rx	High level

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Chapter 2 Clock And Reset Unit (CRU)

2.1 Overview

The CRU is an APB slave module that is designed for generating all of the internal and system clocks, resets of chip. CRU generates system clock from PLL output clock or external clock source, and generates system reset from external power-on-reset, watchdog timer reset or software reset.

CRU supports the following features:

- Compliance to the AMBA APB interface
- Embedded four PLLs
- Support only one crystal
- Flexible selection of clock source
- Supports the respective gating of all clocks
- Supports the respective software reset of all modules

2.2 Block Diagram

The CRU comprises with:

- Four PLLs
- Register configuration unit
- Clock generate unit
- Reset generate unit

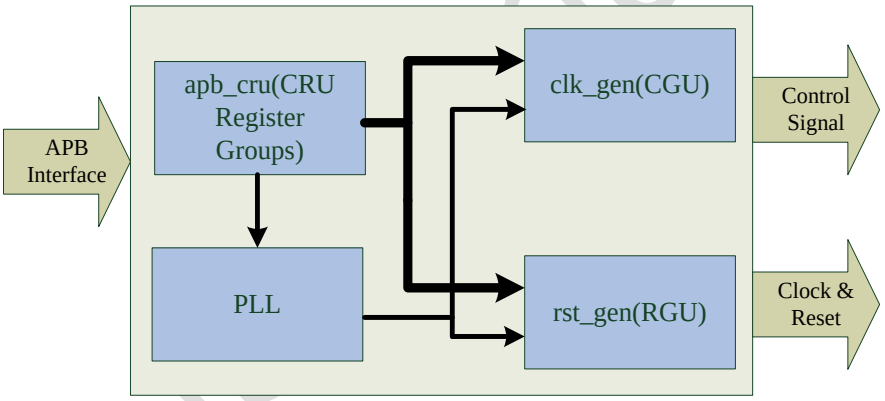


Fig. 2-1 CRU Architecture

2.3 System Clock Solution

The following diagrams show clock architecture (mux and divider information).

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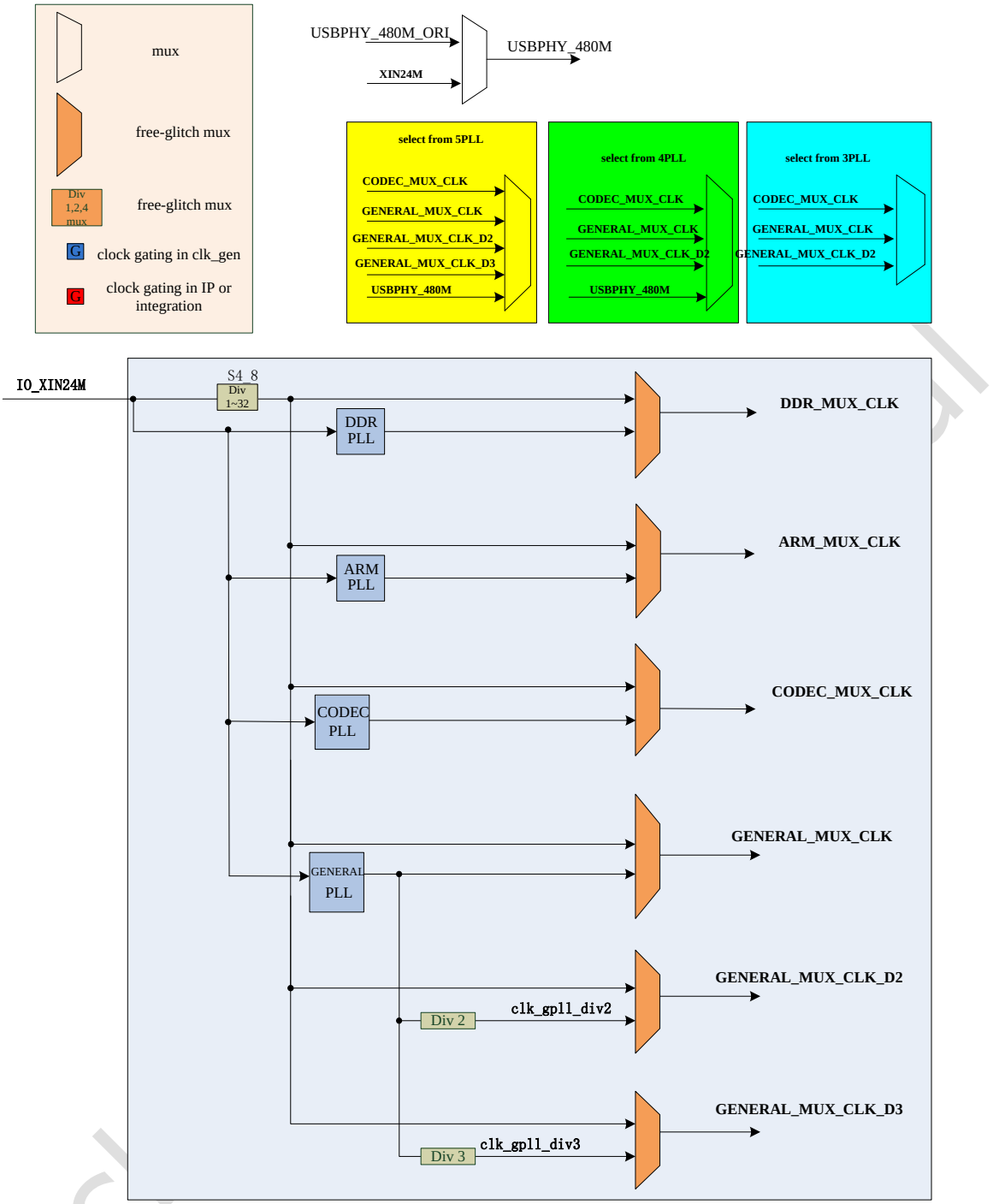


Fig. 2-2 Chip Clock Architecture Diagram 1

Rock

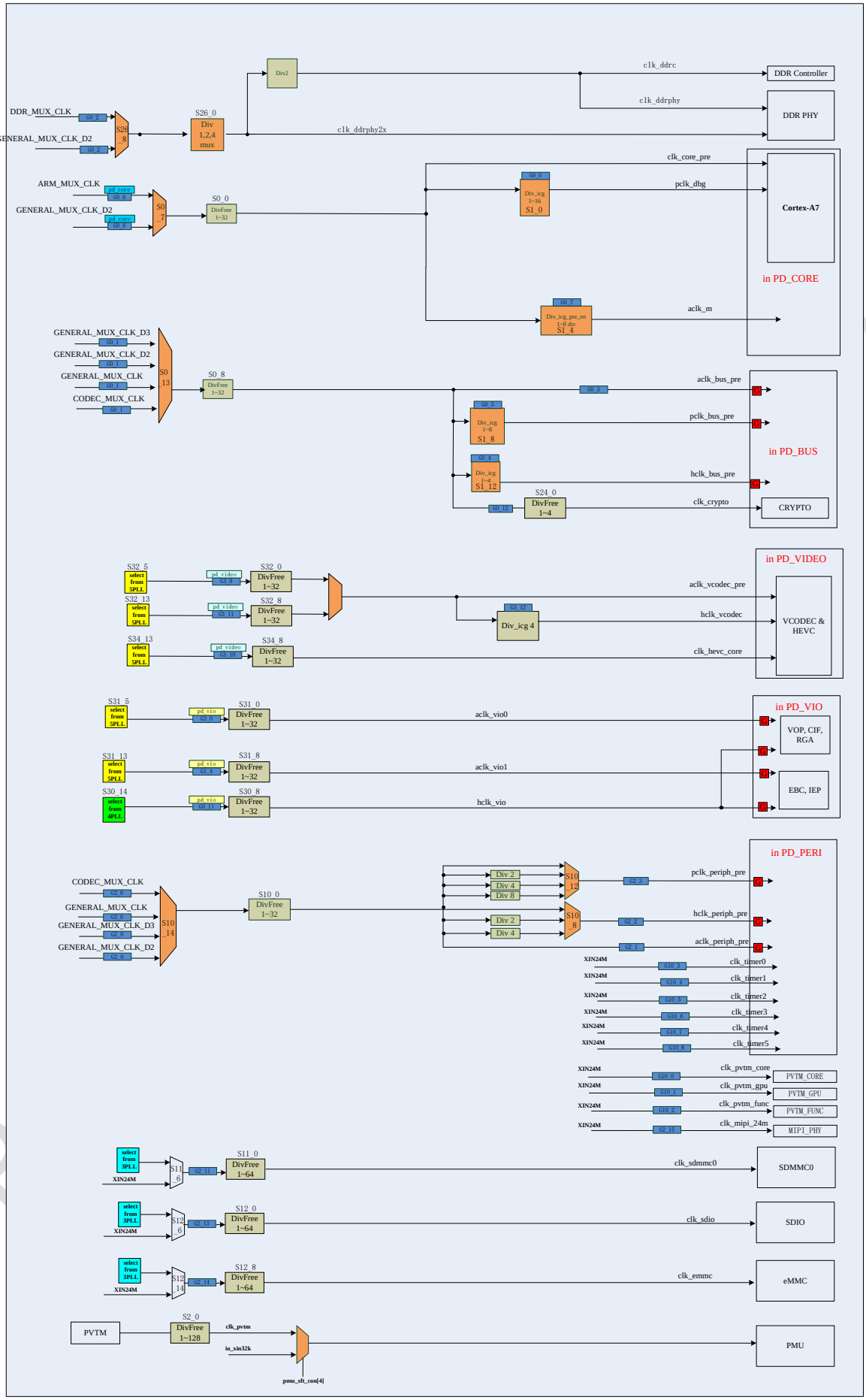


Fig. 2-3 Chip Clock Architecture Diagram 2

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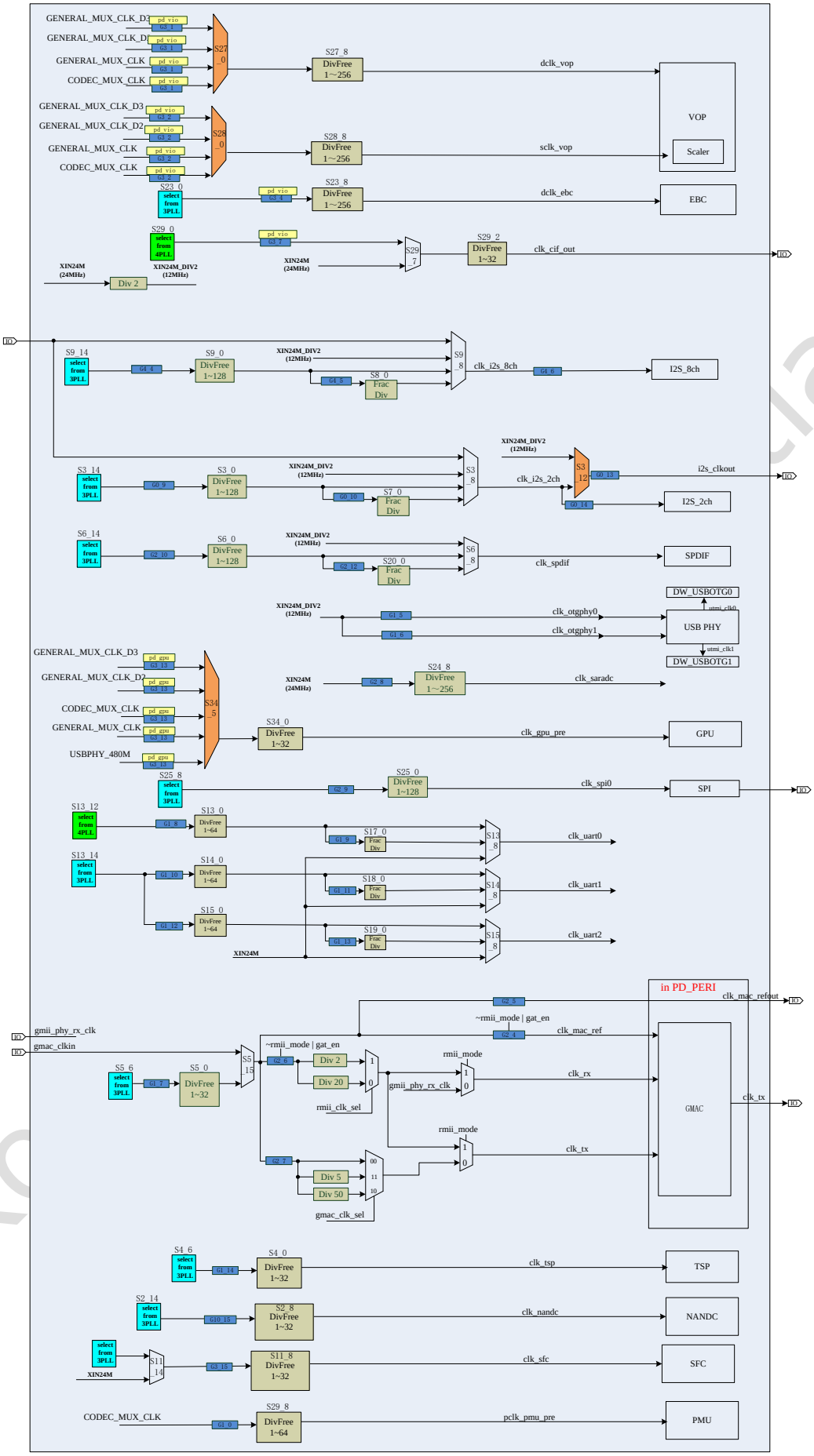


Fig. 2-4 Chip Clock Architecture Diagram 3

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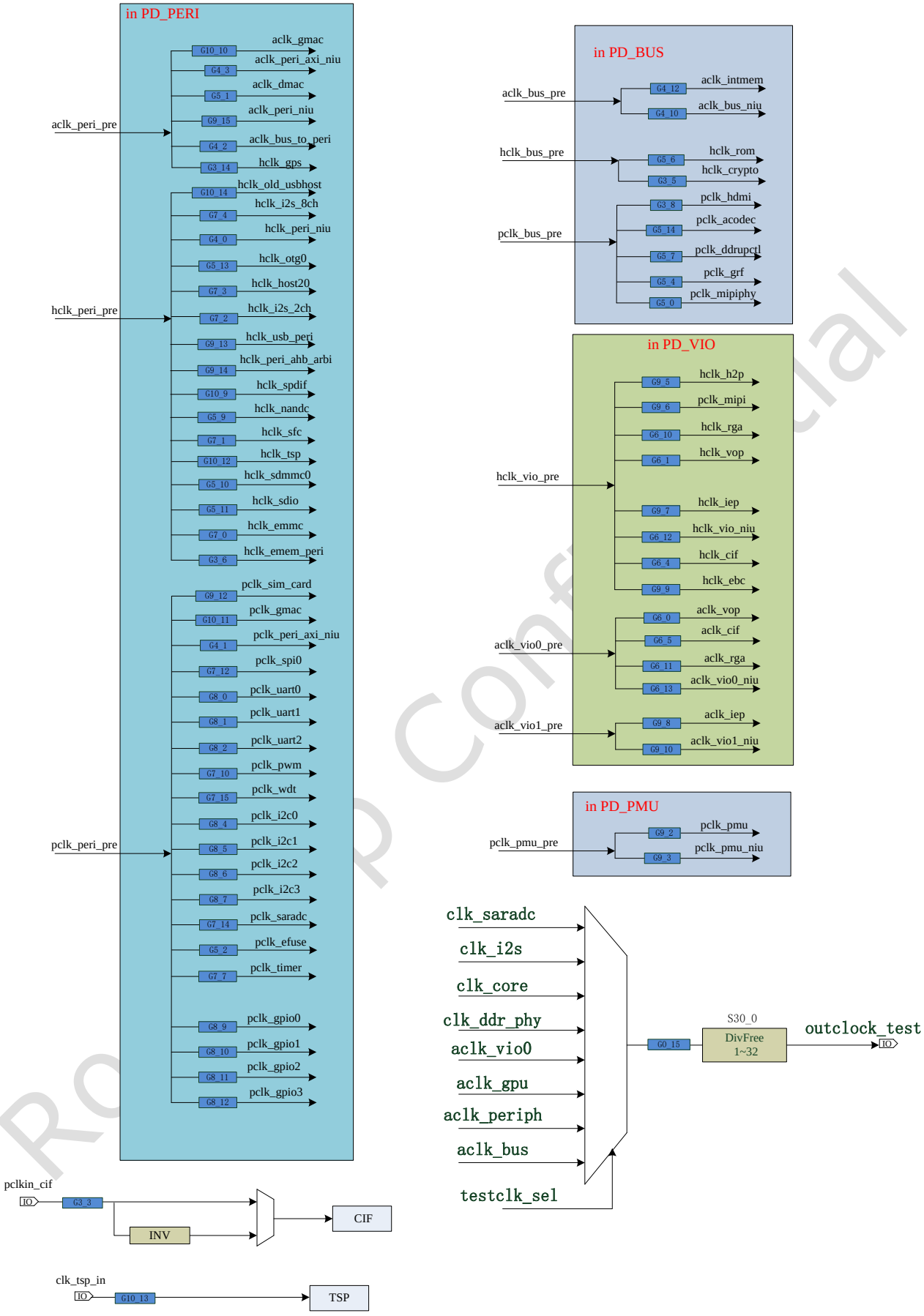


Fig. 2-5 Chip Clock Architecture Diagram 4

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Description about input clock
The source of input clock in upper diagrams is listed as following Table.

Table 2-1 Input clock description in clock architecture diagram

Input Clock	Source	IO Name
xin24m	External crystal oscillator (24MHz)	XIN24M

2.4 System Reset Solution

The following diagrams show reset architecture in this device.

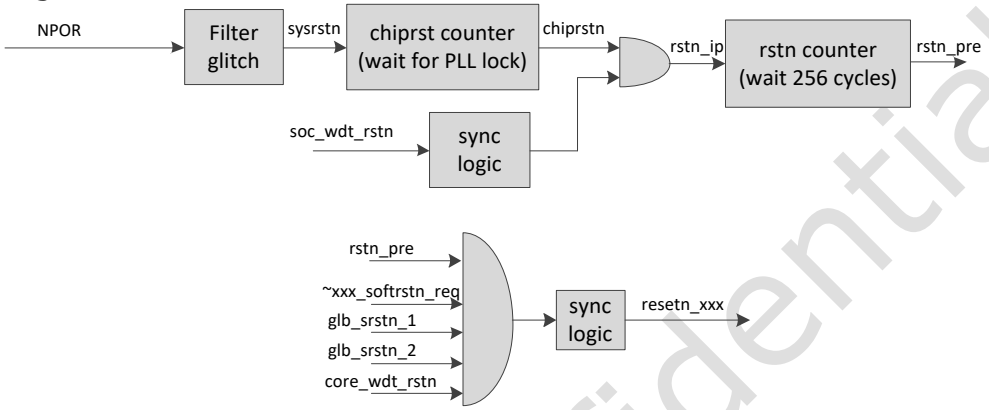


Fig. 2-6 Reset Architecture Diagram

Reset source of each reset signal includes hardware reset(NPOR), soc watch dog reset(soc_wdt_rstn), software reset request(xxx_softrstn_req), global software reset1(glb_srstn_1), global software reset2(glb_srstn_2) and A7 core watch dog reset(core_wdt_rstn).
The 'xxx' of resetn_xxx and xxx_softrstn_req is the module name.
Soc_wdt_rstn is the reset from watch-dog IP in the SoC, but core_wdt_rstn is the reset from A7 core watch-dog block.
Glb_srstn_1 and glb_srstn_2 are the global software reset by programming CRU register. When writing register CRU_GLB_SRST_FST_VALUE as 0xfdb9, glb_srstn_1 will be asserted, and when writing register CRU_GLB_SRST_SND_VALUE as 0xeca8, glb_srstn_2 will be asserted. The two software reset will be self-clear by hardware. Glb_srstn_1 will reset the all logic, and Glb_srstn_2 will reset the all logic except GRF and all GPIOs.

2.5 Function Description

There are four PLLs in the chip: ARM PLL, DDR PLL, CODEC PLL and GENERAL PLL, and it supports only one crystal oscillator: 24MHz. Each PLL can only receive 24MHz oscillator. Four PLLs all can be set to slow mode or deep slow mode, directly output selectable 24MHz or 32.768kHz. When power on or changing PLL setting, we must force PLL into slow mode to ensure output stable clock.
To maximize the flexibility, some of clocks can select divider source from multi-PLLs.
To provide some specific frequency, another solution is integrated: fractional divider. In order to be sure the performance for divided clock, there is some usage limit, we can only get low frequency and divider factor must be larger than 20.
All clocks can be software gated and all reset can be software generated.

2.6 PLL Introduction

2.6.1 Overview

The chip uses 2.4GHz PLL for all four PLLs. The 2.4GHz PLL is a general purpose, high-performance PLL-based clock generator. The PLL is a multi-function, general purpose frequency synthesizer. Ultra-wide input and output ranges along with best-in-class jitter performance allow the PLL to be used for almost any clocking application. With excellent supply noise immunity, the PLL is ideal for use in noisy mixed signal SoC environments.
2.4GHz PLL supports the following features:

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- Input Frequency Range: 1MHz to 800MHz(Integer Mode) and 10MHz to 800MHz (Fractional Mode)
- Output Frequency Range: 12MHz to 2.4GHz
- 24 bit fractional accuracy, and fractional mode jitter performance to nearly match integer mode performance.
- 4:1 VCO frequency range allows PLL to be optimized for minimum jitter or minimum power.
- Isolated analog supply (2.5V) allows for excellent supply rejection in noisy SoC applications.
- Lock Detect Signal indicates when frequency lock has been achieved.

2.6.2 Block diagram

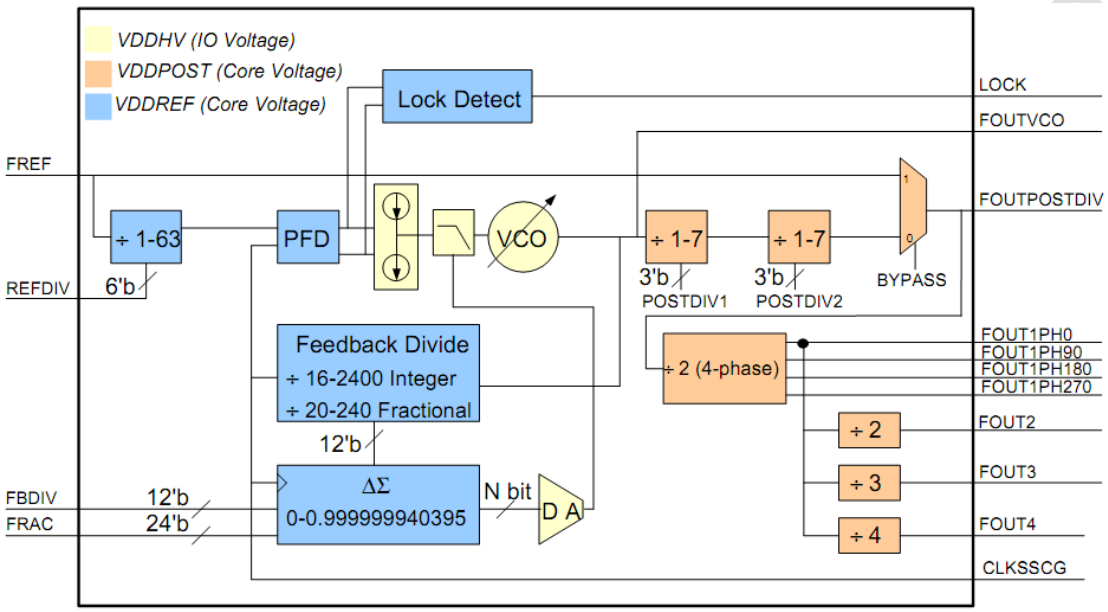


Fig. 2-7 PLL Block Diagram

How to calculate the PLL

The Fractional PLL output frequency can be calculated using some simple formulas. These formulas also embedded within the Fractional PLL Verilog model:

If DSMPD = 1 (DSM is disabled, "integer mode")

FOUTVCO = FREF / REFDIV * FBDIV

FOUTPOSTDIV = FOUTVCO / POSTDIV1 / POSTDIV2

If DSMPD = 0 (DSM is enabled, "fractional mode")

FOUTVCO = FREF / REFDIV * (FBDIV + FRAC / 224)

FOUTPOSTDIV = FOUTVCO / POSTDIV1 / POSTDIV2

Where:

FOUTVCO = Fractional PLL non-divided output frequency

FOUTPOSTDIV = Fractional PLL divided output frequency (output of second post divider)

FREF = Fractional PLL input reference frequency

REFDIV = Fractional PLL input reference clock divider

FVCO = Frequency of internal VCO

FBDIV = Integer value programmed into feedback divide

FRAC = Fractional value programmed into DSM

Changing the PLL Programming

In most cases the PLL programming can be changed on-the-fly and the PLL will simply slew to the new frequency. However, certain changes have the potential to cause glitches on the PLL output clocks. These changes include:

- Switching into or out of BYPASS mode may cause a glitch on FOUTPOSTDIV
- Changing POSTDIV1 or POSTDIV2 may cause a short pulse with width equal to as little

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as one VCO period on FOUTPOSTDIV
- Changing POSTDIV could cause a shortened pulse on FOUT1PH* or FOUT2/3/4
- Asserting PD or FOUTPOSTDIVPD may cause a glitch on FOUTPOSTDIV

2.7 Register Description

This section describes the control/status registers of the design.

2.7.1 Registers Summary

Name	Offset	Size	Reset Value	Description
CRU_APLL_CON0	0x0000	W	0x000010af	ARM PLL control register0
CRU_APLL_CON1	0x0004	W	0x00001046	ARM PLL control register1
CRU_APLL_CON2	0x0008	W	0x00000001	ARM PLL control register2
CRU_DPLL_CON0	0x0010	W	0x00001064	DDR PLL control register0
CRU_DPLL_CON1	0x0014	W	0x00001043	DDR PLL control register1
CRU_DPLL_CON2	0x0018	W	0x00000001	DDR PLL control register2
CRU_CPLL_CON0	0x0020	W	0x0000107d	Codec PLL control register0
CRU_CPLL_CON1	0x0024	W	0x00001046	Codec PLL control register1
CRU_CPLL_CON2	0x0028	W	0x00000001	Codec PLL control register2
CRU_GPLL_CON0	0x0030	W	0x00004063	General PLL control register0
CRU_GPLL_CON1	0x0034	W	0x00001042	General PLL control register1
CRU_GPLL_CON2	0x0038	W	0x00000001	General PLL control register2
CRU_MODE_CON	0x0040	W	0x00000000	System work mode control register
CRU_CLKSEL0_CON	0x0044	W	0x00000100	Internal clock select and divide register0
CRU_CLKSEL1_CON	0x0048	W	0x00003113	Internal clock select and divide register1
CRU_CLKSEL2_CON	0x004c	W	0x00000707	Internal clock select and divide register2
CRU_CLKSEL3_CON	0x0050	W	0x0000001f	Internal clock select and divide register3
CRU_CLKSEL4_CON	0x0054	W	0x00000003	Internal clock select and divide register4
CRU_CLKSEL5_CON	0x0058	W	0x00000003	Internal clock select and divide register5
CRU_CLKSEL6_CON	0x005c	W	0x0000021f	Internal clock select and divide register6
CRU_CLKSEL7_CON	0x0060	W	0x0bb8ea60	Internal clock select and divide register7
CRU_CLKSEL8_CON	0x0064	W	0x0bb8ea60	Internal clock select and divide register8
CRU_CLKSEL9_CON	0x0068	W	0x0000001f	Internal clock select and divide register9
CRU_CLKSEL10_CON	0x006c	W	0x0000a100	Internal clock select and divide register10

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Name	Offset	Size	Reset Value	Description
CRU_CLKSEL11_CON	0x0070	W	0x00000017	Internal clock select and divide register11
CRU_CLKSEL12_CON	0x0074	W	0x00001717	Internal clock select and divide register12
CRU_CLKSEL13_CON	0x0078	W	0x0000121f	Internal clock select and divide register13
CRU_CLKSEL14_CON	0x007c	W	0x0000021f	Internal clock select and divide register14
CRU_CLKSEL15_CON	0x0080	W	0x0000021f	Internal clock select and divide register15
CRU_CLKSEL17_CON	0x0088	W	0x0bb8ea60	Internal clock select and divide register17
CRU_CLKSEL18_CON	0x008c	W	0x0bb8ea60	Internal clock select and divide register18
CRU_CLKSEL19_CON	0x0090	W	0x0bb8ea60	Internal clock select and divide register19
CRU_CLKSEL20_CON	0x0094	W	0x0bb8ea60	Internal clock select and divide register20
CRU_CLKSEL23_CON	0x00a0	W	0x00000100	Internal clock select and divide register23
CRU_CLKSEL24_CON	0x00a4	W	0x00001701	Internal clock select and divide register24
CRU_CLKSEL25_CON	0x00a8	W	0x0000011f	Internal clock select and divide register25
CRU_CLKSEL26_CON	0x00ac	W	0x00000000	Internal clock select and divide register26
CRU_CLKSEL27_CON	0x00b0	W	0x00000301	Internal clock select and divide register27
CRU_CLKSEL28_CON	0x00b4	W	0x00000301	Internal clock select and divide register28
CRU_CLKSEL29_CON	0x00b8	W	0x00000524	Internal clock select and divide register29
CRU_CLKSEL30_CON	0x00bc	W	0x00000300	Internal clock select and divide register30
CRU_CLKSEL31_CON	0x00c0	W	0x00004040	Internal clock select and divide register31
CRU_CLKSEL32_CON	0x00c4	W	0x00000101	Internal clock select and divide register32
CRU_CLKSEL34_CON	0x00cc	W	0x00004141	Internal clock select and divide register34
CRU_CLKGATE0_CON	0x00d0	W	0x00000000	Internal clock gating control register0
CRU_CLKGATE1_CON	0x00d4	W	0x00000000	Internal clock gating control register1

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Name	Offset	Size	Reset Value	Description
CRU_CLKGATE2_CON	0x00d8	W	0x00000000	Internal clock gating control register2
CRU_CLKGATE3_CON	0x00dc	W	0x00000000	Internal clock gating control register3
CRU_CLKGATE4_CON	0x00e0	W	0x00000000	Internal clock gating control register0
CRU_CLKGATE5_CON	0x00e4	W	0x00000000	Internal clock gating control register5
CRU_CLKGATE6_CON	0x00e8	W	0x00000000	Internal clock gating control register6
CRU_CLKGATE7_CON	0x00ec	W	0x00000000	Internal clock gating control register7
CRU_CLKGATE8_CON	0x00f0	W	0x00000000	Internal clock gating control register8
CRU_CLKGATE9_CON	0x00f4	W	0x00000000	Internal clock gating control register9
CRU_CLKGATE10_CON	0x00f8	W	0x00000000	Internal clock gating control register10
CRU_GLB_SRST_FST_VALUE	0x0100	W	0x00000000	The first global software reset config value
CRU_GLB_SRST_SND_VALUE	0x0104	W	0x00000000	The second global software reset config value
CRU_SOFTRST0_CON	0x0110	W	0x00000000	Internal software reset control register0
CRU_SOFTRST1_CON	0x0114	W	0x00000000	Internal software reset control register1
CRU_SOFTRST2_CON	0x0118	W	0x00000000	Internal software reset control register2
CRU_SOFTRST3_CON	0x011c	W	0x00000000	Internal software reset control register3
CRU_SOFTRST4_CON	0x0120	W	0x00000000	Internal software reset control register4
CRU_SOFTRST5_CON	0x0124	W	0x00000000	Internal software reset control register5
CRU_SOFTRST6_CON	0x0128	W	0x00000000	Internal software reset control register6
CRU_SOFTRST7_CON	0x012c	W	0x00000000	Internal software reset control register7
CRU_SOFTRST8_CON	0x0130	W	0x00000000	Internal software reset control register8
CRU_MISC_CON	0x0134	W	0x00008000	SCU control register
CRU_GLB_CNT_TH	0x0140	W	0x3a980064	global reset wait counter threshold
CRU_GLB_RST_ST	0x0150	W	0x00000000	global reset status

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Name	Offset	Size	Reset Value	Description
CRU_SDMMC_CON0	0x01c0	W	0x00000004	sdmmc control0
CRU_SDMMC_CON1	0x01c4	W	0x00000000	sdmmc control1
CRU_SDIO_CON0	0x01c8	W	0x00000004	sdio0 control0
CRU_SDIO_CON1	0x01cc	W	0x00000000	sdio0 control1
CRU_EMMC_CON0	0x01d8	W	0x00000004	emmc control0
CRU_EMMC_CON1	0x01dc	W	0x00000000	emmc control1
CRU_PLL_PRG_EN	0x01f0	W	0x00000000	PLL program enable

*Notes: Size : **B** - Byte (8 bits) access, **HW** - Half WORD (16 bits) access, **W** -WORD (32 bits) access*

2.7.2 Detail Register Description

CRU_APLL_CON0
Address: Operational Base + offset (0x0000)
ARM PLL control register0

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	bp PLL bypass, active high
14:12	RW	0x1	postdiv1 PLL factor postdiv1
11:0	RW	0x0af	fbdiv PLL factor fbdiv

CRU_APLL_CON1
Address: Operational Base + offset (0x0004)
ARM PLL control register1

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	rstmode PLL Reset select 0: internal reset 1: software reset
14	RW	0x0	rst PLL Software Reset 0: normal 1: reset

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Bit	Attr	Reset Value	Description
13	RW	0x0	pd PLL software power down, active high
12	RW	0x1	dsmpd when 1, PLL work at integer mode when 0, PLL work at frac mode
11	RO	0x0	reserved
10	RW	0x0	lock PLL lock status 0: unlock 1: lock
9	RO	0x0	reserved
8:6	RW	0x1	postdiv2 PLL factor postdiv2
5:0	RW	0x06	refdiv PLL factor refdiv

CRU_APLL_CON2
Address: Operational Base + offset (0x0008)
ARM PLL control register2

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27	RW	0x0	fout4phasepd 4 phase clock power down, active high
26	RW	0x0	foutvcopd buffered VCO clock power down, active high
25	RW	0x0	foutpostdivpd post divide power down, active high
24	RW	0x0	dacpd PLL cancellation DAC power down, active high
23:0	RW	0x000001	frac PLL factor frac

CRU_DPLL_CON0
Address: Operational Base + offset (0x0010)
DDR PLL control register0

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	bp PLL bypass, active high
14:12	RW	0x1	postdiv1 PLL factor postdiv1

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Bit	Attr	Reset Value	Description
11:0	RW	0x064	fbdiv PLL factor fbdiv

CRU_DPLL_CON1
Address: Operational Base + offset (0x0014)
DDR PLL control register1

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	rstmode PLL Reset select 0: internal reset 1: software reset
14	RW	0x0	rst PLL Software Reset 0: normal 1: reset
13	RW	0x0	pd PLL software power down, active high
12	RW	0x1	dsmpd when 1, PLL work at integer mode when 0, PLL work at frac mode
11	RO	0x0	reserved
10	RW	0x0	lock PLL lock status 0: unlock 1: lock
9	RO	0x0	reserved
8:6	RW	0x1	postdiv2 PLL factor postdiv2
5:0	RW	0x03	refdiv PLL factor refdiv

CRU_DPLL_CON2
Address: Operational Base + offset (0x0018)
DDR PLL control register2

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27	RW	0x0	fout4phasepd 4 phase clock power down, active high
26	RW	0x0	foutvcopd buffered VCO clock power down, active high

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Bit	Attr	Reset Value	Description
25	RW	0x0	foutpostdivpd post divide power down, active high
24	RW	0x0	dacpd PLL cancellation DAC power down, active high
23:0	RW	0x000001	frac PLL factor frac

CRU_CPLL_CON0
Address: Operational Base + offset (0x0020)
CODEC PLL control register0

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	bp PLL bypass, active high
14:12	RW	0x1	postdiv1 PLL factor postdiv1
11:0	RW	0x07d	fbdiv PLL factor fbdiv

CRU_CPLL_CON1
Address: Operational Base + offset (0x0024)
CODEC PLL control register1

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	rstmode PLL Reset select 0: internal reset 1: software reset
14	RW	0x0	rst PLL Software Reset 0: normal 1: reset
13	RW	0x0	pd PLL software power down, active high
12	RW	0x1	dsmpd when 1, PLL work at integer mode when 0, PLL work at frac mode
11	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
10	RW	0x0	lock PLL lock status 0: unlock 1: lock
9	RO	0x0	reserved
8:6	RW	0x1	postdiv2 PLL factor postdiv2
5:0	RW	0x06	refdiv PLL factor refdiv

CRU_CPLL_CON2
Address: Operational Base + offset (0x0028)
CODEC PLL control register2

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27	RW	0x0	fout4phasepd 4 phase clock power down, active high
26	RW	0x0	foutvcopd buffered VCO clock power down, active high
25	RW	0x0	foutpostdivpd post divide power down, active high
24	RW	0x0	dacpd PLL cancellation DAC power down, active high
23:0	RW	0x000001	frac PLL factor frac

CRU_GPLL_CON0
Address: Operational Base + offset (0x0030)
GENERAL PLL control register0

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	bp PLL bypass, active high
14:12	RW	0x4	postdiv1 PLL factor postdiv1
11:0	RW	0x063	fbdiv PLL factor fbdiv

CRU_GPLL_CON1
Address: Operational Base + offset (0x0034)
GENERAL PLL control register1

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	rstmode PLL Reset select 0: internal reset 1: software reset
14	RW	0x0	rst PLL Software Reset 0: normal 1: reset
13	RW	0x0	pd PLL software power down, active high
12	RW	0x1	dsmpd when 1, PLL work at integer mode when 0, PLL work at frac mode
11	RO	0x0	reserved
10	RW	0x0	lock PLL lock status 0: unlock 1: lock
9	RO	0x0	reserved
8:6	RW	0x1	postdiv2 PLL factor postdiv2
5:0	RW	0x02	refdiv PLL factor refdiv

CRU_GPLL_CON2
Address: Operational Base + offset (0x0038)
GENERAL PLL control register2

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27	RW	0x0	fout4phasepd 4 phase clock power down, active high
26	RW	0x0	foutvcopd buffered VCO clock power down, active high
25	RW	0x0	foutpostdivpd post divide power down, active high
24	RW	0x0	dacpd PLL cancellation DAC power down, active high
23:0	RW	0x000001	frac PLL factor frac

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CRU_MODE_CON
Address: Operational Base + offset (0x0040)
System work mode control register

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:13	RO	0x0	reserved
12	RW	0x0	gpll_work_mode GENERAL PLL work mode select 1'b0: Slow mode, clock from external 24MHz OSC (default) 1'b1: Normal mode, clock from PLL output
11:9	RO	0x0	reserved
8	RW	0x0	cpll_work_mode CODEC PLL work mode select 1'b0: Slow mode, clock from external 24MHz OSC (default) 1'b1: Normal mode, clock from PLL output
7:5	RO	0x0	reserved
4	RW	0x0	dpll_work_mode DDR PLL work mode select 1'b0: Slow mode, clock from external 24MHz OSC (default) 1'b1: Normal mode, clock from PLL output
3:1	RO	0x0	reserved
0	RW	0x0	apll_work_mode ARM PLL work mode select 1'b0: Slow mode, clock from external 24MHz OSC (default) 1'b1: Normal mode, clock from PLL output

CRU_CLKSEL0_CON
Address: Operational Base + offset (0x0044)
Internal clock select and divide register0

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RO	0x0	reserved
14:13	RW	0x0	bus_clk_pll_sel pd_bus aclk_bus pll source selection 2'b00: select CODEC PLL 2'b01: select GENERAL PLL 2'b10: select GENERAL PLL DIV2 2'b11: select GENERAL PLL DIV3
12:8	RW	0x01	aclk_bus_div_con aclk_bus clock divider frequency aclk_bus=bus_clk_src/(aclk_bus_div_con+1)

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Bit	Attr	Reset Value	Description
7	RW	0x0	core_clk_pll_sel core clock pll source selection 1'b0: select ARM PLL 1'b1: select GENERAL PLL div2
6:5	RO	0x0	reserved
4:0	RW	0x00	a7_core_div_con Control A7 core clock divider frequency clk_core=core_clk_src/(a7_core_div_con+1)

CRU_CLKSEL1_CON
Address: Operational Base + offset (0x0048)
Internal clock select and divide register1

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RO	0x0	reserved
14:12	RW	0x3	bus_pclk_div_con Control bus subsystem APB clock divider frequency pclk_bus=bus_aclk_src/(bus_pclk_div_con+1)
11:10	RO	0x0	reserved
9:8	RW	0x1	bus_hclk_div_con Control bus subsystem AHB clock divider frequency hclk_bus=bus_aclk_src/(bus_hclk_div_con+1)
7	RO	0x0	reserved
6:4	RW	0x1	core_aclk_div_con Control A7 core axi clock divider frequency aclk_core=core_clk_src/(core_aclk_div_con+1)
3:0	RW	0x3	pclk_dbg_div_con pclk_dbg div control pclk_debg=pclk_dbg_src/(pclk_dbg_div_con+1)

CRU_CLKSEL2_CON
Address: Operational Base + offset (0x004c)
Internal clock select and divide register2

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit

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Bit	Attr	Reset Value	Description
15:14	RW	0x0	nandc_clk_pll_sel nandc pll source selection 2'b00: select codec pll clock 2'b01: select general pll clock 2'b10: select general pll div2 clock
13	RO	0x0	reserved
12:8	RW	0x07	nandc_div_con Control NANDC clock divider frequency clk_nandc=nandc_clk_src/(nandc_div_con+1)
7	RO	0x0	reserved
6:0	RW	0x07	pvtm_div_con func pvtm clock divider frequency clk_pvtm=pvtm_clk_src/(pvtm_div_con+1)

CRU_CLKSEL3_CON

Address: Operational Base + offset (0x0050)

Internal clock select and divide register3

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:14	RW	0x0	i2s_2ch_pll_sel Control I2S_2ch PLL source selection 2'b00: select codec pll clock 2'b01: select general pll clock 2'b10: select general pll div2 clock
13	RO	0x0	reserved
12	RW	0x0	i2s_2ch_clkout_sel I2S_2ch output clock selection 1'b0: select cru generated clock 1'b1: select 12M clock
11:10	RO	0x0	reserved
9:8	RW	0x0	i2s_2ch_clk_sel Control I2S_2ch clock work frequency selection 2'b00: select divider output from pll divider 2'b01: select divider output from fraction divider 2'b10: select io input clock 2'b11: select 12MHz from osc input
7	RO	0x0	reserved
6:0	RW	0x1f	i2s_2ch_pll_div_con Control I2S_2ch PLL output divider frequency i2s_div_clk=i2s_div_src/(i2s_pll_div_con+1)

CRU_CLKSEL4_CON

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Address: Operational Base + offset (0x0054)
Internal clock select and divide register4

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:13	RO	0x0	reserved
12:8	RW	0x00	clk_24m_div_con Control clk_24m divider frequency 24m_div_clk=clk_24m/(clk_24m_div_con+1)
7:6	RW	0x0	tsp_pll_sel Control TSP clock PLL source selection 2'b00: select codec pll clock 2'b01: select general pll clock 2'b10: select general pll div2 clock
5	RO	0x0	reserved
4:0	RW	0x03	clk_tsp_div_con Control clk_tsp divider frequency tsp_div_clk=tsp_div_src/(clk_tsp_div_con+1)

CRU_CLKSEL5_CON
Address: Operational Base + offset (0x0058)
Internal clock select and divide register5

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	rmii_extclk_sel Control RMII external clock selection 1'b0: select internal divider clock 1'b1: select external input clock
14:8	RO	0x0	reserved
7:6	RW	0x0	mac_pll_sel Control MAC clock PLL source selection 2'b00: select codec pll clock 2'b01: select general pll clock 2'b10: select general pll div2 clock
5	RO	0x0	reserved
4:0	RW	0x03	clk_mac_div_con Control clk_mac divider frequency mac_div_clk=mac_div_src/(clk_mac_div_con+1)

CRU_CLKSEL6_CON
Address: Operational Base + offset (0x005c)

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Internal clock select and divide register6

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:14	RW	0x0	spdif_pll_sel Control SPDIF PLL source selection 2'b00: select codec pll clock 2'b01: select general pll clock 2'b10: select general pll div2 clock
13:10	RO	0x0	reserved
9:8	RW	0x2	spdif_clk_sel Control SPDIF clock work frequency selection 2'b00: select divider output from pll divider 2'b01: select divider output from fraction divider 2'b10: select 12MHz from osc inpu
7	RO	0x0	reserved
6:0	RW	0x1f	spdif_pll_div_con Control SPDIF PLL output divider frequency spdif_div_clk=spdif_div_src/(spdif_pll_div_con+1)

CRU_CLKSEL7_CON

Address: Operational Base + offset (0x0060)

Internal clock select and divide register7

Bit	Attr	Reset Value	Description
31:0	RW	0x0bb8ea60	i2s_2ch_frac_factor Control I2S 2channel fraction divider frequency High 16-bit for numerator Low 16-bit for denominator

CRU_CLKSEL8_CON

Address: Operational Base + offset (0x0064)

Internal clock select and divide register8

Bit	Attr	Reset Value	Description
31:0	RW	0x0bb8ea60	i2s_8ch_frac_factor Control I2S 8channel fraction divider frequency High 16-bit for numerator Low 16-bit for denominator

CRU_CLKSEL9_CON

Address: Operational Base + offset (0x0068)

Internal clock select and divide register9

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:14	RW	0x0	i2s_8ch_pll_sel Control I2S_8ch PLL source selection 2'b00: select codec pll clock 2'b01: select general pll clock 2'b10: select general pll div2 clock
13:10	RO	0x0	reserved
9:8	RW	0x0	i2s_8ch_clk_sel Control I2S_8ch clock work frequency selection 2'b00: select divider output from pll divider 2'b01: select divider output from fraction divider 2'b10: select io input clock 2'b11: select 12MHz from osc input
7	RO	0x0	reserved
6:0	RW	0x1f	i2s_8ch_pll_div_con Control I2S_8ch PLL output divider frequency i2s_div_clk=i2s_div_src/(i2s_pll_div_con+1)

CRU_CLKSEL10_CON

Address: Operational Base + offset (0x006c)

Internal clock select and divide register10

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:14	RW	0x2	peri_pll_sel Control peripheral clock PLL source selection 2'b00: select general pll clock 2'b01: select codec pll clock 2'b10: select general div2 pll clock 2'b11: select general div3 pll clock
13:12	RW	0x2	peri_pclk_div_con Control the divider ratio between aclk_periph and pclk_periph 2'b00: aclk_periph:pclk_periph = 1:1 2'b01: aclk_periph:pclk_periph = 2:1 2'b10: aclk_periph:pclk_periph = 4:1 2'b11: aclk_periph:pclk_periph = 8:1
11:10	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
9:8	RW	0x1	peri_hclk_div_con Control the divider ratio between aclk_periph and hclk_periph 2'b00: aclk_periph:hclk_periph = 1:1 2'b01: aclk_periph:hclk_periph = 2:1 2'b10: aclk_periph:hclk_periph = 4:1
7:5	RO	0x0	reserved
4:0	RW	0x00	peri_aclk_div_con Control periphral clock divider frequency aclk_periph=periph_clk_src/(peri_aclk_div_con+1)

CRU_CLKSEL11_CON
Address: Operational Base + offset (0x0070)
Internal clock select and divide register11

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:14	RW	0x0	sfc_clk_pll_sel sfc pll source selection 2'b00: select codec pll clock 2'b01: select general pll clock 2'b10: select general pll div2 clock 2'b11: select 24M clock
13	RO	0x0	reserved
12:8	RW	0x00	sfc_div_con Control SFC clock divider frequency clk_sfc=sfc_clk_src/(sfc_div_con+1)
7:6	RW	0x0	mmc0_pll_sel Control mmc clock PLL source selection 2'b00: select codec pll clock 2'b01: select general pll clock 2'b10: select general pll div2 clock 2'b11: select 24M clock
5:0	RW	0x17	mmc0_div_con Control SDMMC0 divider frequency clk_sdmmc0=general_pll_clk/(mmc0_div_con+1)

CRU_CLKSEL12_CON
Address: Operational Base + offset (0x0074)
Internal clock select and divide register12

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:14	RW	0x0	emmc_pll_sel Control emmc clock PLL source selection 2'b00: select codec pll clock 2'b01: select general pll clock 2'b10: select general pll div2 clock 2'b11: select 24M clock
13:8	RW	0x17	emmc_div_con Control EMMC divider frequency clk_emmc=general_pll_clk/(emmc_div_con+1)
7:6	RW	0x0	sdio_pll_sel Control sdio clock PLL source selection 2'b00: select codec pll clock 2'b01: select general pll clock 2'b10: select general pll div2 clock 2'b11: select 24M clock
5:0	RW	0x17	sdio_div_con Control SDIO divider frequency clk_sdio=general_pll_clk/(sdio_div_con+1)

CRU_CLKSEL13_CON

Address: Operational Base + offset (0x0078)

Internal clock select and divide register13

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:14	RW	0x0	uart12_pll_sel Control UART1 and UART2 clock PLL source selection 2'b00: select codec pll clock 2'b01: select general pll clock 2'b10: select general pll div2 clock
13:12	RW	0x1	uart0_pll_sel Control UART0 clock PLL source selection 2'b00: select codec pll clock 2'b01: select general pll clock 2'b10: select general pll div2 clock 2'b11: select USBPHY 480M clock
11:10	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
9:8	RW	0x2	uart0_clk_sel Control UART0 clock work frequency selection 2'b00: select divider output from pll divider 2'b01: select divider output from fraction divider 2'b10: select 24MHz from osc inpu
7	RO	0x0	reserved
6:0	RW	0x1f	uart0_div_con Control UART0 divider frequency clk_uart0=uart_clk_src/(uart0_div_con+1)

CRU_CLKSEL14_CON
Address: Operational Base + offset (0x007c)
Internal clock select and divide register14

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:10	RO	0x0	reserved
9:8	RW	0x2	uart1_clk_sel Control UART1 clock work frequency selection 2'b00: select divider output from pll divider 2'b01: select divider output from fraction divider 2'b10: select 24MHz from osc inpu
7	RO	0x0	reserved
6:0	RW	0x1f	uart1_div_con Control UART1 divider frequency clk_uart1=uart_clk_src/(uart1_div_con+1)

CRU_CLKSEL15_CON
Address: Operational Base + offset (0x0080)
Internal clock select and divide register15

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:10	RO	0x0	reserved
9:8	RW	0x2	uart2_clk_sel Control UART2 clock work frequency selection 2'b00: select divider output from pll divider 2'b01: select divider output from fraction divider 2'b10: select 24MHz from osc inpu
7	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
6:0	RW	0x1f	uart2_div_con Control UART2 divider frequency clk_uart2=uart_clk_src/(uart2_div_con+1)

CRU_CLKSEL17_CON
Address: Operational Base + offset (0x0088)
Internal clock select and divide register17

Bit	Attr	Reset Value	Description
31:0	RW	0x0bb8ea60	uart0_frac_factor Control UART0 fraction divider frequency High 16-bit for numerator Low 16-bit for denominator

CRU_CLKSEL18_CON
Address: Operational Base + offset (0x008c)
Internal clock select and divide register18

Bit	Attr	Reset Value	Description
31:0	RW	0x0bb8ea60	uart1_frac_factor Control UART1 fraction divider frequency High 16-bit for numerator Low 16-bit for denominator

CRU_CLKSEL19_CON
Address: Operational Base + offset (0x0090)
Internal clock select and divide register19

Bit	Attr	Reset Value	Description
31:0	RW	0x0bb8ea60	uart2_frac_factor Control UART2 fraction divider frequency High 16-bit for numerator Low 16-bit for denominator

CRU_CLKSEL20_CON
Address: Operational Base + offset (0x0094)
Internal clock select and divide register20

Bit	Attr	Reset Value	Description
31:0	RW	0x0bb8ea60	spdif_frac_factor Control SPDIF fraction divider frequency High 16-bit for numerator Low 16-bit for denominator

CRU_CLKSEL23_CON
Address: Operational Base + offset (0x00a0)
Internal clock select and divide register23

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:8	RW	0x01	ebc_dclk_div_con Control EBC clock divider frequency dclk_ebc=ebc_dclk_src/(ebc_dclk_div_con+1)
7:2	RO	0x0	reserved
1:0	RW	0x0	ebc_dclk_pll_sel Control EBC display clock PLL source selection 2'b00: select codec pll clock 2'b01: select general pll clock 2'b10: select general pll div2 clock

CRU_CLKSEL24_CON
Address: Operational Base + offset (0x00a4)
Internal clock select and divide register24

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:8	RW	0x17	saradc_div_con Control SARADC clock divider frequency clk_saradc=24MHz/(saradc_div_con+1)
7:2	RO	0x0	reserved
1:0	RW	0x1	crypto_div_con crypto clock divider frequency clk=clk/(div_con+1)

CRU_CLKSEL25_CON
Address: Operational Base + offset (0x00a8)
Internal clock select and divide register25

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:10	RO	0x0	reserved
9:8	RW	0x1	spi_clk_pll_sel SPI clock pll source selection 2'b00: select codec pll clock 2'b01: select general pll clock 2'b10: select general pll div2 clock
7	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
6:0	RW	0x1f	spi0_div_con Control SPI0 clock divider frequency clk_spi0=general_pll_clk/(spi0_div_con+1)

CRU_CLKSEL26_CON
Address: Operational Base + offset (0x00ac)
Internal clock select and divide register26

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:9	RO	0x0	reserved
8	RW	0x0	ddr_clk_pll_sel DDR clock pll source selection 1'b0: select DDR PLL 1'b1: select GENERAL PLL div2
7:2	RO	0x0	reserved
1:0	RW	0x0	ddr_div_sel Control DDR divider frequency 2'b00: clk_ddr_src:clk_ddrphy = 1:1 2'b01: clk_ddr_src:clk_ddrphy = 2:1 2'b10: clk_ddr_src:clk_ddrphy = 4:1

CRU_CLKSEL27_CON
Address: Operational Base + offset (0x00b0)
Internal clock select and divide register27

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:8	RW	0x03	vop_dclk_div_con Control VOP clock divider frequency dclk_vop=vop_dclk_src/(vop_dclk_div_con+1)
7:2	RO	0x0	reserved
1:0	RW	0x1	vop_dclk_pll_sel Control VOP display clock PLL source selection 2'b00: select codec pll clock 2'b01: select general pll clock 2'b10: select general pll div2 clock 2'b11: select general pll div3 clock

CRU_CLKSEL28_CON
Address: Operational Base + offset (0x00b4)

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Internal clock select and divide register28

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:8	RW	0x03	vop_sclk_div_con Control VOP display clock divider frequency sclk_vop=vop_sclk_src/(vop_sclk_div_con+1)
7:2	RO	0x0	reserved
1:0	RW	0x1	vop_sclk_pll_sel Control VOP display clock PLL source selection 2'b00: select codec pll clock 2'b01: select general pll clock 2'b10: select general pll div2 clock 2'b11: select general pll div3 clock

CRU_CLKSEL29_CON

Address: Operational Base + offset (0x00b8)

Internal clock select and divide register29

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:14	RO	0x0	reserved
13:8	RW	0x05	pmu_div_con Control PMU clock divider frequency clk_pmu=pmu_clk_src/(pmu_div_con+1)
7	RW	0x0	cif_clk_sel Control CIF clock selection 1'b0: select from PLL divider output 1'b1: select from 24MHz osc
6:2	RW	0x09	cif_div_con Control CIF clock divider frequency clk_cif=cif_clk_src/(cif_div_con+1)
1:0	RW	0x0	cif_pll_sel Control CIF clock PLL source selection 2'b00: select codec pll clock 2'b01: select general pll clock 2'b10: select general pll div2 clock 2'b11: usbphy480M

CRU_CLKSEL30_CON

Address: Operational Base + offset (0x00bc)

Internal clock select and divide register30

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:14	RW	0x0	vio_hclk_pll_sel Control VIO AHB clock PLL source selection 2'b00: select codec pll clock 2'b01: select general pll clock 2'b10: select general pll div2 clock 2'b11: select usbphy 480m clock
13	RO	0x0	reserved
12:8	RW	0x03	vio_hclk_div_con Control VIO AHB clock divider frequency hclk_vio=vio_hclk_src/(vio_hclk_div_con+1)
7	RW	0x0	cif_clkin_inv_sel CIF input clock inverter selection 1'b0: select not invert 1'b1: select invert
6:5	RO	0x0	reserved
4:0	RW	0x00	testout_div_con testout clock divider frequency clk_testout=testout_clk_src/(testout_div_con+1)

CRU_CLKSEL31_CON
Address: Operational Base + offset (0x00c0)
Internal clock select and divide register31

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:13	RW	0x2	vio1_aclk_pll_sel Control VIO1 AXI clock PLL source selection 3'b000: select codec pll clock 3'b001: select general pll clock 3'b010: select general pll div2 clock 3'b011: select general pll div3 clock 3'b100: select USBPHY 480M clock
12:8	RW	0x00	vio1_aclk_div_con Control VIO1 AXI clock divider frequency aclk_vio1=vio1_aclk_src/(vio1_aclk_div_con+1)

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Bit	Attr	Reset Value	Description
7:5	RW	0x2	vio0_aclk_pll_sel Control VIO0 AXI clock PLL source selection 3'b000: select codec pll clock 3'b001: select general pll clock 3'b010: select general pll div2 clock 3'b011: select general pll div3 clock 3'b100: select USBPHY 480M clock
4:0	RW	0x00	vio0_aclk_div_con Control VIO0 AXI clock divider frequency aclk_vio0=vio0_aclk_src/(vio0_aclk_div_con+1)

CRU_CLKSEL32_CON
Address: Operational Base + offset (0x00c4)
Internal clock select and divide register32

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:13	RW	0x0	vdpu_aclk_pll_sel Control VDPU AXI clock PLL source selection 3'b000: select codec pll clock 3'b001: select general pll clock 3'b010: select general pll div2 clock 3'b011: select general pll div3 clock 3'b100: select USBPHY 480M clock
12:8	RW	0x01	vdpu_aclk_div_con Control VDPU AXI clock divider frequency aclk_vdpu=vdpu_aclk_src/(vdpu_aclk_div_con+1)
7:5	RW	0x0	vepu_aclk_pll_sel Control VEPU AXI clock PLL source selection 3'b000: select codec pll clock 3'b001: select general pll clock 3'b010: select general pll div2 clock 3'b011: select general pll div3 clock 3'b100: select USBPHY 480M clock
4:0	RW	0x01	vepu_aclk_div_con Control VEPU AXI clock divider frequency aclk_vepu=vepu_aclk_src/(vepu_aclk_div_con+1)

CRU_CLKSEL34_CON
Address: Operational Base + offset (0x00cc)
Internal clock select and divide register34

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:13	RW	0x2	hevc_core_clk_pll_sel HEVC CORE clock PLL source selection 3'b000: select codec pll clock 3'b001: select general pll clock 3'b010: select general pll div2 clock 3'b011: select general pll div3 clock 3'b100: select USBPHY 480M clock
12:8	RW	0x01	hevc_core_clk_div_con HEVC CORE clock divider frequency clk_hevc_core=hevccore_clk_src/(hevc_core_clk_div_con+1)
7:5	RW	0x2	gpu_aclk_pll_sel Control GPU AXI clock PLL source selection 3'b000: select codec pll clock 3'b001: select general pll clock 3'b010: select general pll div2 clock 3'b011: select general pll div3 clock 3'b100: select USBPHY 480M clock
4:0	RW	0x01	gpu_aclk_div_con Control GPU AXI clock divider frequency aclk_gpu=gpu_aclk_src/(gpu_aclk_div_con+1)

CRU_CLKGATE0_CON

Address: Operational Base + offset (0x00d0)

Internal clock gating control register0

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	testclk_gate_en Test output clock disable When HIGH, disable clock
14	RW	0x0	clk_i2s_2ch_gate_en I2S_2ch clock disable. When HIGH, disable clock
13	RW	0x0	clk_i2s_2ch_out_gate_en I2S_2ch output clock disable. When HIGH, disable clock
12	RW	0x0	clk_crypto_gate_en crypto clock disable. When HIGH, disable clock

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Bit	Attr	Reset Value	Description
11	RW	0x0	hclk_disp_gate_en display AHB clock disable. When HIGH, disable clock
10	RW	0x0	clk_i2s_2ch_frac_src_gate_en I2S_2ch fraction divider source clock disable. When HIGH, disable clock
9	RW	0x0	clk_i2s_2ch_src_gate_en I2S_2ch source clock disable. When HIGH, disable clock
8	RO	0x0	reserved
7	RW	0x0	aclk_core_gate_en ARM core axi clock(aclk_core) disable. When HIGH, disable clock
6	RW	0x0	core_src_clk_gate_en CORE source clock path clock disable. When HIGH, disable clock
5	RW	0x0	pclk_bus_gate_en BUS system APB clock(pclk_bus_pre) disable. When HIGH, disable clock , This bit suggests keep enable.
4	RW	0x0	hclk_bus_gate_en BUS system AHB clock(hclk_bus_pre) disable. When HIGH, disable clock, This bit suggests keep enable.
3	RW	0x0	aclk_bus_gate_en BUS system AXI clock(aclk_bus_pre) disable. When HIGH, disable clock, This bit suggests keep enable.
2	RW	0x0	clk_ddrphy_src_gate_en DDR PHY clock(clk_ddrphy) disable. When HIGH, disable clock
1	RW	0x0	bus_src_clk_gate_en BUS clock source clock disable. When HIGH, disable clock, This bit suggests keep enable.
0	RW	0x0	clk_core_periph_gate_en ARM core peripheral clock(clk_core_periph) disable. When HIGH, disable clock

CRU_CLKGATE1_CON

Address: Operational Base + offset (0x00d4)

Internal clock gating control register1

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
14	RW	0x0	clk_tsp_gate_en clk_tsp clock disable. When HIGH, disable clock
13	RW	0x0	clk_uart2_frac_src_gate_en UART2 fraction divider source clock disable. When HIGH, disable clock
12	RW	0x0	clk_uart2_src_gate_en UART2 source clock disable. When HIGH, disable clock
11	RW	0x0	clk_uart1_frac_src_gate_en UART1 fraction divider source clock disable. When HIGH, disable clock
10	RW	0x0	clk_uart1_src_gate_en UART1 source clock disable. When HIGH, disable clock
9	RW	0x0	clk_uart0_frac_src_gate_en UART0 fraction divider source clock disable. When HIGH, disable clock
8	RW	0x0	clk_uart0_src_gate_en UART0 source clock disable. When HIGH, disable clock
7	RW	0x0	clk_mac_src_gate_en clk_mac source clock disable. When HIGH, disable clock
6	RW	0x0	clk_otgphy1_gate_en OTGPHY1 clock(clk_otgphy1) disable. When HIGH, disable clock
5	RW	0x0	clk_otgphy_gate_en OTGPHY UTMI reference clock (utmi_ref_clk) disable. When HIGH, disable clock
4	RW	0x0	aclk_vio1_src_gate_en aclk_vio1_src clock disable. When HIGH, disable clock
3	RW	0x0	clk_jtag_gate_en JTAG clock disable. When HIGH, disable clock
2:1	RO	0x0	reserved
0	RW	0x0	pclk_pmu_src_gate_en pclk_pmu src clock disable. When HIGH, disable clock

CRU_CLKGATE2_CON
Address: Operational Base + offset (0x00d8)
Internal clock gating control register2

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	clk_mipiphy_24m_gate_en MIPI PHY 24M clock disable. When HIGH, disable clock
14	RW	0x0	clk_emmc_src_gate_en EMMC source clock disable. When HIGH, disable clock
13	RW	0x0	clk_sdio_src_gate_en SDIO source clock disable. When HIGH, disable clock
12	RW	0x0	clk_spdif_frac_src_gate_en SPDIF fraction divider source clock disable. When HIGH, disable clock
11	RW	0x0	clk_mmc0_src_gate_en SDMMC0 source clock disable. When HIGH, disable clock
10	RW	0x0	clk_spdif_src_gate_en SPDIF source clock disable. When HIGH, disable clock
9	RW	0x0	clk_spi0_src_gate_en SPI0 source clock disable. When HIGH, disable clock
8	RW	0x0	clk_saradc_src_gate_en SARADC source clock disable. When HIGH, disable clock
7	RW	0x0	clk_mac_tx_gate_en clk_mac_tx clock disable. When HIGH, disable clock
6	RW	0x0	clk_mac_rx_gate_en clk_mac_rx clock disable. When HIGH, disable clock
5	RW	0x0	clk_mac_refout_gate_en clk_mac_refout clock disable. When HIGH, disable clock
4	RW	0x0	clk_mac_ref_gate_en clk_mac_ref clock disable. When HIGH, disable clock
3	RW	0x0	pclk_periph_gate_en PERIPH system APB clock(pclk_periph) disable. When HIGH, disable clock

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Bit	Attr	Reset Value	Description
2	RW	0x0	hclk_periph_gate_en PERIPH system AHB clock(hclk_periph) disable. When HIGH, disable clock
1	RW	0x0	aclk_periph_gate_en PERIPH system AXI clock(aclk_periph) disable. When HIGH, disable clock
0	RW	0x0	clk_periph_src_gate_en PERIPH system source clock disable. When HIGH, disable clock

CRU_CLKGATE3_CON

Address: Operational Base + offset (0x00dc)

Internal clock gating control register3

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	clk_sfc_gate_en sfc clock disable. When HIGH, disable clock
14	RW	0x0	hclk_gps_gate_en GPS AHB bus source axi clock disable. When HIGH, disable clock
13	RW	0x0	aclk_gpu_src_gate_en GPU AXI source clock disable. When HIGH, disable clock
12	RW	0x0	hclk_vdpu_gate_en VDPU AHB source clock disable. When HIGH, disable clock
11	RW	0x0	aclk_vdpu_src_gate_en VDPU AXI source clock disable. When HIGH, disable clock, This bit suggests keep enable.
10	RW	0x0	clk_hevc_core_src_gate_en HEVC CORE clk source clock(clk_cif_out) disable. When HIGH, disable clock
9	RW	0x0	aclk_vepu_src_gate_en VEPU AXI source clock disable. When HIGH, disable clock, This bit suggests keep enable.
8	RW	0x0	pclk_hdmi_gate_en HDMI APB bus clock disable. When HIGH, disable clock
7	RW	0x0	clk_cif_out_src_gate_en CIF out clk source clock(clk_cif_out) disable. When HIGH, disable clock

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Bit	Attr	Reset Value	Description
6	RW	0x0	hclk_emem_peri_gate_en hclk_emem_peri souce clock disable. When HIGH, disable clock
5	RW	0x0	hclk_crypto_gate_en hclk_crypto clock disable. When HIGH, disable clock
4	RW	0x0	dclk_ebc_src_gate_en EBC DCLK souce clock disable. When HIGH, disable clock
3	RW	0x0	pclkin_cif_gate_en CIF pix input clk source clock disable. When HIGH, disable clock
2	RW	0x0	sclk_vop_src_gate_en VOP SCLK souce clock disable. When HIGH, disable clock
1	RW	0x0	dclk_vop_src_gate_en VOP DCLK souce clock disable. When HIGH, disable clock
0	RW	0x0	aclk_vio0_src_gate_en VIO0 AXI source clock disable. When HIGH, disable clock, This bit suggests keep enable.

CRU_CLKGATE4_CON
Address: Operational Base + offset (0x00e0)
Internal clock gating control register0

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:13	RO	0x0	reserved
12	RW	0x0	aclk_intmem_gate_en Internal memory AXI clock(aclk_intmem) disable. When HIGH, disable clock, This bit suggests keep enable.
11	RO	0x0	reserved
10	RW	0x0	aclk_bus_niu_gate_en BUS system NIU AXI clock disable. When HIGH, disable clock, This bit suggests keep enable.
9:7	RO	0x0	reserved
6	RW	0x0	clk_i2s_8ch_gate_en I2S_8ch clock disable. When HIGH, disable clock
5	RW	0x0	clk_i2s_8ch_frac_src_gate_en I2S_8ch fraction divider source clock disable. When HIGH, disable clock

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Bit	Attr	Reset Value	Description
4	RW	0x0	clk_i2s_8ch_src_gate_en I2S_8ch source clock disable. When HIGH, disable clock
3	RW	0x0	aclk_peri_axi_niu_gate_en PERIPH BUS NIU AXI clock disable. When HIGH, disable clock, This bit suggests keep enable.
2	RW	0x0	aclk_peri_gate_en PERIPH AXI clock disable. When HIGH, disable clock, This bit suggests keep enable.
1	RW	0x0	pclk_peri_axi_niu_gate_en PERIPH BUS NIU APB clock disable. When HIGH, disable clock, This bit suggests keep enable.
0	RW	0x0	hclk_peri_axi_niu_gate_en PERIPH BUS NIU AHB clock disable. When HIGH, disable clock, This bit suggests keep enable.

CRU_CLKGATE5_CON

Address: Operational Base + offset (0x00e4)

Internal clock gating control register5

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RO	0x0	reserved
14	RW	0x0	pclk_acodec_gate_en audio codec APB clock disable. When HIGH, disable clock
13	RW	0x0	hclk_otg0_gate_en USB OTG PHY0 AHB clock disable. When HIGH, disable clock
12	RO	0x0	reserved
11	RW	0x0	hclk_sdio_gate_en SDIO AHB clock disable. When HIGH, disable clock
10	RW	0x0	hclk_sdmmc0_gate_en SDMMC0 AHB clock disable When HIGH, disable clock
9	RW	0x0	hclk_nandc_gate_en NANDC AHB clock disable When HIGH, disable clock
8	RO	0x0	reserved
7	RW	0x0	pclk_ddrupctl_gate_en DDR uPCTL APB clock disable. When HIGH, disable clock, This bit suggests keep enable.

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Bit	Attr	Reset Value	Description
6	RW	0x0	hclk_rom_gate_en ROM AHB clock disable. When HIGH, disable clock
5	RO	0x0	reserved
4	RW	0x0	pclk_grf_gate_en GRF APB clock disable. When HIGH, disable clock, This bit suggests keep enable.
3	RO	0x0	reserved
2	RW	0x0	pclk_eFuse_gate_en EFUSE APB clock disable. When HIGH, disable clock
1	RW	0x0	aclk_dmac_gate_en DMAC AXI clock disable. When HIGH, disable clock
0	RW	0x0	pclk_mipiphy_gate_en mipiphy apb clock disable. When HIGH, disable clock

CRU_CLKGATE6_CON

Address: Operational Base + offset (0x00e8)

Internal clock gating control register6

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:14	RO	0x0	reserved
13	RW	0x0	aclk_vio0_gate_en VIO0 AXI clock disable. When HIGH, disable clock, This bit suggests keep enable.
12	RW	0x0	hclk_vio_bus_gate_en VIO AHB bus clock disable. When HIGH, disable clock, This bit suggests keep enable.
11	RW	0x0	aclk_rga_gate_en RGA AXI clock disable. When HIGH, disable clock
10	RW	0x0	hclk_rga_gate_en RGA AHB clock disable. When HIGH, disable clock
9:6	RO	0x0	reserved
5	RW	0x0	aclk_cif_gate_en CIF AXI clock disable. When HIGH, disable clock

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Bit	Attr	Reset Value	Description
4	RW	0x0	hclk_cif_gate_en CIF AHB clock disable. When HIGH, disable clock
3:2	RO	0x0	reserved
1	RW	0x0	hclk_vio_gate_en VIO AHB clock disable. When HIGH, disable clock
0	RW	0x0	aclk_vio0_gate_en VIO0 AXI clock disable. When HIGH, disable clock

CRU_CLKGATE7_CON
Address: Operational Base + offset (0x00ec)
Internal clock gating control register7

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	pclk_wdt_gate_en WDT APB clock disable. When HIGH, disable clock
14	RW	0x0	pclk_saradc_gate_en SARADC APB clock disable. When HIGH, disable clock
13	RO	0x0	reserved
12	RW	0x0	pclk_spi0_gate_en SPI0 APB clock disable. When HIGH, disable clock
11	RO	0x0	reserved
10	RW	0x0	pclk_pwm01_gate_en PWM0 and PWM1 APB clock disable. When HIGH, disable clock
9:8	RO	0x0	reserved
7	RW	0x0	pclk_timer_gate_en TIMER APB clock disable. When HIGH, disable clock
6:5	RO	0x0	reserved
4	RW	0x0	hclk_i2s_8ch_gate_en I2S_8ch AHB clock disable. When HIGH, disable clock
3	RW	0x0	hclk_host_gate_en USB HOST PHY AHB clock disable. When HIGH, disable clock

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Bit	Attr	Reset Value	Description
2	RW	0x0	hclk_i2s_2ch_gate_en I2S_2ch AHB clock disable. When HIGH, disable clock
1	RW	0x0	hclk_sfc_gate_en SFC AHB clock disable. When HIGH, disable clock
0	RW	0x0	hclk_emmc_gate_en EMMC AHB clock disable. When HIGH, disable clock

CRU_CLKGATE8_CON

Address: Operational Base + offset (0x00f0)

Internal clock gating control register8

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:13	RO	0x0	reserved
12	RW	0x0	pclk_gpio3_gate_en GPIO3 APB clock disable. When HIGH, disable clock
11	RW	0x0	pclk_gpio2_gate_en GPIO2 APB clock disable. When HIGH, disable clock
10	RW	0x0	pclk_gpio1_gate_en GPIO1 APB clock disable. When HIGH, disable clock
9	RW	0x0	pclk_gpio0_gate_en GPIO0 APB clock disable. When HIGH, disable clock
8	RO	0x0	reserved
7	RW	0x0	pclk_i2c3_gate_en I2C3 APB clock disable. When HIGH, disable clock
6	RW	0x0	pclk_i2c2_gate_en I2C2 APB clock disable. When HIGH, disable clock
5	RW	0x0	pclk_i2c1_gate_en I2C1 APB clock disable. When HIGH, disable clock
4	RW	0x0	pclk_i2c0_gate_en I2C0 APB clock disable. When HIGH, disable clock
3	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
2	RW	0x0	pclk_uart2_gate_en UART2 APB clock disable. When HIGH, disable clock
1	RW	0x0	pclk_uart1_gate_en UART1 APB clock disable. When HIGH, disable clock
0	RW	0x0	pclk_uart0_gate_en UART0 APB clock disable. When HIGH, disable clock

CRU_CLKGATE9_CON

Address: Operational Base + offset (0x00f4)

Internal clock gating control register9

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	aclk_peri_niu_clock_en periph NIU AXI clock disable. When HIGH, disable clock, This bit suggests keep enable.
14	RW	0x0	hclk_peri_arbi_clock_en periph arbitor AHB clock disable. When HIGH, disable clock, This bit suggests keep enable.
13	RW	0x0	hclk_usb_peri_clock_en USB peri AHB clock disable. When HIGH, disable clock
12	RW	0x0	pclk_sim_clock_en SIM card APB clock disable. When HIGH, disable clock
11	RO	0x0	reserved
10	RW	0x0	aclk_vio1_clock_en VIO1 AXI clock disable. When HIGH, disable clock, This bit suggests keep enable.
9	RW	0x0	hclk_ebc_clock_en EBC AHB clock disable. When HIGH, disable clock
8	RW	0x0	aclk_iep_clock_en IEP AXI clock disable. When HIGH, disable clock
7	RW	0x0	hclk_iep_clock_en IEP AHB clock disable. When HIGH, disable clock

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Bit	Attr	Reset Value	Description
6	RW	0x0	pclk_vio_mipi_gate_en pd_vio mipi controller clock disable. When HIGH, disable clock
5	RW	0x0	hclk_vio_h2p_gate_en pd_vio AHB h2p bridge clock disable. When HIGH, disable clock
4	RO	0x0	reserved
3	RW	0x0	pclk_pmu_niu_clock_en PD_PMU NOC APB clock disable. When HIGH, disable clock, This bit suggests keep enable.
2	RW	0x0	pclk_pmu_clock_en PMU APB clock disable. When HIGH, disable clock, This bit suggests keep enable.
1:0	RO	0x0	reserved

CRU_CLKGATE10_CON
Address: Operational Base + offset (0x00f8)
Internal clock gating control register10

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	clk_nandc_gate_en Nandc clock disable. When HIGH, disable clock
14	RW	0x0	clk_old_usb_host_gate_en old usb host clock disable. When HIGH, disable clock
13	RW	0x0	clkin_tsp_gate_en TSP IO clkin clock disable. When HIGH, disable clock
12	RW	0x0	hclk_tsp_gate_en TSP AHB clock disable. When HIGH, disable clock
11	RW	0x0	pclk_gmac_gate_en GMAC APB clock disable. When HIGH, disable clock
10	RW	0x0	aclk_gmac_gate_en GMAC AXI clock disable. When HIGH, disable clock
9	RW	0x0	hclk_spdif_8ch_gate_en spdif_8ch AHB clock disable. When HIGH, disable clock

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Bit	Attr	Reset Value	Description
8	RW	0x0	clk_timer5_gate_en Timer5 clock disable. When HIGH, disable clock
7	RW	0x0	clk_timer4_gate_en Timer4 clock disable. When HIGH, disable clock
6	RW	0x0	clk_timer3_gate_en Timer3 clock disable. When HIGH, disable clock
5	RW	0x0	clk_timer2_gate_en Timer2 clock disable. When HIGH, disable clock
4	RW	0x0	clk_timer1_gate_en Timer1 clock disable. When HIGH, disable clock
3	RW	0x0	clk_timer0_gate_en Timer0 clock disable. When HIGH, disable clock
2	RW	0x0	func_pvtm_gate_en FUNC PVTM clock disable. When HIGH, disable clock
1	RW	0x0	gpu_pvtm_gate_en PD_GPU PVTM clock disable. When HIGH, disable clock
0	RW	0x0	core_pvtm_gate_en PD_CORE PVTM clock disable. When HIGH, disable clock

CRU_GLB_SRST_FST_VALUE
Address: Operational Base + offset (0x0100)
The first global software reset config value

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0000	glb_srst_fst_value The first global software reset config value If config 0xfdb9, it will generate first global software reset.

CRU_GLB_SRST_SND_VALUE
Address: Operational Base + offset (0x0104)
The second global software reset config value

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0000	glb_srst_snd_value The second global software reset config value If config 0xeca8, it will generate second global software reset.

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CRU_SOFTRST0_CON

Address: Operational Base + offset (0x0110)

Internal software reset control register0

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	l2c_srstn_req L2C software reset request. When HIGH, reset relative logic
14	RW	0x0	strc_sys_asrstn_req Structure system AXI software reset request. When HIGH, reset relative logic
13	R/W SC	0x0	aclk_core_srstn_req core AXI clock software reset request. When HIGH, reset relative logic
12	RW	0x0	core_top_dbg_srstn_req CPU top debug software reset request. When HIGH, reset relative logic
11	RW	0x0	core3_dbg_srstn_req core3 CPU debug software reset request. When HIGH, reset relative logic
10	RW	0x0	core2_dbg_srstn_req core2 CPU debug software reset request. When HIGH, reset relative logic
9	RW	0x0	core1_dbg_srstn_req core1 CPU debug software reset request. When HIGH, reset relative logic
8	RW	0x0	core0_dbg_srstn_req core0 CPU debug software reset request. When HIGH, reset relative logic
7	R/W SC	0x0	core3_srstn_req core3 CPU software reset request. When HIGH, reset relative logic
6	R/W SC	0x0	core2_srstn_req core2 CPU software reset request. When HIGH, reset relative logic
5	R/W SC	0x0	core1_srstn_req core1 CPU software reset request. When HIGH, reset relative logic
4	R/W SC	0x0	core0_srstn_req core0 CPU software reset request. When HIGH, reset relative logic

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Bit	Attr	Reset Value	Description
3	R/W SC	0x0	core3_posrstn_req core3 CPU PO software reset request. When HIGH, reset relative logic
2	R/W SC	0x0	core2_posrstn_req core2 CPU PO software reset request. When HIGH, reset relative logic
1	R/W SC	0x0	core1_posrstn_req core1 CPU PO software reset request. When HIGH, reset relative logic
0	R/W SC	0x0	core0_posrstn_req core0 CPU PO software reset request. When HIGH, reset relative logic

CRU_SOFTRST1_CON

Address: Operational Base + offset (0x0114)

Internal software reset control register1

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	acodec_psrstn_req audio codec software reset request. When HIGH, reset relative logic
14	RW	0x0	eFuse_psrstn_req EFUSE APB software reset request. When HIGH, reset relative logic
13	RW	0x0	core_pvtm_srstn_req CORE PVTM software reset request. When HIGH, reset relative logic
12	RO	0x0	reserved
11	RW	0x0	func_pvtm_srstn_req func PVTM software reset request. When HIGH, reset relative logic
10	RW	0x0	gpu_pvtm_srstn_req GPU PVTM software reset request. When HIGH, reset relative logic
9	RW	0x0	i2s_8ch_srstn_req I2S 8channel software reset request. When HIGH, reset relative logic
8	RW	0x0	i2s_2ch_srstn_req I2S 2channel software reset request. When HIGH, reset relative logic

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Bit	Attr	Reset Value	Description
7	RW	0x0	peri_niu_srstn_req periph_niu software reset request. When HIGH, reset relative logic
6	RW	0x0	rom_srstn_req ROM software reset request. When HIGH, reset relative logic
5	RW	0x0	intmem_srstn_req Internal memory software reset request. When HIGH, reset relative logic
4	RW	0x0	spdif_srstn_req SPDIF software reset request. When HIGH, reset relative logic
3	RW	0x0	ahb2apb_hsrstn_req AHB2APB software reset request. When HIGH, reset relative logic
2	RW	0x0	bussys_hsrstn_req BUS AHB software reset request. When HIGH, reset relative logic
1:0	RO	0x0	reserved

CRU_SOFTRST2_CON

Address: Operational Base + offset (0x0118)

Internal software reset control register2

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	sfc_srstn_req SFC software reset request. When HIGH, reset relative logic
14	RW	0x0	i2c3_srstn_req I2C3 software reset request. When HIGH, reset relative logic
13	RW	0x0	i2c2_srstn_req I2C2 software reset request. When HIGH, reset relative logic
12	RW	0x0	i2c1_srstn_req I2C1 software reset request. When HIGH, reset relative logic
11	RW	0x0	i2c0_srstn_req I2C0 software reset request. When HIGH, reset relative logic
10	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
9	RW	0x0	uart2_srstn_req UART2 software reset request. When HIGH, reset relative logic
8	RW	0x0	uart1_srstn_req UART1 software reset request. When HIGH, reset relative logic
7	RW	0x0	uart0_srstn_req UART0 software reset request. When HIGH, reset relative logic
6:5	RO	0x0	reserved
4	RW	0x0	mipiphy_psrstn_req mipiphy apb bus software reset request. When HIGH, reset relative logic
3	RW	0x0	gpio3_srstn_req GPIO3 software reset request. When HIGH, reset relative logic
2	RW	0x0	gpio2_srstn_req GPIO2 software reset request. When HIGH, reset relative logic
1	RW	0x0	gpio1_srstn_req GPIO1 software reset request. When HIGH, reset relative logic
0	RW	0x0	gpio0_srstn_req GPIO0 software reset request. When HIGH, reset relative logic

CRU_SOFTRST3_CON

Address: Operational Base + offset (0x011c)

Internal software reset control register3

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	usb_peri_srstn_req USB PERIPH software reset request. When HIGH, reset relative logic
14	RW	0x0	emem_peri_srstn_req EMEM PERIPH software reset request. When HIGH, reset relative logic
13	RW	0x0	bus_peri_srstn_req BUS PERIPH software reset request. When HIGH, reset relative logic

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Bit	Attr	Reset Value	Description
12	RW	0x0	smart_card_srstn_req smart_card software reset request. When HIGH, reset relative logic
11	RW	0x0	periphsys_psrstn_req PERIPH APB software reset request. When HIGH, reset relative logic
10	RW	0x0	periphsys_hsrstn_req PERIPH AHB software reset request. When HIGH, reset relative logic
9	RW	0x0	periphsys_asrstn_req PERIPH AXI software reset request. When HIGH, reset relative logic
8	RW	0x0	gmac_srstn_req GMAC software reset request. When HIGH, reset relative logic
7	RW	0x0	grf_srstn_req GRF software reset request. When HIGH, reset relative logic
6	RO	0x0	reserved
5	RW	0x0	crypto_srstn_req crypto software reset request. When HIGH, reset relative logic
4	RW	0x0	dap_sys_srstn_req DAP system software reset request. When HIGH, reset relative logic
3	RW	0x0	dap_srstn_req DAP software reset request. When HIGH, reset relative logic
2	RW	0x0	dap_po_srstn_req DAP power software reset request. When HIGH, reset relative logic
1	RO	0x0	reserved
0	RW	0x0	pwm0_srstn_req PWM0 software reset request. When HIGH, reset relative logic

CRU_SOFTRST4_CON

Address: Operational Base + offset (0x0120)

Internal software reset control register4

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit

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Bit	Attr	Reset Value	Description
15	RW	0x0	ddrmsch_srstn_req DDR memory scheduler software reset request. When HIGH, reset relative logic
14:11	RO	0x0	reserved
10	RW	0x0	otgc1_srstn_req USBOTG controller1 software reset request. When HIGH, reset relative logic Host Controller utmi_clk domain reset
9	RO	0x0	reserved
8	RW	0x0	usbotg1_srstn_req USBOTG1 software reset request. When HIGH, reset relative logic Host Controller hclk domain reset.
7	RW	0x0	otgc0_srstn_req USBOTG controller0 software reset request. When HIGH, reset relative logic. OTG Controller utmi_clk domain reset.
6	RO	0x0	reserved
5	RW	0x0	usbotg0_srstn_req USBOTG0 software reset request. When HIGH, reset relative logic OTG Controller hclk domain reset.
4	RW	0x0	nandc_srstn_req NANDC software reset request. When HIGH, reset relative logic
3	RW	0x0	gps_srstn_req GPS software reset request. When HIGH, reset relative logic
2:1	RO	0x0	reserved
0	RW	0x0	dma2_srstn_req DMA2 software reset request. When HIGH, reset relative logic

CRU_SOFTRST5_CON

Address: Operational Base + offset (0x0124)

Internal software reset control register5

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RO	0x0	reserved
14	RW	0x0	usbhost0_ehci_srstn_req usbhost0_ehci clock input0 domain software reset request. When HIGH, reset relative logic

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Bit	Attr	Reset Value	Description
13	RW	0x0	tsp_clkin_srstn_req TSP clock input domain software reset request. When HIGH, reset relative logic
12	RW	0x0	tsp_srstn_req TSP software reset request. When HIGH, reset relative logic
11	RW	0x0	ddrctrl_psrstn_req DDR controller APB software reset request. When HIGH, reset relative logic
10	RW	0x0	ddrctrl_srstn_req DDR controller software reset request. When HIGH, reset relative logic
9	RW	0x0	ddrphy_psrstn_req DDR PHY APB software reset request. When HIGH, reset relative logic
8	RW	0x0	ddrphy_srstn_req DDR PHY software reset request. When HIGH, reset relative logic
7	RW	0x0	saradc_srstn_req SARADC software reset request. When HIGH, reset relative logic
6	RW	0x0	wdt_srstn_req WDT software reset request. When HIGH, reset relative logic
5	RO	0x0	reserved
4	RW	0x0	spi_srstn_req SPI software reset request. When HIGH, reset relative logic
3	RW	0x0	emmc_srstn_req EMMC software reset request. When HIGH, reset relative logic
2	RW	0x0	sdio_srstn_req SDIO software reset request. When HIGH, reset relative logic
1	RW	0x0	sdmmc_srstn_req SDMMC software reset request. When HIGH, reset relative logic
0	RO	0x0	reserved

CRU_SOFTRST6_CON
Address: Operational Base + offset (0x0128)
Internal software reset control register6

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	pmu_srstn_req PMU software reset request. When HIGH, reset relative logic
14	RW	0x0	cif_srstn_req CIF software reset request. When HIGH, reset relative logic
13	RW	0x0	rga_hsrstn_req RGA AHB software reset request. When HIGH, reset relative logic
12	RW	0x0	rga_asrstn_req RGA AXI software reset request. When HIGH, reset relative logic
11	RW	0x0	iep_hsrstn_req IEP AHB software reset request. When HIGH, reset relative logic
10	RW	0x0	iep_asrstn_req IEP AXI software reset request. When HIGH, reset relative logic
9	RW	0x0	usbpor_srst_req USBPHY POR software reset request. When HIGH, reset relative logic. USB phy analog domain reset, including both OTG and HOST phy .
8	RW	0x0	host_utmi_srst_req USBHOST UTMI software reset request. When HIGH, reset relative logic HOST phy digital domain reset. It should last at least 10 utmi_clk_1 cycles.
7	RW	0x0	otg_utmi_srstn_req USBOTG UTMI software reset request. When HIGH, reset relative logic OTG phy digital domain reset. It should last at least 10 utmi_clk_0 cycles.
6	RW	0x0	vop_dsrstn_req VOP DCLK software reset request. When HIGH, reset relative logic
5	RW	0x0	vio_hsrstn_req VIO AHB software reset request. When HIGH, reset relative logic

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Bit	Attr	Reset Value	Description
4	RW	0x0	vio0_asrstn_req VIO0 AXI software reset request. When HIGH, reset relative logic
3	RW	0x0	vio_bus_hsrstn_req VIO bus AHB software reset request. When HIGH, reset relative logic
2	RW	0x0	vio0_asrstn_req VIO 0 NIU AXI software reset request. When HIGH, reset relative logic
1	RW	0x0	vio_arbi_hsrstn_req VIO arbitor AHB software reset request. When HIGH, reset relative logic
0	RW	0x0	hdmi_psrstn_req HDMI PCLK software reset request. When HIGH, reset relative logic

CRU_SOFTRST7_CON

Address: Operational Base + offset (0x012c)

Internal software reset control register7

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:13	RO	0x0	reserved
12	RW	0x0	ebc_hsrstn_req EBC AHB software reset request. When HIGH, reset relative logic
11	RW	0x0	ebc_asrstn_req EBC AXI software reset request. When HIGH, reset relative logic
10	RW	0x0	gpu_niu_asrstn_req GPU NIU AXI software reset request. When HIGH, reset relative logic
9	RO	0x0	reserved
8	RW	0x0	gpu_srstn_req GPU core software reset request. When HIGH, reset relative logic
7	RW	0x0	vop_ssrstn_req VOP SCLK software reset request. When HIGH, reset relative logic
6	RO	0x0	reserved
5	RW	0x0	pmu_niu_psrstn_req PD_PMU NIU APB software reset request. When HIGH, reset relative logic

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Bit	Attr	Reset Value	Description
4	RW	0x0	vcodec_niu_asrstn_req VCODEC NIU AXI software reset request. When HIGH, reset relative logic
3	RW	0x0	hevc_core_srstn_req HEVC CORE software reset request. When HIGH, reset relative logic
2	RW	0x0	vio1_asrstn_req VIO second AXI software reset request. When HIGH, reset relative logic
1	RW	0x0	vcodec_hsrstn_req VCODEC AHB software reset request. When HIGH, reset relative logic
0	RW	0x0	vcodec_asrstn_req VCODEC AXI software reset request. When HIGH, reset relative logic

CRU_SOFTRST8_CON

Address: Operational Base + offset (0x0130)

Internal software reset control register8

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:10	RO	0x0	reserved
9	RW	0x0	vio_mipi_dsi_srstn_req pd_vio mipi_dsi software reset request. When HIGH, reset relative logic
8	RW	0x0	vio_h2p_srstn_req pd_vio h2p bridge software reset request. When HIGH, reset relative logic
7	RW	0x0	timer5_srstn_req Timer5 software reset request. When HIGH, reset relative logic
6	RW	0x0	timer4_srstn_req Timer4 software reset request. When HIGH, reset relative logic
5	RW	0x0	timer3_srstn_req Timer3 software reset request. When HIGH, reset relative logic
4	RW	0x0	timer2_srstn_req Timer2 software reset request. When HIGH, reset relative logic

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Bit	Attr	Reset Value	Description
3	RW	0x0	timer1_srstn_req Timer1 software reset request. When HIGH, reset relative logic
2	RW	0x0	timer0_srstn_req Timer0 software reset request. When HIGH, reset relative logic
1	RW	0x0	dbg_psrstn_req DEBUG APB software reset request. When HIGH, reset relative logic
0	RW	0x0	core_dbg_srstn_req CORE DEBUG software reset request. When HIGH, reset relative logic

CRU_MISC_CON
Address: Operational Base + offset (0x0134)
SCU control register

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x1	usb480_src_sel USB480 and 24M selection 1'b0: select 480M 1'b1: select 24M
14:11	RO	0x0	reserved
10:8	RW	0x0	testclk_sel Output clock selection for test 3'b000: clk_pvtm 3'b001: sclk_vop 3'b010: clk_core 3'b011: clk_ddrphy 3'b100: aclk_vio0 3'b101: aclk_gpu 3'b110: aclk_peri 3'b111: aclk_bus
7:1	RO	0x0	reserved
0	RW	0x0	core0_porst_wdt_sel Select reset watchdog when A7 core 0 power on reset 1'b0: not reset watchdog 1'b1: reset watchdog

CRU_GLB_CNT_TH
Address: Operational Base + offset (0x0140)
global reset wait counter threshold

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Bit	Attr	Reset Value	Description
31:16	RW	0x3a98	pll_lock_period PLL lock period configuration value
15	RW	0x0	wdt_glb_srst_ctrl watch dog trigger global soft reset select 1'b0: watch_dog trigger second global reset 1'b1: watch_dog trigger first global reset
14	RO	0x0	reserved
13:12	RW	0x0	pmu_glb_srst_ctrl watch dog trigger global soft reset select 2'b00: pmu reset by first global soft reset 2'b01: pmu reset by second global soft reset 2'b10: pmu not reset by any global soft reset
11:10	RO	0x0	reserved
9:0	RW	0x064	glb_rst_cnt_th Global soft reset counter threshold value

CRU_GLB_RST_ST
Address: Operational Base + offset (0x0150)
global reset status

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3	W1C	0x0	snd_glb_wdt_rst_st second global watch_dog rst flag 1'b0: last hot reset is not second global watch_dog triggered reset 1'b1: last hot reset is second global watch_dog triggered reset
2	W1C	0x0	fst_glb_wdt_rst_st first global watch_dog rst flag 1'b0: last hot reset is not first global watch_dog triggered reset 1'b1: last hot reset is first global watch_dog triggered reset
1	W1C	0x0	snd_glb_rst_st second global rst flag 1'b0: last hot reset is not second global rst 1'b1: last hot reset is second global rst
0	W1C	0x0	fst_glb_rst_st first global rst flag 1'b0: last hot reset is not first global rst 1'b1: last hot reset is first global rst

CRU_SDMMC_CON0
Address: Operational Base + offset (0x01c0)
sdmmc control0

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:12	RW	0x0	reserved
11	RW	0x0	sdmmc_drv_sel sdmmc drive select For detail configuration, please refer to Chapter13 Mobile storage host controller.
10:3	RW	0x00	sdmmc_drv_delaynum sdmmc drive delay number For detail configuration, please refer to Chapter13 Mobile storage host controller.
2:1	RW	0x2	sdmmc_drv_degree sdmmc drive degree For detail configuration, please refer to Chapter13 Mobile storage host controller.
0	RW	0x0	sdmmc_init_state sdmmc initial state For detail configuration, please refer to Chapter13 Mobile storage host controller.

CRU_SDMMC_CON1

Address: Operational Base + offset (0x01c4)

sdmmc control1

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:11	RW	0x0	reserved
10	RW	0x0	sdmmc_sample_sel sdmmc sample select For detail configuration, please refer to Chapter13 Mobile storage host controller.
9:2	RW	0x00	sdmmc_sample_delaynum sdmmc sample delay number For detail configuration, please refer to Chapter13 Mobile storage host controller.
1:0	RW	0x0	sdmmc_sample_degree sdmmc sample degree For detail configuration, please refer to Chapter13 Mobile storage host controller.

CRU_SDIO_CON0

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Address: Operational Base + offset (0x01c8)
sdio0 control0

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:12	RW	0x0	reserved
11	RW	0x0	sdio0_drv_sel sdio0 drive select For detail configuration, please refer to Chapter13 Mobile storage host controller.
10:3	RW	0x00	sdio0_drv_delaynum sdio0 drive delay number For detail configuration, please refer to Chapter13 Mobile storage host controller.
2:1	RW	0x2	sdio0_drv_degree sdio0 drive degree For detail configuration, please refer to Chapter13 Mobile storage host controller.
0	RW	0x0	sdio0_init_state sdio0 initial state For detail configuration, please refer to Chapter13 Mobile storage host controller.

CRU_SDIO_CON1
Address: Operational Base + offset (0x01cc)
sdio0 control1

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:11	RW	0x0	reserved
10	RW	0x0	sdio0_sample_sel sdio0 sample select For detail configuration, please refer to Chapter13 Mobile storage host controller.
9:2	RW	0x00	sdio0_sample_delaynum sdio0 sample delay number For detail configuration, please refer to Chapter13 Mobile storage host controller.
1:0	RW	0x0	sdio0_sample_degree sdio0 sample degree For detail configuration, please refer to Chapter13 Mobile storage host controller.

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CRU_EMMC_CON0
Address: Operational Base + offset (0x01d8)
emmc control0

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:12	RW	0x0	reserved
11	RW	0x0	emmc_drv_sel emmc drive select For detail configuration, please refer to Chapter13 Mobile storage host controller.
10:3	RW	0x00	emmc_drv_delaynum emmc drive delay number For detail configuration, please refer to Chapter13 Mobile storage host controller.
2:1	RW	0x2	emmc_drv_degree emmc drive degree For detail configuration, please refer to Chapter13 Mobile storage host controller.
0	RW	0x0	emmc_init_state emmc initial state For detail configuration, please refer to Chapter13 Mobile storage host controller.

CRU_EMMC_CON1
Address: Operational Base + offset (0x01dc)
emmc control1

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:11	RW	0x0	reserved
10	RW	0x0	emmc_sample_sel emmc sample select For detail configuration, please refer to Chapter13 Mobile storage host controller.
9:2	RW	0x00	emmc_sample_delaynum emmc sample delay number For detail configuration, please refer to Chapter13 Mobile storage host controller.

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Bit	Attr	Reset Value	Description
1:0	RW	0x0	emmc_sample_degree emmc sample degree For detail configuration, please refer to Chapter13 Mobile storage host controller.

CRU_PLL_PRG_EN
Address: Operational Base + offset (0x01f0)
PLL program enable

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:0	RW	0x0000	pll_prg_en pll program enable when pll_prg_en is 16'h5a5a, all the pll_con can be programed

2.8 Timing Diagram

Power on reset timing is shown as follow:

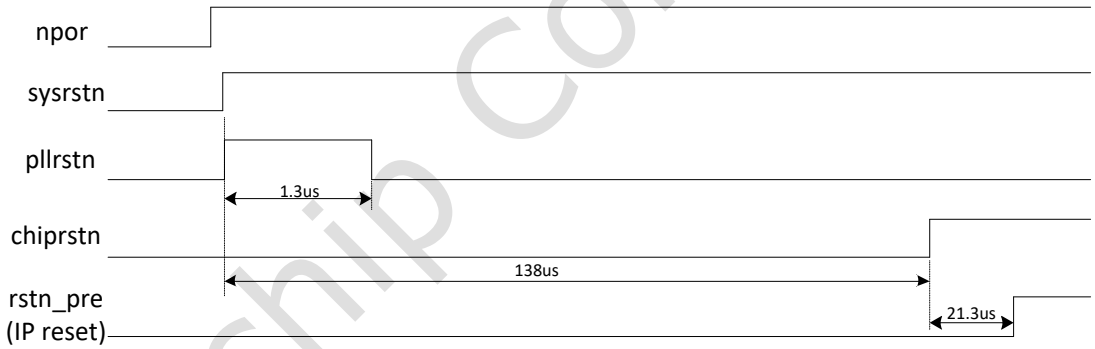


Fig. 2-8 Chip Power On Reset Timing Diagram

NPOR is hardware reset signal from out-chip, which is filtered glitch to obtain signal sysrstn. To make PLLs work normally, the PLL reset signal (pllrstn) must maintain high for more than 1us, and PLLs start to lock when pllrstn deassert, and the PLL max lock time is 1500 PLL REFCLK cycles. And then the system will wait about 138us, and then deactive reset signal chiprstn. The signal chiprstn is used to generate output clocks in CRU. After CRU start output clocks, the system waits again for 512cycles (21.3us) to deactive signal rstn_pre, which is used to generate power on reset of all IP.

2.9 Application Notes

2.9.1 PLL usage

The chip uses four PLLs (ARM PLL, DDR PLL, CODEC PLL and GENERAL PLL) for SOC clock generation.

A. PLL output frequency configuration
FBDIV, POSTDIV1, BYPASS can be configured by programming CRU_APLL_CON0, CRU_DPLL_CON0, CRU_CPLL_CON0 and CRU_GPLL_CON0.
DSMPD, REFDIV, POSTDIV2 can be configured by programming CRU_APLL_CON1, CRU_DPLL_CON1, CRU_CPLL_CON1 and CRU_GPLL_CON1.

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FRAC can be configured by programming CRU_APLL_CON2, CRU_DPLL_CON2, CRU_CPLL_CON2 and CRU_GPLL_CON2.

If DSMPD = 1 (DSM is disabled, "integer mode")
FOUTVCO = FREF / REFDIV * FBDIV
FOUTPOSTDIV = FOUTVCO / POSTDIV1 / POSTDIV2
When FREF is 24MHz, and if 700MHz FOUTPOSTDIV is needed. The configuration can be:

DSMPD = 1
REFDIV = 6
FBDIV = 175
POSTDIV1=1
POSTDIV2=1

And then
FOUTVCO = FREF / REFDIV * FBDIV = 24/6*175=700
FOUTPOSTDIV = FOUTVCO / POSTDIV1 / POSTDIV2=700/1/1=700

If DSMPD = 0 (DSM is enabled, "fractional mode")
FOUTVCO = FREF / REFDIV * (FBDIV + FRAC / 224)
FOUTPOSTDIV = FOUTVCO / POSTDIV1 / POSTDIV2
When FREF is 24MHz, and if 491.52MHz FOUTPOSTDIV is needed. The configuration can be:

DSMPD = 0
REFDIV = 1
FBDIV = 40
FRAC = 24'hf5c28f
POSTDIV1=2
POSTDIV2=1

And then
FOUTVCO = FREF / REFDIV * (FBDIV + FRAC / 224) = 24/1*(40+24'hf5c28f /224)= 983.04
FOUTPOSTDIV = FOUTVCO / POSTDIV1 / POSTDIV2=983.04/2/1=491.52

B. PLL frequency range requirement

All the value range requirements are as follow.

FREF (Input Frequency Range in Integer Mode):	1MHz to 800MHz
FREF (Input Frequency Range in Fractional Mode):	10MHz to 800MHz
FREF/ REFDIV (The divided reference frequency):	1 to 50MHz
FOUTVCO:	600MHz to 2.4GHz

C. PLL setting consideration

- If the POSTDIV value is changed during operation a short pulse (glitch) may occur on FOUTPOSTDIV. The minimum width of the short pulse will be equal to twice the period of the VCO. Therefore, if the circuitry clocked by the PLL is sensitive to short pulses, the new divide value should be re-timed so that it is synchronous with the rising edge of the output clock (FOUTPOSTDIV). Glitches cannot occur on any of the other outputs.
- For lowest power operation, the minimum VCO and FREF frequencies should be used. For minimum jitter operation, the highest VCO and FREF frequencies should be used. The normal operating range for the VCO is described above in.
- The supply rejection will be worse at the low end of the VCO range so care should be taken to keep the supply clean for low power applications.
- The feedback divider is not capable of dividing by all possible settings due to the use of a power-saving architecture. The following settings are valid for FBDIV:
  - DSMPD=1 (Integer Mode):
    12,13,14,16-4095 (practical value is limited to 3200, 2400, or 1600 (FVCOMAX / FREFMIN))
  - DSMPD=0 (Fractional Mode):
    19-4091 (practical value is limited to 320, 240, or 160 (FVCOMAX / FREFMIN))

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- The PD input places the PLL into the lowest power mode. In this case, all analog circuits are turned off and FREF will be "ignored". The FOUTPOSTDIV and FOUTVCO pins are forced to logic low (0V).
- The BYPASS pin controls a MUX which selects FREF to be passed to the FOUTPOSTDIV when active high. However, the PLL continues to run as it normally would if bypass were low. This is a useful feature for PLL testing since the clock path can be verified without the PLL being required to work. Also, the effect that the PLL induced supply noise has on the output buffering can be evaluated. It is not recommended to switch between BYPASS mode and normal mode for regular chip operation since this may result in a glitch. Also, FOUTPOSTDIVPD should be set low if the PLL is to be used in BYPASS mode.

2.9.2 PLL frequency change and lock check

The PLL programming support changed on-the-fly and the PLL will simply slew to the new frequency.
PLL lock state can be check in CRU_APLL_CON1[10], CRU_DPLL_CON1[10],CRU_CPLL_CON1[10],CRU_GPLL_CON1[10] register. The lock state is high when both original hardware PLL lock and PLL counter lock are high. The PLL counter lock initial value is CRU_GLB_CNT_TH[31:16].
The max delay time is 1500 REF_CLK.
PLL locking consists of three phases.

- Phase 1 is control voltage slewing. During this phase one of the clocks (reference or divide) is much faster than the other, and the PLL frequency adjusts almost continuously. When locking from power down, the divide clock is initially very slow and steadily increases frequency. Slew time is about 2-5s. It will take slightly longer for faster VCO settings when locking from power down, since the PLL must slew further.
- Phase 2 is small signal phase acquisition. During this phase, the internal up/down signals alternate semi-chaotically as the phase slowly adjusts until the two signals are aligned. The duration of this phase depends on the loop bandwidth and is faster with higher bandwidth. Bandwidth can be estimated as FREF / REFDIV / 20 for integer mode and FREF /REFDIV / 40 for fractional mode. The duration of small signal locking is about 1/Bandwidth.
- Phase 3 is the digital cycle count. After the last cycle slip is detected, an internal counter waits 256 FREF / REFDIV cycles before the lock signal goes high. This is frequently the dominant factor in lock time – especially for slower reference clock signals or large reference divide settings. This time can be calculated as 256*REFDIV/FREF.

2.9.3 Fractional divider usage

To get specific frequency, clocks of I2S, SPDIF and UART can be generated by fractional divider. Generally you must set that denominator is 20 times larger than numerator to generate precise clock frequency. So the fractional divider applies only to generate low frequency clock like I2S, SPDIF and UART.

2.9.4 Global software reset

Two global software resets are designed in the chip, you can program CRU_GLB_SRST_FST_VALUE[15:0] as 0xfdb9 to assert the first global software reset glb_srstn_1 and program CRU_GLB_SRST_SND_VALUE[15:0] as 0xeca8 to assert the second global software reset glb_srstn_2. These two software resets are self-deasserted by hardware.
Glb_srstn_1 resets almost all logic.
Glb_srstn_2 resets almost all logic except GRF and GPIOs.
After global reset, the reset trigger source can be check in CRU_GLB_RST_ST.

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Chapter 3 GPU

3.1 Overview

The GPU is a hardware accelerator for 2D and 3D graphics systems. Its triangle rate can be 30 Mtris/s, pixel rate can be 300Mpix/s@300MHz..
The GPU supports the following graphics standards:

- OpenGL ES 2.0
- OpenGL ES 1.1
- OpenVG 1.1

The GPU consists of:

- 2 Pixel Processors (PPs)
- 1 geometry Processor (GP)
- 1 Level2 Cache controller (L2)
- 1 Memory Management Unit (MMU) for each GP and PP included in the GPU

The GPU contains a 64-bit APB bus and a 64-bit AXI bus. CPU configures GPU through APB bus, GPU read and write data through AXI bus.

3.2 Block Diagram

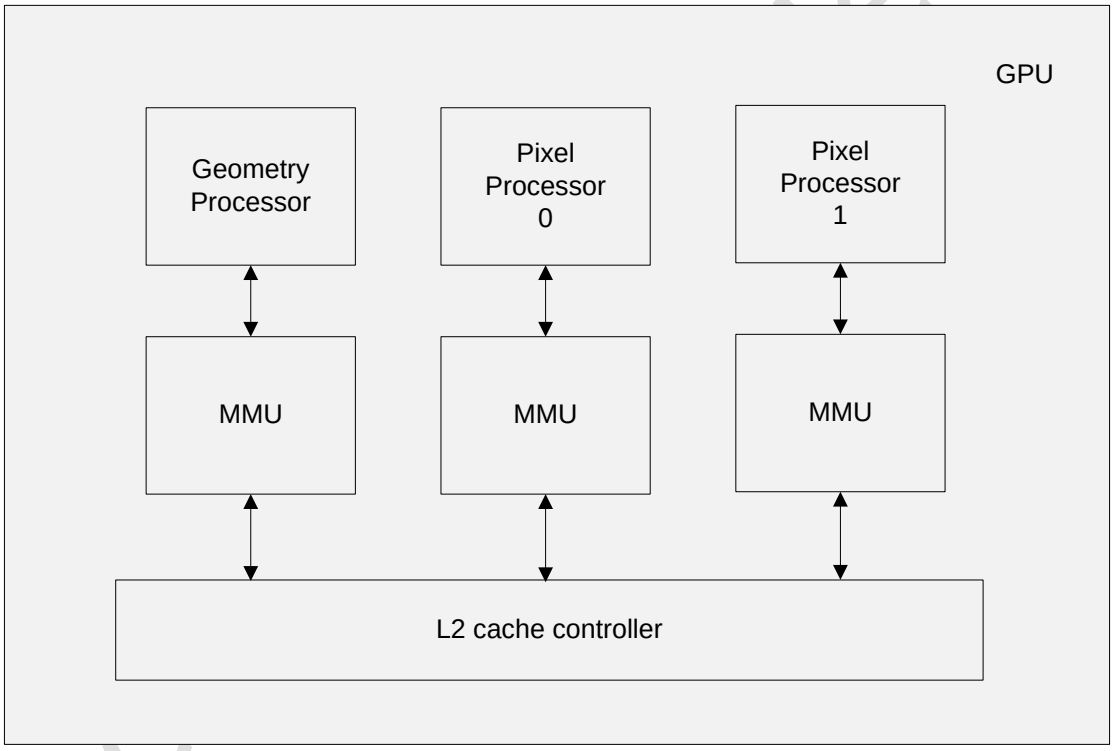


Fig. 3-1 GPU block diagram

As GPU block diagram shows, The GPU contains one geometry processor, 2 pixel processors, 3 MMU and a L2 cache controller.
The pixel processor features are:

- Each pixel processor used processes a different tile, enabling a faster turnaround.
- Programmable fragment shader
- Alpha blending
- Complete non-power-of-2 texture support
- Cube mapping
- Fast dynamic branching
- Fast trigonometric functions, including arctangent
- Full floating-point arithmetic
- Framebuffer blend with destination alpha
- Indexable texture samplers
- Line, quad, triangle and point sprites

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- No limit on program length
- Perspective correct texturing
- Point sampling, bilinear and trilinear filtering
- Programmable mipmap level-of-detail biasing and replacement
- Stencil buffering, 8-bit
- Two-sided stencil
- Unlimited dependent texture reads
- 4-level hierarchical Z and stencil operations
- Up to 512 times Full scene Anti-Aliasing (FSAA). 4x multisampling times 128x supersampling
- 4-bit per texel compressed texture format

The geometry processor features are:
- Programmable vertex shader
- Flexible input and output formats
- Autonomous operation tile list generation
- Indexed and no-indexed geometry input
- Primitive constructions with points, lines, triangles and quads

The L2 cache controller features are:
- 32KB size
- 4-way set-associative
- Supports up to 32 outstanding AXI transactions
- Implements a standard pseudo-LRU algorithm
- Cache line and line fill burst size is 64 bytes
- Support eight to 64 bytes uncached read bursts and write bursts
- 64-bit interface to memory sub-system
- Support for hit-under-miss and miss-under-miss with the only limitation of AXI ordering rules.

The MMU features are:
- Accesses control registers through the bus infrastructure to configure the memory system
- Each processor has its own MMU to control and translate memory access that the GPU initiates

3.3 Function description

Please refer to the Mali400 documents for the GPU detail description..

3.4 Register description

The GPU address range is 0x1009_0000 ~ 0x100a_0000.

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3.5 Interface description

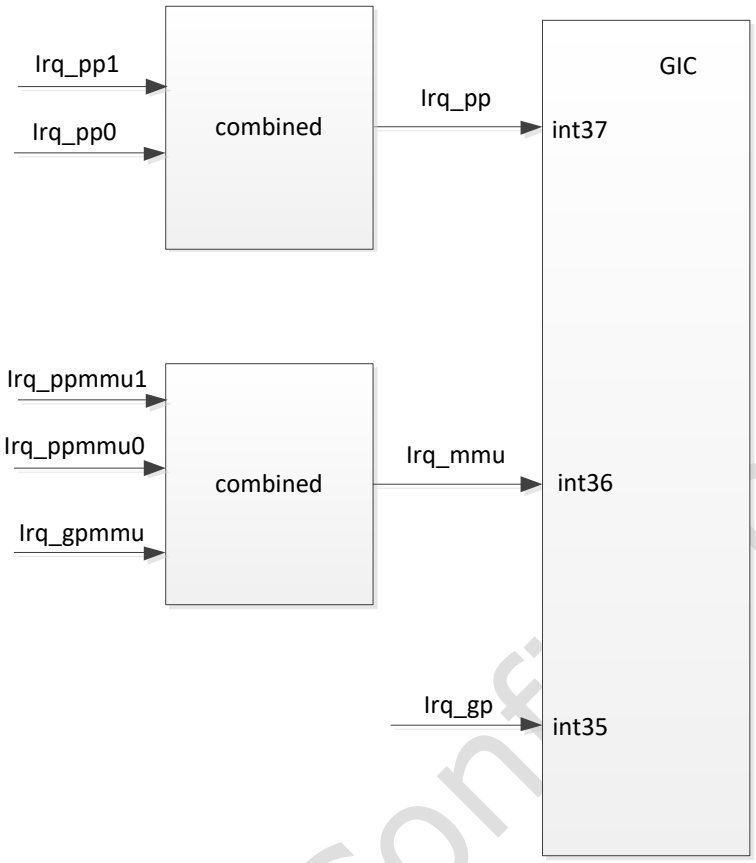


Fig. 3-2 GPU interrupt connection

The GPU now has three interrupt output. irq_ppmmu and irq_gpmmu is combined to irq_mmu.

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Chapter 4 General Register Files (GRF)

4.1 Overview

The general register files will be used to do static set by software, which is composed of many registers for system control.

4.1.1 Features

The function of general register file is:

- IOMUX control
- Control the state of GPIO in power-down mode
- GPIO PAD pull down and pull up control
- Used for common system control
- Used to record the system state

4.2 GRF Register Description

4.2.1 Register Summary

Name	Offset	Size	Reset Value	Description
GRF_GPIO0A_IOMUX	0x00a8	W	0x00000000	GPIO0A IOMUX control
GRF_GPIO0B_IOMUX	0x00ac	W	0x00000000	GPIO0B IOMUX control
GRF_GPIO0C_IOMUX	0x00b0	W	0x00000000	GPIO0C IOMUX control
GRF_GPIO0D_IOMUX	0x00b4	W	0x00000000	GPIO0D IOMUX control
GRF_GPIO1A_IOMUX	0x00b8	W	0x00000c00	GPIO1A IOMUX control
GRF_GPIO1B_IOMUX	0x00bc	W	0x00000030	GPIO1B IOMUX control
GRF_GPIO1C_IOMUX	0x00c0	W	0x00000000	GPIO1C IOMUX control
GRF_GPIO1D_IOMUX	0x00c4	W	0x00000000	GPIO1D IOMUX control
GRF_GPIO2A_IOMUX	0x00c8	W	0x00000000	GPIO2A IOMUX control
GRF_GPIO2B_IOMUX	0x00cc	W	0x00000000	GPIO2B IOMUX control
GRF_GPIO2C_IOMUX	0x00d0	W	0x00000000	GPIO2C IOMUX control
GRF_GPIO2D_IOMUX	0x00d4	W	0x00000000	GPIO2D IOMUX control
GRF_GPIO3A_IOMUX	0x00d8	W	0x00000000	GPIO3A IOMUX control
GRF_GPIO3B_IOMUX	0x00dc	W	0x00000000	GPIO3B IOMUX control
GRF_GPIO3C_IOMUX	0x00e0	W	0x00000000	GPIO3D IOMUX control
GRF_GPIO3D_IOMUX	0x00e4	W	0x00000000	GPIO3D IOMUX control
GRF_GPIO2C_IOMUX2	0x00e8	W	0x00000000	GPIO2C IOMUX control
GRF_CIF_IOMUX	0x00ec	W	0x00000000	CIF IOMUX control
GRF_CIF_IOMUX1	0x00f0	W	0x00000000	CIF IOMUX control register1
GRF_GPIO0L_PULL	0x0118	W	0x00000000	GPIO0A / GPIO0B pull up/down control
GRF_GPIO0H_PULL	0x011c	W	0x00000000	GPIO0C / GPIO0D pull up/down control
GRF_GPIO1L_PULL	0x0120	W	0x00000000	GPIO0A / GPIO0B pull up/down control
GRF_GPIO1H_PULL	0x0124	W	0x00000000	GPIO1C / GPIO1D pull up/down control
GRF_GPIO2L_PULL	0x0128	W	0x00000000	GPIO2A / GPIO2B pull up/down control

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Name	Offset	Size	Reset Value	Description
GRF_GPIO2H_PULL	0x012c	W	0x00000000	GPIO2C / GPIO2D pull up/down control
GRF_GPIO3L_PULL	0x0130	W	0x00000000	GPIO3A / GPIO3B pull up/down control
GRF_GPIO3H_PULL	0x0134	W	0x00000000	GPIO3C / GPIO3D pull up/down control
GRF_ACODEC_CON	0x013c	W	0x00000020	SoC control register
GRF_SOC_CON0	0x0140	W	0x00000120	SoC control register
GRF_SOC_CON1	0x0144	W	0x00000000	SoC control register
GRF_SOC_CON2	0x0148	W	0x00000084	SoC control register
GRF_SOC_STATUS0	0x014c	W	0x00000000	SoC status register
GRF_LVDS_CON0	0x0150	W	0x00000000	LVDS control register
GRF_DMAC_CON0	0x015c	W	0x00000000	DMAC control register
GRF_DMAC_CON1	0x0160	W	0x00000000	DMAC control register
GRF_DMAC_CON2	0x0164	W	0x00000010	DMAC control register
GRF_MAC_CON0	0x0168	W	0x00000810	GMAC control register0
GRF_MAC_CON1	0x016c	W	0x00004040	GMAC control register1
GRF_TVE_CON	0x0170	W	0x00000000	TV encoder control register
GRF_UOC0_CON0	0x017c	W	0x00000000	OTG control register
GRF_UOC1_CON1	0x0184	W	0x00000000	usb host control register
GRF_UOC1_CON2	0x0188	W	0x0000c820	UOC1 control register 2
GRF_UOC1_CON3	0x018c	W	0x00000b40	UOC1 control register 3
GRF_UOC1_CON4	0x0190	W	0x0000001c	USB HOST 2.0 control register
GRF_UOC1_CON5	0x0194	W	0x00000000	USB HOST 2.0 control register
GRF_DDRC_STAT	0x019c	W	0x00000000	DDRC status
GRF_SOC_STATUS1	0x01a4	W	0x00000000	SoC status register
GRF_CPU_CON0	0x01a8	W	0x00002002	CPU control register
GRF_CPU_CON1	0x01ac	W	0x00000000	CPU control register
GRF_CPU_CON2	0x01b0	W	0x0000003f	CPU control register
GRF_CPU_CON3	0x01b4	W	0x00002aaa	CPU control register
GRF_CPU_STATUS0	0x01c0	W	0x00000000	CPU status register
GRF_CPU_STATUS1	0x01c4	W	0x00000000	CPU status register
GRF_OS_REG0	0x01c8	W	0x00000000	software OS register
GRF_OS_REG1	0x01cc	W	0x00000000	software OS register
GRF_OS_REG2	0x01d0	W	0x00000000	software OS register
GRF_OS_REG3	0x01d4	W	0x00000000	software OS register
GRF_OS_REG4	0x01d8	W	0x00000000	software OS register
GRF_OS_REG5	0x01dc	W	0x00000000	software OS register
GRF_OS_REG6	0x01e0	W	0x00000000	software OS register
GRF_OS_REG7	0x01e4	W	0x00000000	software OS register
GRF_PVTM_CON0	0x0200	W	0x00000000	PVTM control register
GRF_PVTM_CON1	0x0204	W	0x00000000	PVTM control register
GRF_PVTM_CON2	0x0208	W	0x00000000	PVTM control register

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Name	Offset	Size	Reset Value	Description
GRF_PVTM_CON3	0x020c	W	0x00000000	PVTM control register
GRF_PVTM_STATUS0	0x0210	W	0x00000000	PVTM status register0
GRF_PVTM_STATUS1	0x0214	W	0x00000000	PVTM status register1
GRF_PVTM_STATUS2	0x0218	W	0x00000000	PVTM status register2
GRF_PVTM_STATUS3	0x021c	W	0x00000000	PVTM status register3
GRF_DFI_WRNUM	0x0220	W	0x00000000	DFI write number register
GRF_DFI_RDNUM	0x0224	W	0x00000000	DFI read number register
GRF_DFI_ACTNUM	0x0228	W	0x00000000	DFI active number register
GRF_DFI_TIMERVAL	0x022c	W	0x00000000	DFI work time
GRF_NIF_FIFO0	0x0230	W	0x00000000	NIF status register
GRF_NIF_FIFO1	0x0234	W	0x00000000	NIF status register
GRF_NIF_FIFO2	0x0238	W	0x00000000	NIF status register
GRF_NIF_FIFO3	0x023c	W	0x00000000	NIF status register
GRF_USBPHY0_CON0	0x0280	W	0x00008618	usbphy control register
GRF_USBPHY0_CON1	0x0284	W	0x0000e007	usbphy control register
GRF_USBPHY0_CON2	0x0288	W	0x000082aa	usbphy control register
GRF_USBPHY0_CON3	0x028c	W	0x00000200	usbphy control register
GRF_USBPHY0_CON4	0x0290	W	0x00000002	usbphy control register
GRF_USBPHY0_CON5	0x0294	W	0x00000000	usbphy control register
GRF_USBPHY0_CON6	0x0298	W	0x00000004	usbphy control register
GRF_USBPHY0_CON7	0x029c	W	0x000068c0	usbphy control register
GRF_USBPHY1_CON0	0x02a0	W	0x00008618	usbphy control register
GRF_USBPHY1_CON1	0x02a4	W	0x0000e007	usbphy control register
GRF_USBPHY1_CON2	0x02a8	W	0x000082aa	usbphy control register
GRF_USBPHY1_CON3	0x02ac	W	0x00000200	usbphy control register
GRF_USBPHY1_CON4	0x02b0	W	0x00000002	usbphy control register
GRF_USBPHY1_CON5	0x02b4	W	0x00000000	usbphy control register
GRF_USBPHY1_CON6	0x02b8	W	0x00000004	usbphy control register
GRF_USBPHY1_CON7	0x02bc	W	0x000068c0	usbphy control register
GRF_UOC_STATUS0	0x02c0	W	0x00000000	SoC status register 0
GRF_CHIP_TAG	0x0300	W	0x00003112	chip tag register
GRF_MMC_DET_CNT	0x0304	W	0x0000fdb9	mmc0 detect filter counter register
GRF_EFUSE_PRG_EN	0x037c	W	0x00000000	eFuse program register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

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4.2.2 Detail Register Description

GRF_GPIO0A_IOMUX
Address: Operational Base + offset (0x000a8)
GPIO0A IOMUX control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:14	RW	0x0	gpio0a7_sel GPIO0A[7] IOMUX select 2'b10: hdmi_ddcsda, HDMI ddcsda signal 2'b01: i2c3_sda, I2C sda data signal 2'b00: GPIO, general purpose IO
13:12	RW	0x0	gpio0a6_sel GPIO0A[6] IOMUX select 2'b10: hdmi_ddcscl, HDMI ddcscl signal 2'b01: i2c3_scl, I2C scl clock signal 2'b00: GPIO, general purpose IO
11:8	RO	0x0	reserved
7:6	RW	0x0	gpio0a3_sel GPIO0A[3] IOMUX select 2'b01: i2c1_sda, I2C sda data signal 2'b10: sdio_cmd, SDIO command signal 2'b00: GPIO, general purpose IO
5	RO	0x0	reserved
4	RW	0x0	gpio0a2_sel GPIO0A[2] IOMUX select 1'b1: i2c1_scl, I2C scl clock signal 1'b0: GPIO, general purpose IO
3	RO	0x0	reserved
2	RW	0x0	gpio0a1_sel GPIO0A[1] IOMUX select 1'b1: i2c0_sda, I2C sda data signal 1'b0: GPIO, general purpose IO
1	RO	0x0	reserved
0	RW	0x0	gpio0a0_sel GPIO0A[0] IOMUX select 1'b1: i2c0_scl, I2C scl clock signal 1'b0: GPIO, general purpose IO

GRF_GPIO0B_IOMUX
Address: Operational Base + offset (0x000ac)
GPIO0B IOMUX control

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:14	RW	0x0	gpio0b7_sel GPIO0B[7] IOMUX select 2'b01: hdmi_hotplugin, HDMI hotplug in signal. 2'b00: GPIO, general purpose IO
13:12	RW	0x0	gpio0b6_sel GPIO0B[6] IOMUX select 2'b01: i2s_sdi_mux0, I2S data_in signal for IOMUX mode0 2'b10: spi_csn0_mux2, SPI chip select signal for IOMUX mode2 2'b00: GPIO, general purpose IO
11:10	RW	0x0	gpio0b5_sel GPIO0B[5] IOMUX select 2'b01: i2s_sdo_mux0, I2S data_out signal for IOMUX mode0 2'b10: spi_rxd_mux2, SPI RX data signal for IOMUX mode2 2'b00: GPIO, general purpose IO
9	RO	0x0	reserved
8	RW	0x0	gpio0b4_sel GPIO0B[4] IOMUX select 1'b1: i2s_lrcktx_mux0, I2S TX lack signal for IOMUX mode0 1'b0: GPIO, general purpose IO
7:6	RW	0x0	gpio0b3_sel GPIO0B[3] IOMUX select 2'b01: i2s_lrckrx_mux0, I2S RX lack signal for IOMUX mode0 2'b10: spi_txd_mux2, SPI TX data signal for IOMUX mode2 2'b00: GPIO, general purpose IO
5:4	RO	0x0	reserved
3:2	RW	0x0	gpio0b1_sel GPIO0B[1] IOMUX select 2'b01: i2s_sclk_mux0, I2S SCLK signal for IOMUX mode0 2'b10: spi_clk_mux2, SPI clock signal for IOMUX mode2 2'b00: GPIO, general purpose IO
1	RO	0x0	reserved
0	RW	0x0	gpio0b0_sel GPIO0B[0] IOMUX select 1'b1: i2s_mclk_mux0, I2S MCLK signal for IOMUX mode0 1'b0: GPIO, general purpose IO

GRF_GPIO0C_IOMUX
Address: Operational Base + offset (0x000b0)
GPIO0C IOMUX control

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RO	0x0	reserved
14	RW	0x0	gpio0c7_sel GPIO0C[7] IOMUX select 1'b1: nand_cs1, NAND chip select signal 1'b0: GPIO, general purpose IO
13:9	RO	0x0	reserved
8	RW	0x0	gpio0c4_sel GPIO0C[4] IOMUX select 1'b11: hdmi_cecsda, HDMI cec sda signal. 1'b10: GPIO, general purpose IO
7:4	RO	0x0	reserved
3:2	RW	0x0	gpio0c1_sel GPIO0C[1] IOMUX select 2'b10: uart0_rstn, UART reset signal 2'b01: sc_io, sim card IO signal 2'b00: GPIO, general purpose IO
1:0	RO	0x0	reserved

GRF_GPIO0D_IOMUX
Address: Operational Base + offset (0x000b4)
GPIO0D IOMUX control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:13	RO	0x0	reserved
12	RW	0x0	gpio0d6_sel GPIO0D[6] IOMUX select 1'b1: sdio_power, SDIO power enable signal 1'b0: GPIO, general purpose IO
11:9	RO	0x0	reserved
8	RW	0x0	gpio0d4_sel GPIO0D[4] IOMUX select 1'b1: pwm_2, PWM channel 2 1'b0: GPIO, general purpose IO
7	RO	0x0	reserved
6	RW	0x0	gpio0d3_sel GPIO0D[3] IOMUX select 1'b1: pwm_1, PWM channel 1 1'b0: GPIO, general purpose IO

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Bit	Attr	Reset Value	Description
5	RO	0x0	reserved
4	RW	0x0	gpio0d2_sel GPIO0D[2] IOMUX select 1'b1: pwm_0, PWM channel 0 1'b0: GPIO, general purpose IO
3	RO	0x0	reserved
2	RW	0x0	gpio0d1_sel GPIO0D[1] IOMUX select 1'b1: uart2_ctsn, UART CTS signal 1'b0: GPIO, general purpose IO
1:0	RW	0x0	gpio0d0_sel GPIO0D[0] IOMUX select 2'b01: uart2_rtsn, UART RTS signal 2'b10: pmic_sleep_mux0, PMIC sleep control for IOMUX mode0 2'b00: GPIO, general purpose IO

GRF_GPIO1A_IOMUX
Address: Operational Base + offset (0x000b8)
GPIO1A IOMUX control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RO	0x0	reserved
14	RW	0x0	gpio1a7_sel GPIO1A[7] IOMUX select 1'b1: sdmmc_wrprt, SDMMC write protect signal 1'b0: GPIO, general purpose IO
13:12	RO	0x0	reserved
11:10	RW	0x3	gpio1a5_sel GPIO1A[5] IOMUX select 2'b01: i2s_sdi_mux1, I2S data-in signal for IOMUX mode1 2'b10: sdio_data3, SDIO data signal 2'b00: GPIO, general purpose IO
9:8	RW	0x0	gpio1a4_sel GPIO1A[4] IOMUX select 2'b01: i2s_sdo_mux1, I2S data-out signal for IOMUX mode1 2'b10: sdio_data2, SDIO data signal 2'b00: GPIO, general purpose IO
7	RO	0x0	reserved
6	RW	0x0	gpio1a3_sel GPIO1A[3] IOMUX select 1'b1: i2s_lrcktx_mux1, I2S TX LRCK signal for IOMUX mode1 1'b0: GPIO, general purpose IO

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Bit	Attr	Reset Value	Description
5:4	RW	0x0	gpio1a2_sel GPIO1A[2] IOMUX select 2'b01: i2s_lrckrx_mux1, I2S RX LRCK signal for IOMUX mode1 2'b10: sdio_data1, SDIO data signal 2'b00: GPIO, general purpose IO
3:2	RW	0x0	gpio1a1_sel GPIO1A [1] IOMUX select 2'b01: i2s_sclk_mux1, I2S SCLK signal for IOMUX mode1 2'b10: sdio_data0, SDIO data signal 2'b11: pmic_sleep_mux1, PMIC sleep control for IOMUX mode1 2'b00: GPIO, general purpose IO
1:0	RW	0x0	gpio1a0_sel GPIO1A[0] IOMUX select 2'b01: i2s_mclk_mux1, I2S MCLK signal for IOMUX mode1 2'b10: sdio_clkout, SDIO clock-out signal 2'b11: xin32k, input 32KHz signal 2'b00: GPIO, general purpose IO

GRF_GPIO1B_IOMUX
Address: Operational Base + offset (0x000bc)
GPIO1B IOMUX control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RO	0x0	reserved
14	RW	0x0	gpio1b7_sel GPIO1B [7] IOMUX select 1'b1: sdmmc_cmd, SDMMC command signal 1'b0: GPIO, general purpose IO
13	RO	0x0	reserved
12	RW	0x0	gpio1b6_sel GPIO1B [6] IOMUX select 1'b1: sdmmc_pwren, SDMMC power enable signal 1'b0: GPIO, general purpose IO
11:9	RO	0x0	reserved
8	RW	0x0	gpio1b4_sel GPIO1B [4] IOMUX select 1'b1: spi_csn1_mux0, SPI chip select signal for IOMUX mode0 1'b0: GPIO, general purpose IO

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Bit	Attr	Reset Value	Description
7:6	RW	0x0	gpio1b3_sel GPIO1B [3] IOMUX select 2'b01: spi_csn0_mux0, SPI chip select signal for IOMUX mode0 2'b10: uart1_rtsn, UART RTS signal 2'b00: GPIO, general purpose IO
5:4	RW	0x3	gpio1b2_sel GPIO1B [2] IOMUX select 2'b01: spi_rxd_mux0, SPI RX data signal for IOMUX mode0 2'b10: uart1_sin, UART data-in signal 2'b00: GPIO, general purpose IO
3:2	RW	0x0	gpio1b1_sel GPIO1B [1] IOMUX select 2'b01: spi_txd_mux0, SPI TX data signal for IOMUX mode0 2'b10: uart1_sout, UART data-out signal 2'b00: GPIO, general purpose IO
1:0	RW	0x0	gpio1b0_sel GPIO1B[0] IOMUX select 2'b01: spi_clk_mux0, SPI clock signal for IOMUX mode0 2'b10: uart1_ctsn, UART CTS signal 2'b00: GPIO, general purpose IO

GRF_GPIO1C_IOMUX
Address: Operational Base + offset (0x000c0)
GPIO1C IOMUX control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:14	RW	0x0	gpio1c7_sel GPIO1C[7] IOMUX select 2'b01: nand_cs3, NAND chip select signal 2'b10: emmc_rstnout, eMMC reset signal 2'b00: GPIO, general purpose IO
13:12	RW	0x0	gpio1c6_sel GPIO1C[6] IOMUX select 2'b01: nand_cs2, NAND chip select signal 2'b10: emmc_cmd_mux0, eMMC command signal for IOMUX mode0 2'b00: GPIO, general purpose IO
11:10	RW	0x0	gpio1c5_sel GPIO1C[5] IOMUX select 2'b10: jtag_tms when sdmmc0_detectn is invalid 2'b01: sdmmc_d3, SDMMC data signal 2'b00: GPIO, general purpose IO

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Bit	Attr	Reset Value	Description
9:8	RW	0x0	gpio1c4_sel GPIO1C[4] IOMUX select 2'b10: jtag_tck when sdmmc0_detectn is invalid 2'b01: sdmmc_d2, SDMMC data signal 2'b00: GPIO, general purpose IO
7:6	RW	0x0	gpio1c3_sel GPIO1C[3] IOMUX select 2'b01: sdmmc_d1, SDMMC data signal 2'b10: uart2_rx, UART RX signal 2'b00: GPIO, general purpose IO
5:4	RW	0x0	gpio0c2_sel GPIO0C[2] IOMUX select 2'b01: sdmmc_d0, SDMMC data signal 2'b10: uart2_tx, UART TX signal 2'b00: GPIO, general purpose IO
3	RO	0x0	reserved
2	RW	0x0	gpio1c1_sel GPIO1C[1] IOMUX select 1'b1: sdmmc_detn, SDMMC detect signal 1'b0: GPIO, general purpose IO
1	RO	0x0	reserved
0	RW	0x0	gpio1c0_sel GPIO1C[0] IOMUX select 1'b1: sdmmc_clkout, SDMMC clock-out signal 1'b0: GPIO, general purpose IO

GRF_GPIO1D_IOMUX
Address: Operational Base + offset (0x000c4)
GPIO1D IOMUX control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:14	RW	0x0	gpio1d7_sel GPIO1D[7] IOMUX select 2'b01: nand_d7, NAND data signal 2'b10: emmc_d7, eMMC data signal 2'b11: spi_csn1_mux1, SPI chip select signal for IOMUX mode1 2'b00: GPIO, general purpose IO

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Bit	Attr	Reset Value	Description
13:12	RW	0x0	gpio1d6_sel GPIO1D[6] IOMUX select 2'b01: nand_d6, NAND data signal 2'b10: emmc_d6, eMMC data signal 2'b11: spi_csn0_mux1, SPI chip select signal for IOMUX mode1 2'b00: GPIO, general purpose IO
11:10	RW	0x0	gpio1d5_sel GPIO1D[5] IOMUX select 2'b01: nand_d5, NAND data signal 2'b10: emmc_d5, eMMC data signal 2'b11: spi_txd1_mux1, SPI TX data signal for IOMUX mode1 2'b00: GPIO, general purpose IO
9:8	RW	0x0	gpio1d4_sel GPIO1D[4] IOMUX select 2'b01: nand_d4, NAND data signal 2'b10: emmc_d4, eMMC data signal 2'b11: spi_rxd1_mux1, SPI RX data signal for IOMUX mode1 2'b00: GPIO, general purpose IO
7:6	RW	0x0	gpio1d3_sel GPIO1D[3] IOMUX select 2'b11: sfc_d3, SFC data signal 2'b10: emmc_d3, eMMC data signal 2'b01: nand_d3, NAND data signal 2'b00: GPIO, general purpose IO
5:4	RW	0x0	gpio1d2_sel GPIO1D[2] IOMUX select 2'b11: sfc_d2, SFC data signal 2'b10: emmc_d2, eMMC data signal 2'b01: nand_d2, NAND data signal 2'b00: GPIO, general purpose IO
3:2	RW	0x0	gpio1d1_sel GPIO1D[1] IOMUX select 2'b11: sfc_d1, SFC data signal 2'b10: emmc_d1, eMMC data signal 2'b01: nand_d1, NAND data signal 2'b00: GPIO, general purpose IO
1:0	RW	0x0	gpio1d0_sel GPIO1D[0] IOMUX select 2'b11: sfc_d0, SFC data signal 2'b10: emmc_d0, eMMC data signal 2'b01: nand_d0, NAND data signal 2'b00: GPIO, general purpose IO

GRF_GPIO2A_IOMUX
Address: Operational Base + offset (0x000c8)

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GPIO2A IOMUX control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:14	RW	0x0	gpio2a7_sel GPIO2A[7] IOMUX select 2'b01: nand_dqs, NAND DQS signal 2'b10: emmc_clkout, eMMC clock out signal 2'b00: GPIO, general purpose IO
13	RO	0x0	reserved
12	RW	0x0	gpio2a6_sel GPIO2A[6] IOMUX select 1'b1: nand_cs0, NAND chip select signal 1'b0: GPIO, general purpose IO
11:10	RW	0x0	gpio2a5_sel GPIO2A[5] IOMUX select 2'b01: nand_wp, NAND write protect signal 2'b10: emmc_pwren, eMMC power enable signal 2'b00: GPIO, general purpose IO
9:8	RW	0x0	gpio2a4_sel GPIO2A[4] IOMUX select 2'b11: sfc_clk, SFC clock signal 2'b01: nand_rdy, NAND ready signal 2'b10: emmc_cmd_mux1, eMMC command signal for IOMUX mode1 2'b00: GPIO, general purpose IO
7:6	RW	0x0	gpio2a3_sel GPIO2A[3] IOMUX select 2'b10: sfc_csn1, SFC CS signal 2'b01: nand_rdn, NAND read enable signal 2'b00: GPIO, general purpose IO
5:4	RW	0x0	gpio2a2_sel GPIO2A[2] IOMUX select 2'b10: sfc_csn0, SFC CS signal 2'b01: nand_wrn, NAND write enable signal 2'b00: GPIO, general purpose IO
3:2	RW	0x0	gpio2a1_sel GPIO2A[1] IOMUX select 2'b01: nand_cle, NAND command latch enable signal 2'b00: GPIO, general purpose IO
1:0	RW	0x0	gpio2a0_sel GPIO2A[0] IOMUX select 2'b01: nand_ale, NAND address latch enable signal 2'b10: spi_clk_mux1, SPI clock signal for IOMUX mode1 2'b00: GPIO, general purpose IO

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GRF_GPIO2B_IOMUX
Address: Operational Base + offset (0x000cc)
GPIO2B IOMUX control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:14	RW	0x0	gpio2b7_sel GPIO2B[7] IOMUX select 2'b11: gmac_rxer, GMAC rxer signal 2'b10: ebc_sdce5, EBC sdce signal 2'b01: vop_d13, VOP data signal 2'b00: GPIO, general purpose IO
13:12	RW	0x0	gpio2b6_sel GPIO2B[6] IOMUX select 2'b11: gmac_clk, GMAC clk signal 2'b10: ebc_sdce4, EBC sdce signal 2'b01: vop_d12, VOP data signal 2'b00: GPIO, general purpose IO
11:10	RW	0x0	gpio2b5_sel GPIO2B[5] IOMUX select 2'b11: gmac_txen, GMAC txen signal 2'b10: ebc_sdce3, EBC sdce signal 2'b01: vop_d11, VOP data signal 2'b00: GPIO, general purpose IO
9:8	RW	0x0	gpio2b4_sel GPIO2B[4] IOMUX select 2'b11: gmac_mdio, GMAC mdio signal 2'b10: ebc_sdce2, EBC sdce signal 2'b01: vop_d10, VOP data signal 2'b00: GPIO, general purpose IO
7:6	RW	0x0	gpio2b3_sel GPIO2B[3] IOMUX select 2'b11: gmac_rxclk, GMAC rx clk signal 2'b10: ebc_gdclk, EBC gdclk signal 2'b01: vop_den, VOP data enable signal 2'b00: GPIO, general purpose IO
5:4	RW	0x0	gpio2b2_sel GPIO2B[2] IOMUX select 2'b11: gmac_crs, GMAC crs signal 2'b10: ebc_sdoe, EBC sdoe signal 2'b01: vop_vsync, VOP vertical sync signal 2'b00: GPIO, general purpose IO

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Bit	Attr	Reset Value	Description
3:2	RW	0x0	gpio2b1_sel GPIO2B[1] IOMUX select 2'b11: gmac_txclk, GMAC tx clk signal 2'b10: ebc_sdle, EBC sdle signal 2'b01: vop_hsync, VOP horizontal sync signal 2'b00: GPIO, general purpose IO
1:0	RW	0x0	gpio2b0_sel GPIO2B[0] IOMUX select 2'b11: gmac_rxdv, GMAC rxdv signal 2'b10: ebc_sdclk, EBC sdclk signal 2'b01: vop_dclk, VOP display clock signal 2'b00: GPIO, general purpose IO

GRF_GPIO2C_IOMUX
Address: Operational Base + offset (0x000d0)
GPIO2C IOMUX control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:8	RO	0x0	reserved
7:6	RW	0x0	gpio2c3_sel GPIO2C[3] IOMUX select 2'b11: gmac_txd0, GMAC tx data signal 2'b10: ebc_pdpwr0, EBC pdpwr0 signal 2'b01: vop_d17, VOP data signal 2'b00: GPIO, general purpose IO
5:4	RW	0x0	gpio2c2_sel GPIO2C[2] IOMUX select 2'b11: gmac_txd1, GMAC tx data signal 2'b10: ebc_gdsp, EBC gdsp signal 2'b01: vop_d16, VOP data signal 2'b00: GPIO, general purpose IO
3:2	RW	0x0	gpio2c1_sel GPIO2C[1] IOMUX select 2'b11: gmac_rxd0, GMAC rx data signal 2'b10: ebc_gdoe, EBC gdoe signal 2'b01: vop_d15, VOP data signal 2'b00: GPIO, general purpose IO

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Bit	Attr	Reset Value	Description
1:0	RW	0x0	gpio2c0_sel GPIO2C[0] IOMUX select 2'b11: gmac_rxd1, GMAC rx data signal 2'b10: ebc_vcom, EBC vcom signal 2'b01: vop_d14, VOP data signal 2'b00: GPIO, general purpose IO

GRF_GPIO2D_IOMUX
Address: Operational Base + offset (0x000d4)
GPIO2D IOMUX control

31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RO	0x0	reserved
14:12	RW	0x0	gpio2d0_sel GPIO2D[0] IOMUX select 3'b100: gmac_col, GMAC col signal 3'b011: gps_clk, GPS clock signal 3'b010: ebc_gdpwr1, EBC gdpwr1 signal 3'b001: vop_d22, VOP data signal 3'b000: GPIO, general purpose IO
11:10	RW	0x0	gpio2d5_sel GPIO2D[5] IOMUX select 2'b10: uart0_ctsn, UART CTS signal 2'b01: sc_det, sim card detect signal 2'b00: GPIO, general purpose IO
9:8	RO	0x0	reserved
7:6	RW	0x0	gpio2d3_sel GPIO2D[3] IOMUX select 2'b10: uart0_sin, UART data-in signal 2'b01: sc_clk, sim card clock signal 2'b00: GPIO, general purpose IO
5:4	RW	0x0	gpio2d2_sel GPIO2D[2] IOMUX select 2'b10: uart0_sout, UART data-out signal 2'b01: sc_rst, sim card reset signal 2'b00: GPIO, general purpose IO
3:2	RW	0x0	gpio2d1_sel GPIO2D[1] IOMUX select 2'b11: gmac_mdc, GMAC mdc signal 2'b10: ebc_gdpwr2, EBC gdpwr2 signal 2'b01: vop_d23, VOP data signal 2'b00: GPIO, general purpose IO
1:0	RO	0x0	reserved

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GRF_GPIO3B_IOMUX
Address: Operational Base + offset (0x000dc)
GPIO3B IOMUX control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:7	RO	0x0	reserved
6	RW	0x0	gpio3b3_sel GPIO3B[3] IOMUX select 1'b1: testclk_out, internal clock output for probe 1'b0: GPIO, general purpose IO
5:0	RO	0x0	reserved

GRF_GPIO3C_IOMUX
Address: Operational Base + offset (0x000e0)
GPIO3D IOMUX control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:4	RO	0x0	reserved
3:2	RW	0x0	gpio3c1_sel GPIO3C[1] IOMUX select 2'b01: otg_drvvbus, OTG drive VBUS signal 2'b10: pmic_sleep_mux2, PMIC sleep control for IOMUX mode2 2'b00: GPIO, general purpose IO
1:0	RO	0x0	reserved

GRF_GPIO3D_IOMUX
Address: Operational Base + offset (0x000e4)
GPIO3D IOMUX control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RO	0x0	reserved
14	RW	0x0	gpio3d7_sel GPIO3D[7] IOMUX select 1'b1: testclk_out, internal clock output for probe 1'b0: GPIO, general purpose IO
13:7	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
6	RW	0x0	gpio3d3_sel GPIO3D[3] IOMUX select 1'b1: spdif_tx, SPDIF tx signal 1'b0: GPIO, general purpose IO
5	RO	0x0	reserved
4	RW	0x0	gpio3d2_sel GPIO3D[2] IOMUX select 1'b1: pwm_irin, PWM channel for infrared radiation input 1'b0: GPIO, general purpose IO
3:0	RO	0x0	reserved

GRF_GPIO2C_IOMUX2
Address: Operational Base + offset (0x000e8)
GPIO2C IOMUX control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RO	0x0	reserved
14:12	RW	0x0	gpio2c7_sel GPIO2C[7] IOMUX select 3'b100: gmac_txd3, GMAC tx data signal 3'b011: gps_mag, GPS mag signal 3'b010: ebc_border1, EBC border1 signal 3'b001: vop_d21, VOP data signal 3'b000: GPIO, general purpose IO
11	RO	0x0	reserved
10:8	RW	0x0	gpio2c6_sel GPIO2C[6] IOMUX select 3'b100: gmac_txd2, GMAC tx data signal 3'b011: gps_sign, GPS sign signal 3'b010: ebc_border0, EBC border0 signal 3'b001: vop_d20, VOP data signal 3'b000: GPIO, general purpose IO
7	RO	0x0	reserved
6:4	RW	0x0	gpio2c5_sel GPIO2C[5] IOMUX select 3'b100: gmac_rxd2, GMAC rx data signal 3'b011: i2c2_scl, I2C clock signal 3'b010: ebc_sdshr, EBC sdshr signal 3'b001: vop_d19, VOP data signal 3'b000: GPIO, general purpose IO
3	RO	0x0	Reserved

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Bit	Attr	Reset Value	Description
2:0	RW	0x0	gpio2c4_sel GPIO2C[4] IOMUX select 3'b100: gmac_rxd3, GMAC rx data signal 3'b011: i2c2_sda, I2C data signal 3'b010: ebc_gdrl, EBC gdrl signal 3'b001: vop_d18, VOP data signal 3'b000: GPIO, general purpose IO

GRF_CIF_IOMUX
Address: Operational Base + offset (0x00ec)
CIF IOMUX control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RO	0x0	reserved
14	RW	0x0	cifd7_sel cif_d7 IOMUX select 1'b1: ts_d7 1'b0: cif_d7
13	RO	0x0	reserved
12	RW	0x0	cifd6_sel cif_d6 IOMUX select 1'b1: ts_d6 1'b0: cif_d6
11	RO	0x0	reserved
10	RW	0x0	cifd5_sel cif_d5 IOMUX select 1'b1: ts_d5 1'b0: cif_d5
9	RO	0x0	reserved
8	RW	0x0	cifd4_sel cif_4 IOMUX select 1'b1: ts_d4 1'b0: cif_d4
7	RO	0x0	reserved
6	RW	0x0	cifd3_sel cif_d3 IOMUX select 1'b1: ts_d3 1'b0: cif_d3
5	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
4	RW	0x0	cifd2_sel cif_d2 IOMUX select 1'b1: ts_d2 1'b0: cif_d2
3	RO	0x0	reserved
2	RW	0x0	cifd1_sel cif_d1 IOMUX select 1'b1: ts_d1 1'b0: cif_d1
1	RO	0x0	reserved
0	RW	0x0	cifd0_sel cif_d0 IOMUX select 1'b1: ts_d0 1'b0: cif_d0

GRF_CIF_IOMUX1
Address: Operational Base + offset (0x00f0)
CIF IOMUX control register1

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:7	RO	0x0	reserved
6	RW	0x0	cif_clkout_sel cif_clkout IOMUX select 1'b1: ts_clk 1'b0: cif_clkout
5	RO	0x0	reserved
4	RW	0x0	cif_clkin_sel cif_clkin IOMUX select 1'b1: ts_valid 1'b0: cif_clkin
3	RO	0x0	reserved
2	RW	0x0	cif_href_sel cif_href IOMUX select 1'b1: ts_error 1'b0: cif_href
1	RO	0x0	reserved
0	RW	0x0	cif_vsync_sel cif_vsync IOMUX select 1'b1: ts_sync 1'b0: cif_vsync

GRF_GPIO0L_PULL

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Address: Operational Base + offset (0x00118)
GPIO0A / GPIO0B pull up/down control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:8	RW	0x00	gpio0b_pull GPIO0B pull up/down enable Values written to this register independently control Pullup/Pulldown or not for the corresponding data bit in GPIO. 1'b0: pull up/down enable, PAD type will decide to be up or down, not related with this value 1'b1: pull up/down disable bit8 - GPIO0B[0] pull up/down control bit9 - GPIO0B[1] pull up/down control bit10 - GPIO0B[2] pull up/down control ... bit15 - GPIO0B[7] pull up/down control
7:0	RW	0x00	gpio0a_pull GPIO0A pull up/down enable Values written to this register independently control Pullup/Pulldown or not for the corresponding data bit in GPIO. 1'b0: pull up/down enable, PAD type will decide to be up or down, not related with this value 1'b1: pull up/down disable bit0 - GPIO0A[0] pull up/down control bit1 - GPIO0A[1] pull up/down control bit2 - GPIO0A[2] pull up/down control ... bit7 - GPIO0A[7] pull up/down control

GRF_GPIO0H_PULL
Address: Operational Base + offset (0x0011c)
GPIO0C / GPIO0D pull up/down control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit

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Bit	Attr	Reset Value	Description
15:8	RW	0x00	gpio0d_pull GPIO0D pull up/down enable Values written to this register independently control Pullup/Pulldown or not for the corresponding data bit in GPIO. 1'b0: pull up/down enable, PAD type will decide to be up or down, not related with this value 1'b1: pull up/down disable bit8 - GPIO0D[0] pull up/down control bit9 - GPIO0D[1] pull up/down control bit10 - GPIO0D[2] pull up/down control ... bit15 - GPIO0D[7] pull up/down control
7:0	RW	0x00	gpio0c_pull GPIO0C pull up/down enable Values written to this register independently control Pullup/Pulldown or not for the corresponding data bit in GPIO. 1'b0: pull up/down enable, PAD type will decide to be up or down, not related with this value 1'b1: pull up/down disable bit0 - GPIO0C[0] pull up/down control bit1 - GPIO0C[1] pull up/down control bit2 - GPIO0C[2] pull up/down control ... bit7 - GPIO0C[7] pull up/down control

GRF_GPIO1L_PULL
Address: Operational Base + offset (0x00120)
GPIO0A / GPIO0B pull up/down control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:8	RW	0x00	gpio1b_pull GPIO1B pull up/down enable Values written to this register independently control Pullup/Pulldown or not for the corresponding data bit in GPIO. 1'b0: pull up/down enable, PAD type will decide to be up or down, not related with this value 1'b1: pull up/down disable bit8 - GPIO1B[0] pull up/down control bit9 - GPIO1B[1] pull up/down control bit10 - GPIO1B[2] pull up/down control ... bit15 - GPIO1B[7] pull up/down control

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	gpio1a_pull GPIO1A pull up/down enable Values written to this register independently control Pullup/Pulldown or not for the corresponding data bit in GPIO. 1'b0: pull up/down enable, PAD type will decide to be up or down, not related with this value 1'b1: pull up/down disable bit0 - GPIO1A[0] pull up/down control bit1 - GPIO1A[1] pull up/down control bit2 - GPIO1A[2] pull up/down control ... bit7 - GPIO1A[7] pull up/down control

GRF_GPIO1H_PULL
Address: Operational Base + offset (0x00124)
GPIO1C / GPIO1D pull up/down control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:8	RW	0x00	gpio1d_pull GPIO1d pull up/down enable Values written to this register independently control Pullup/Pulldown or not for the corresponding data bit in GPIO. 1'b0: pull up/down enable, PAD type will decide to be up or down, not related with this value 1'b1: pull up/down disable bit8 - GPIO1D[0] pull up/down control bit9 - GPIO1D[1] pull up/down control bit10 - GPIO1D[2] pull up/down control ... bit15 - GPIO1D[7] pull up/down control
7:0	RW	0x00	gpio1c_pull GPIO1C pull up/down enable Values written to this register independently control Pullup/Pulldown or not for the corresponding data bit in GPIO. 1'b0: pull up/down enable, PAD type will decide to be up or down, not related with this value 1'b1: pull up/down disable bit0 - GPIO1C[0] pull up/down control bit1 - GPIO1C[1] pull up/down control bit2 - GPIO1C[2] pull up/down control ... bit7 - GPIO1C[7] pull up/down control

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GRF_GPIO2L_PULL
Address: Operational Base + offset (0x00128)
GPIO2A / GPIO2B pull up/down control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:8	RW	0x00	gpio2b_pull GPIO2B pull up/down enable Values written to this register independently control Pullup/Pulldown or not for the corresponding data bit in GPIO. 1'b0: pull up/down enable, PAD type will decide to be up or down, not related with this value 1'b1: pull up/down disable bit8 - GPIO2B[0] pull up/down control bit9 - GPIO2B[1] pull up/down control bit10 - GPIO2B[2] pull up/down control ... bit15 - GPIO2B[7] pull up/down control
7:0	RW	0x00	gpio2a_pull GPIO2A pull up/down enable Values written to this register independently control Pullup/Pulldown or not for the corresponding data bit in GPIO. 1'b0: pull up/down enable, PAD type will decide to be up or down, not related with this value 1'b1: pull up/down disable bit0 - GPIO2A[0] pull up/down control bit1 - GPIO2A[1] pull up/down control bit2 - GPIO2A[2] pull up/down control ... bit7 - GPIO2A[7] pull up/down control

GRF_GPIO2H_PULL
Address: Operational Base + offset (0x0012c)
GPIO2C / GPIO2D pull up/down control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit

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Bit	Attr	Reset Value	Description
15:8	RW	0x00	gpio2d_pull GPIO2d pull up/down enable Values written to this register independently control Pullup/Pulldown or not for the corresponding data bit in GPIO. 1'b0: pull up/down enable, PAD type will decide to be up or down, not related with this value 1'b1: pull up/down disable bit8 - GPIO2D[0] pull up/down control bit9 - GPIO2D[1] pull up/down control bit10 - GPIO2D[2] pull up/down control ... bit15 - GPIO2D[7] pull up/down control
7:0	RW	0x00	gpio2c_pull GPIO2C pull up/down enable Values written to this register independently control Pullup/Pulldown or not for the corresponding data bit in GPIO. 1'b0: pull up/down enable, PAD type will decide to be up or down, not related with this value 1'b1: pull up/down disable bit0 - GPIO2C[0] pull up/down control bit1 - GPIO2C[1] pull up/down control bit2 - GPIO2C[2] pull up/down control ... bit7 - GPIO2C[7] pull up/down control

GRF_GPIO3L_PULL
Address: Operational Base + offset (0x00130)
GPIO3A / GPIO3B pull up/down control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:8	RW	0x00	gpio3b_pull GPIO3B pull up/down enable Values written to this register independently control Pullup/Pulldown or not for the corresponding data bit in GPIO. 1'b0: pull up/down enable, PAD type will decide to be up or down, not related with this value 1'b1: pull up/down disable bit8 - GPIO3B[0] pull up/down control bit9 - GPIO3B[1] pull up/down control bit10 - GPIO3B[2] pull up/down control ... bit15 - GPIO3B[7] pull up/down control

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	gpio3a_pull GPIO3A pull up/down enable Values written to this register independently control Pullup/Pulldown or not for the corresponding data bit in GPIO. 1'b0: pull up/down enable, PAD type will decide to be up or down, not related with this value 1'b1: pull up/down disable bit0 - GPIO3A[0] pull up/down control bit1 - GPIO3A[1] pull up/down control bit2 - GPIO3A[2] pull up/down control ... bit7 - GPIO3A[7] pull up/down control

GRF_GPIO3H_PULL
Address: Operational Base + offset (0x00134)
GPIO3C / GPIO3D pull up/down control

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:8	RW	0x00	gpio3d_pull GPIO3d pull up/down enable Values written to this register independently control Pullup/Pulldown or not for the corresponding data bit in GPIO. 1'b0: pull up/down enable, PAD type will decide to be up or down, not related with this value 1'b1: pull up/down disable bit8 - GPIO3D[0] pull up/down control bit9 - GPIO3D[1] pull up/down control bit10 - GPIO3D[2] pull up/down control ... bit15 - GPIO3D[7] pull up/down control
7:0	RW	0x00	gpio3c_pull GPIO3C pull up/down enable Values written to this register independently control Pullup/Pulldown or not for the corresponding data bit in GPIO. 1'b0: pull up/down enable, PAD type will decide to be up or down, not related with this value 1'b1: pull up/down disable bit0 - GPIO3C[0] pull up/down control bit1 - GPIO3C[1] pull up/down control bit2 - GPIO3C[2] pull up/down control ... bit7 - GPIO3C[7] pull up/down control

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GRF_ACODEC_CON
Address: Operational Base + offset (0x0013c)
SoC control register

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:6	RO	0x0	reserved
5:4	RW	0x0	acodec_detectn_debounce_sel acodec_detectn debounce time select 2'b00: 5ms 2'b01: 15ms 2'b10: 35ms 2'b11: 50ms
3	RW	0x0	acodec_detectn_fall_int_en acodec detectn negedge interrupt enable 1'b0: interrupt disable 1'b1: interrupt enable
2	RW	0x0	acodec_detectn_rise_int_en acodec detectn posedge interrupt enable 1'b0: interrupt disable 1'b1: interrupt enable
1	RW	0x0	acodec_detectn_fall_int_pd acodec detectn negedge interrupt pending bit Wirte 1 to it, it will be cleared.
0	RW	0x0	acodec_detectn_rise_int_pd acodec detectn posedge interrupt pending bit Wirte 1 to it, it will be cleared.

GRF_SOC_CON0
Address: Operational Base + offset (0x00140)
SoC control register

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	hdmiphy_dclk_sel 1'b0: dclk from lcdc 1'b1: dclk from cru
14	RW	0x0	ddr_8bit_en When 8bit DDR is used, this bit should be 1.
13	RW	0x0	msch4_mainpartialpop 1'b0: 16bit DDR 1'b1: 8bit DDR

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Bit	Attr	Reset Value	Description
12	RW	0x0	soc_remap remap bit control When soc_remap = 1, the Boot ROM is mapped to address 0x10100000 and internal memory is mapped to address 0x0.
11	RW	0x0	acodec_ad2da_loop acodec loopback enable 1'b0: acodec loopback disable 1'b1: acodec loopback enable
10	RW	0x0	i2s_acodec_sel ACODEC use internal i2s interface enable 1'b0: acodec not use internal i2s interface 1'b1: acodec use internal i2s interface
9	RO	0x0	reserved
8	RW	0x1	force_jtag This bit is used to force IOMUX to jtag. 1'b0: disable 1'b1: enable
7	RW	0x0	mobile_ddr_sel This bit is used to tell DDR monitor the type of DDR used. 1'b0: DDR2/DDR3 1'b1: LPDDR2/LPDDR3
6	RW	0x0	dfi_eff_stat_en DFI monitor start to work. 1'b1: DFI monitor works. 1'b0: DFI monitor stops.
5:4	RW	0x2	sd_detectn_debounce_sel sd_detectn debounce time select 2'b00: 5ms 2'b01: 15ms 2'b10: 35ms 2'b11: 50ms
3	RW	0x0	sd_detectn_fall_int_en SD detectn negedge interrupt enable 1'b0: interrupt disable 1'b1: interrupt enable
2	RW	0x0	sd_detectn_rise_int_en SD detectn posedge interrupt enable 1'b0: interrupt disable 1'b1: interrupt enable
1	RW	0x0	sd_detectn_fall_int_pd SD detectn negedge interrupt pending bit Wirte 1 to it, it will be cleared.
0	RW	0x0	sd_detectn_rise_int_pd SD detectn posedge interrupt pending bit Wirte 1 to it, it will be cleared.

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GRF_SOC_CON1
Address: Operational Base + offset (0x00144)
SoC control register

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	hevc_vpu_sel hevc vpu select 1'b0: select vpu 1'b1: select hevc
14	RW	0x0	mipi_phy_lane3_enable MIPI PHY enalbe lane3 in TTL mode 1'b0: not TTL mode 1'b1: TTL mode
13	RW	0x0	mipi_phy_lane2_enable MIPI PHY enalbe lane2 in TTL mode 1'b0: not TTL mode 1'b1: TTL mode
12	RW	0x0	mipi_lane1_enable MIPI PHY enalbe lane1 in TTL mode 1'b0: not TTL mode 1'b1: TTL mode
11	RW	0x0	mipi_phy_lane0_enable MIPI PHY enalbe lane0 in TTL mode 1'b0: not TTL mode 1'b1: TTL mode
10	RW	0x0	vpu_sel VDPU and VEPU clock select 1'b0: select VEPU aclk as VPU main clock 1'b1: select VDPU aclk as VPU main clock
9:8	RO	0x0	reserved
7	RW	0x0	mipi_phy_enableck MIPI PHY enalbe ck in TTL mode 1'b0: not TTL mode 1'b1: TTL mode
6	RW	0x0	emmc_IOMUX_sel EMMC IOMUX select 1'b0: select EMMC IOMUX mode0 1'b1: select EMMC IOMUX mode1
5	RW	0x0	i2s_IOMUX_sel I2S IOMUX select 1'b0: select I2S IOMUX mode0 1'b1: select I2S IOMUX mode1

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Bit	Attr	Reset Value	Description
4:3	RW	0x0	spi_IOMUX_sel SPI IOMUX select 2'b00: select SPI IOMUX mode0 2'b01: select SPI IOMUX mode1 2'b10: select SPI IOMUX mode2
2:0	RW	0x3	reserved

GRF_SOC_CON2
Address: Operational Base + offset (0x00148)
SoC control register

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	crypto_pwr_idlereq NOC idle request, high valid.
14	RW	0x0	msch_pwr_idlereq MSCH idle request, active high.
13	RW	0x0	core_pwr_idlereq CORE idle request, active high.
12	RW	0x0	peri_pwr_idlereq PERI idle request, active high.
11	RW	0x0	vio_pwr_idlereq VIO idle request, active high.
10	RW	0x0	vpu_pwr_idlereq VPU idle request, active high.
9	RW	0x0	gpu_pwr_idlereq GPU idle request, active high.
8	RW	0x0	sys_pwr_idlereq SYS idle request, active high.
7	RW	0x1	msch4_mainddr3 When DDR3 is used, software should configure this bit to 1.
6:4	RO	0x0	reserved
3	RW	0x0	usb_host_sel usb host select 1'b0: select ehci usb host 1'b1: select old usb host
2	RW	0x1	ddrphy_low_power_en ddrphy low power enable 1'b0: ddrphy into low-power 1'b1: normal

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Bit	Attr	Reset Value	Description
1	RW	0x0	upctl_c_sysreq Software configure enter DDR self-refresh by low power interface. 1'b1: request enter self-refresh 1'b0: not enter self-refresh
0	RW	0x0	upctl_c_active_in DDR clock active in. External signal from system that flags if a hardware low power request can be accepted or should always be denied. 1’b0: may be accepted 1’b1: will be denied

GRF_SOC_STATUS0
Address: Operational Base + offset (0x0014c)
SoC status register

Bit	Attr	Reset Value	Description
31	RO	0x0	acodec_hpdet The flag indicates whether the headset is inserted. 1’b1: having headset to be inserted. 1’b0: don't have.
30	RO	0x0	reserved
29	RO	0x0	crypto_pwr_idle NOC idle state. "1" indicates idle.
28	RO	0x0	msch_pwr_idle MSCH idle state. "1" indicates idle.
27	RO	0x0	sys_pwr_idle SYS idle state. "1" indicates idle.
26	RO	0x0	gpu_pwr_idle GPU idle state. "1" indicates idle.
25	RO	0x0	vpu_pwr_idle VPU idle state. "1" indicates idle.
24	RO	0x0	vio_pwr_idle VIO idle state. "1" indicates idle.
23	RO	0x0	peri_pwr_idle PERI idle state. "1" indicates idle.
22	RO	0x0	core_pwr_idle CORE idle state. "1" indicates idle.
21	RO	0x0	crypto_pwr_idleack NOC idle acknowledge. high valid.
20	RO	0x0	msch_pwr_idleack MSCH idle acknowledge, active high.
19	RO	0x0	sys_pwr_idleack SYS idle acknowledge, active high.
18	RO	0x0	gpu_pwr_idleack GPU idle acknowledge, active high.

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Bit	Attr	Reset Value	Description
17	RO	0x0	vpu_pwr_idleack VPU idle acknowledge, active high.
16	RO	0x0	vio_pwr_idleack VIO idle acknowledge, active high.
15	RO	0x0	peri_pwr_idleack PERI idle acknowledge, active high.
14	RO	0x0	core_pwr_idleack CORE idle acknowledge, active high.
13	RO	0x0	host20_iddig Host2.0 iddig state. It will always be "0".
12:11	RO	0x0	host20_linestate USB Host 2.0 linestate status This bus reflects the state of the single-ended receivers. In Suspend or Sleep mode, this bus is a combinatorial output (directly reflecting the current state of D- and D+, respectively). 2'b11: SE1 (D+ high, D- high) 2'b10: K state for high-speed and full-speed USB traffic; J state for low-speed USB traffic (D+ low, D- high) 2'b01: J state for high-speed and full-speed USB traffic; K state for low-speed USB traffic (D+ high, D- low) 2'b00: SE0 (D+ low, D- low) During normal high-speed packet transfers, the line indicates a high-speed J state.
10	RO	0x0	host20_bvalid USB Host 2.0 bvalid status B-Device Session Valid Indicator Function: This controller signal is output from the USB 2.0 Session Valid comparator and indicates whether the session for a B-device is valid. 1’b1: The session for the B-device is valid. 1’b0: The session for the B-device is not valid.
9	RO	0x0	host20_vbusvalid USB Host 2.0 VBUS valid status VBUS Valid Indicator Function: This controller signal is output from the USB 2.0 VBUS Valid Comparator and indicates whether the VBUS output is at a valid level. 1’b1: The VBUS output is valid. 1’b0: The VBUS output is not valid.
8	RO	0x0	otg0_iddig USB OTG iddig status 1’b0: indicate OTG work as host 1’b1: indicate OTG work as device

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Bit	Attr	Reset Value	Description
7:6	RO	0x0	otg_linestate USB OTG linestate status This bus reflects the state of the single-ended receivers. In Suspend or Sleep mode, this bus is a combinatorial output (directly reflecting the current state of D- and D+, respectively). 2'b11: SE1 (D+ high, D- high) 2'b10: K state for high-speed and full-speed USB traffic; J state for low-speed USB traffic (D+ low, D- high) 2'b01: J state for high-speed and full-speed USB traffic; K state for low-speed USB traffic (D+ high, D- low) 2'b00: SE0 (D+ low, D- low) During normal high-speed packet transfers, the line indicates a high-speed J state.
5	RO	0x0	otg_bvalid USB OTG bvalid status B-Device Session Valid Indicator Function: This controller signal is output from the USB 2.0 Session Valid comparator and indicates whether the session for a B-device is valid. 1'b1: The session for the B-device is valid. 1'b0: The session for the B-device is not valid.
4	RO	0x0	otg_vbusvalid USB OTG VBUS valid status VBUS Valid Indicator Function: This controller signal is output from the USB 2.0 VBUS Valid Comparator and indicates whether the VBUS output is at a valid level. 1'b1: The VBUS output is valid. 1'b0: The VBUS output is not valid.
3:0	RO	0x0	pll_lock PLL lock status: generalpll_lock, codecpll_lock, armpll_lock, ddrpll_lock 1'b1: PLL is lock 1'b0: PLL is unlock

GRF_LVDS_CON0

Address: Operational Base + offset (0x00150)

LVDS control register

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:14	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
13	RW	0x0	mipi_phy_lane3_forcexmode MIPI PHY lane3 force x mode 1'b0: disable 1'b1: enable
12	RW	0x0	mipi_phy_lane2_forcexmode MIPI PHY lane2 force x mode 1'b0: disable 1'b1: enable
11	RW	0x0	mipi_phy_lane1_forcexmode MIPI PHY lane1 force x mode 1'b0: disable 1'b1: enable
10	RW	0x0	mipi_phy_lane0_forcexmode MIPI PHY lane0 force x mode 1'b0: disable 1'b1: enable
9	RW	0x0	mipi_dsi_forcexmode MIPI PHY force x mode 1'b0: disable 1'b1: enable
8	RW	0x0	mipi_phy_lane0_turndisable MIPI PHY lane0 turndisable
7	RW	0x0	mipi_phy_ttl_mode MIPI PHY work in TTL mode 1'b0: disable 1'b1: enable
6	RW	0x0	lvds_mode work in LVDS mode 1'b0: disable 1'b1: enable
5	RW	0x0	mipi_ctrl_dpicoloorm MIPI controller dpi coloorm 1'b0: disable 1'b1: enable
4	RW	0x0	mipi_ctrl_dpishutdown MIPI controller dpi shut down 1'b0: disable 1'b1: enable
3	RW	0x0	lvds_msbsel LVDS lane input format 1'b0: MSB is on D0 1'b1: MSB is on D7

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Bit	Attr	Reset Value	Description
2:1	RW	0x0	lvds_select LVDS output format 2'b00: 8bit mode format-1 2'b01: 8bit mode format-2 2'b10: 8bit mode format-3 2'b11: 6bit mode
0	RW	0x0	ebc_mac_sel LVDS data from ebc or mac or lvds selection 1'b0 : lvds 1'b1 : ebc

GRF_DMAC_CON0
Address: Operational Base + offset (0x0015c)
DMAC control register

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:1	RO	0x0	reserved
0	RW	0x0	dmac_boot_from_pc DMAC boot_from_pc input control Controls the location in which the DMAC executes its initial instruction, after it exits from reset: 1'b0: DMAC waits for an instruction from APB interface 1'b1: DMAC manager thread executes the instruction that is located at the address that boot_addr[31:0] provided.

GRF_DMAC_CON1
Address: Operational Base + offset (0x00160)
DMAC control register

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:0	RW	0x0000	dmac_boot_addr dmac_boot_addr[27:12] DMAC boot_addr[27:12] input control Configures the address location that contains the first instruction the DMAC executes, when it exits from reset.

GRF_DMAC_CON2
Address: Operational Base + offset (0x00164)
DMAC control register

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:6	RO	0x0	reserved
5:4	RW	0x1	dmac_drtype DMAC type of acknowledgement or request for peripheral signals: 2'b00: single level request 2'b01: burst level request 2'b10: acknowledging a flush request 2'b11: reserved
3:0	RW	0x0	dmac_boot_addr dmac_boot_addr[31:28] DMAC boot_addr[31:28] input control Configures the address location that contains the first instruction the DMAC executes, when it exits from reset.

GRF_MAC_CON0
Address: Operational Base + offset (0x0168)
GMAC control register0

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	rxclk_dly_ena_gmac RGMII RX clock delayline enable 1'b1: enable 1'b0: disable
14	RW	0x0	txclk_dly_ena_gmac RGMII TX clock delayline enable 1'b1: enable 1'b0: disable
13:7	RW	0x10	clk_rx_dl_cfg_gmac RGMII RX clock delayline value
6:0	RW	0x10	clk_tx_dl_cfg_gmac RGMII TX clock delayline value

GRF_MAC_CON1
Address: Operational Base + offset (0x016c)
GMAC control register1

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RO	0x0	reserved
14	RW	0x1	rmii_mode RMII mode selection 1'b1: RMII mode
13:12	RW	0x0	gmac_clk_sel RGMII clock selection 2'b00: 125MHz 2'b11: 25MHz 2'b10: 2.5MHz
11	RW	0x0	rmii_clk_sel RMII clock selection 1'b1: 25MHz 1'b0: 2.5MHz
10	RW	0x0	gmac_speed MAC speed 1'b1: 100-Mbps 1'b0: 10-Mbps
9	RW	0x0	gmac_flowctrl GMAC transmit flow control When set high, instructs the GMAC to transmit PAUSE Control frames in Full-duplex mode. In Half-duplex mode, the GMAC enables the Back-pressure function until this signal is made low again
8:6	RW	0x1	gmac_phy_intf_sel PHY interface select 3'b001: RGMII 3'b100: RMII All others: Reserved
5:0	RO	0x0	reserved

GRF_TVE_CON
Address: Operational Base + offset (0x0170)
TV encoder control register

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:13	RO	0x0	reserved
12:7	RW	0x00	gain value

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Bit	Attr	Reset Value	Description
6	RW	0x0	enctr2 config value
5	RW	0x0	enctr1 config value
4	RW	0x0	enctr0 config value
3	RW	0x0	ensc0 config value
2	RW	0x0	endac config value
1	RW	0x0	envbg config value
0	RW	0x0	enextref config value

GRF_UOC0_CON0
Address: Operational Base + offset (0x0017c)
OTG control register

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	otg0_bvalid_irq_pd otg0 bvalid interrupt pending bit Write 1 to this bit, it will be cleared.
14	RW	0x0	otg0_bvalid_irq_en otg0 bvalid interrupt enable 1'b1: interrupt enable 1'b0: interrupt disable
13	RW	0x0	otg0_linestate_irq_pd otg0 linestate interrupt pending Write 1 to this bit, it will be cleared.
12	RW	0x0	otg0_linestate_irq_en otg0 linestate change interrupt enable 1'b1: interrupt enable 1'b0: interrupt disable
11	RO	0x0	reserved
10	RW	0x0	iddig_status control software iddig value 1'b0: host 1'b1: device
9	RW	0x0	iddig_sft_sel 1'b0: iddig to otg controller select USBPHY output 1'b1: iddig to otg controller select grf_uoc0_con5[10]
8	RW	0x0	utmi_dmpulldown 1'b0: DM 15 KOhm pull down disabled 1'b1: DM 15 KOhm pull down enable
7	RW	0x0	utmi_dppulldown 1'b0: DP 15 KOhm pull down disabled 1'b1: DP 15 KOhm pull down enable

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Bit	Attr	Reset Value	Description
6	RW	0x0	utmi_termselect USB Termination Select 1'b1: Full-speed terminations are enabled. 1'b0: High-speed terminations are enabled.
5:4	RW	0x0	utmi_xcvrselect Transceiver Select 2'b11: Sends an LS packet on an FS bus or receives an LS packet. 2'b10: LS Transceiver 2'b01: FS Transceiver 2'b00: HS Transceiver
3:2	RW	0x0	utmi_opmode UTMI+ Operational Mode Function: This controller bus selects the UTMI+ operational mode. 2'b11: Normal operation without SYNC or EOP generation. If the XCVRSEL bus is not set to 2'b00 while OPMODE[1:0] is set to 2'b11, USB PHYbehavior is undefined. 2'b10: Disable bit stuffing and NRZI encoding 2'b01: Non-Driving 2'b00: Normal
1	RW	0x0	utmi_suspend_n Suspend Assertion 1'b1: Normal operating mode 1'b0: Suspend mode
0	RW	0x0	usbphy_soft_con_sel 1'b0: software control USB PHY disable 1'b1: software control USB PHY enable

GRF_UOC1_CON1
Address: Operational Base + offset (0x00184)
usb host control register

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:13	RO	0x0	reserved
12	RW	0x0	usbphy1_vdm_src_en open dm voltage source, active high
11	RW	0x0	usbphy1_vdp_src_en open dp voltage source, active high
10	RW	0x0	usbphy1_rdm_pdwn_en open dm pull down resistor, active high

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Bit	Attr	Reset Value	Description
9	RW	0x0	usbphy1_idp_src_en open dp source current, active high
8	RW	0x0	usbphy1_idm_sink_en open dm sink current enable, active high
7	RW	0x0	usbphy1_idp_sink_en open dp sink current enable, active high
6:0	RO	0x0	reserved

GRF_UOC1_CON2
Address: Operational Base + offset (0x00188)
UOC1 control register 2

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x1	usbhost0_incr4_en USB HOST0 incr4_en bit control, active high
14	RW	0x1	usbhost0_incr16_en USB HOST0 incr16_en bit control
13	RW	0x0	usbhost0_hubsetup_min USB HOST0 hubsetup_min bit control
12	RW	0x0	usbhost0_app_start_clk USB HOST0 app_start_clk bit control
11:6	RW	0x20	usbhost0_fladj_val_common USB HOST0 fladj_val_common bit control
5:0	RW	0x20	usbhost0_fladj USB HOST0 fladj bit control

GRF_UOC1_CON3
Address: Operational Base + offset (0x0018c)
UOC1 control register 3

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	usbhost0_ohci_susp_lgcy USB HOST0 ohci_susp_lgcy bit control
14	RW	0x0	usbhost0_ohci_cntsel USB HOST0 ohci_cntsel bit control
13	RW	0x0	usbhost0_app_prt_ovrcur USB HOST0 app_prt_ovrcur bit control
12	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
11	RW	0x1	usbhost0_word_if USB HOST0 word_if bit control
10	RW	0x0	usbhost0_sim_mode USB HOST0 sim_mode bit control
9	RW	0x1	usbhost0_incrx_en USB HOST0 incrx_en bit control, active high
8	RW	0x1	usbhost0_incr8_en USB HOST0 incr8_en bit control, active high
7	RO	0x0	reserved
6	RW	0x1	usbhost0_ohci_clkcktrst USB HOST0 ohci_clkcktrst bit conrol
5:1	RO	0x0	reserved
0	RW	0x0	usbhost0_autoppd_on_overcur USB HOST0 autoppd_on_overcur bit control

GRF_UOC1_CON4
Address: Operational Base + offset (0x00190)
USB HOST 2.0 control register

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	usbphy_commonon USBPHY common on
14	RO	0x0	reserved
13	RW	0x0	bypasssel0 Transmitter Digital Bypass mode Enable. When 1, OTG used as a UART port.
12	RW	0x0	bypassdmen0 DM0 Transmitter Digital Bypass Enable, active high.
11	RW	0x0	host20disable When 1, HOST 2.0 PHY disable.
10	RW	0x0	otgphydisable When 1, OTGPHY is disabled.
9:8	RW	0x0	otg_scaledown_mode USBOTG scale down mode bit control.
7:6	RW	0x0	host_scaledown_mode USBHOST scale down mode bit control.
5	RW	0x0	utmiotg_idpullup Analog ID Input Sample Enable Function: This controller signal controls ID line sampling. 1'b1: ID pin sampling is enabled, and the IDDIG output is valid. 1'b0: ID pin sampling is disabled, and the IDDIG output is not valid.

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Bit	Attr	Reset Value	Description
4	RW	0x1	utmiotg_dppulldown D+ Pull-Down Resistor Enable
3	RW	0x1	utmiotg_dmpulldown D- Pull-Down Resistor Enable
2	RW	0x1	utmiotg_drvvbus Drive VBUS 1'b1: The VBUS Valid comparator is enabled. 1'b0: The VBUS Valid comparator is disabled.
1	RW	0x0	utmisrp_chrgvbus VBUS Input Charge Enable
0	RW	0x0	utmisrp_dischrgvbus VBUS Input Discharge Enable

GRF_UOC1_CON5
Address: Operational Base + offset (0x00194)
USB HOST 2.0 control register

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	otg1_linestate_irq_pd otg1 linestate interrupt pending Write 1 to this bit, it will be cleared.
14	RW	0x0	otg1_linestate_irq_en otg1 linestate interrupt enable
13:9	RO	0x0	reserved
8	RW	0x0	utmi_dmpulldown 1'b0: DM 15 KOhm pull down disabled 1'b1: DM 15 KOhm pull down enable
7	RW	0x0	utmi_dppulldown 1'b0: DP 15 KOhm pull down disabled 1'b1: DP 15 KOhm pull down enable
6	RW	0x0	utmi_termselect USB Termination Select 1'b1: Full-speed terminations are enabled. 1'b0: High-speed terminations are enabled.
5:4	RW	0x0	utmi_xcvrselect Transceiver Select 2'b11: Sends an LS packet on an FS bus or receives an LS packet. 2'b10: LS Transceiver 2'b01: FS Transceiver 2'b00: HS Transceiver

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Bit	Attr	Reset Value	Description
3:2	RW	0x0	utmi_opmode UTMI+ Operational Mode Function: This controller bus selects the UTMI+ operational mode. 2'b11: Normal operation without SYNC or EOP generation. If the XCVRSEL bus is not set to 00 while OPMODE[1:0] is set to 11, USB PHYbehavior is undefined. 2'b10: Disable bit stuffing and NRZI encoding 2'b01: Non-Driving 2'b00: Normal
1	RW	0x0	utmi_suspend_n Suspend Assertion 1'b1: Normal operating mode 1'b0: Suspend mode
0	RW	0x0	usbphy_soft_con_sel 1'b0: software control USB PHY disable 1'b1: software control USB PHY enable

GRF_DDRC_STAT

Address: Operational Base + offset (0x0019c)

DDRC status

Bit	Attr	Reset Value	Description
31:21	RW	0x000	gpu_idle gpu idle staus
20	RW	0x0	ddrupctl_c_active Confirm that system external to PCTL can accept a Low-power request. Which is high valid.
19	RW	0x0	upctl_c_sysack PCTL low-power request status response. Which is high valid.
18:16	RO	0x0	ddrupctl_stat Current state of the protocol controller 3'b000: Init_mem 3'b001: Config 3'b010: Config_req 3'b011: Access 3'b100: Access_req 3'b101: Low_power 3'b110: Low_power_entry_req 3'b111: Low_power_exit_req

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Bit	Attr	Reset Value	Description
15:0	RO	0x0000	ddrupctl_bbflags Bank busy indication NIF output vector which provides combined information about the status of each memory bank. The de-assertion is based on when pre-charge, activates, reads/writes. Bit0 indication Bank0 busy, bit1 indication Bank1 busy, and so on.

GRF_SOC_STATUS1
Address: Operational Base + offset (0x001a4)
SoC status register

Bit	Attr	Reset Value	Description
31:11	RO	0x0	reserved
10	RO	0x0	mipi_ctrl_edpihalt Halt Indication on Video Interface Active State: High Registered: No. The halts from the command and payload FIFOs are OR'ed in the Command mode and then multiplexed with the h alt from the Video mode.
9	RO	0x0	mipi_ctrl_shutdown D-PHY Digital and Analog Shut Down
8	RO	0x0	mipi_ctrl_rstz D-PHY Reset
7	RO	0x0	mipi_ctrl_forcepll D-PHY Force PLL On Dependency: DSI_HOST_SNPS_PHY = False Active State: High
6	RO	0x0	reserved
5:0	RO	0x00	timer_en_status 1’b0: timer disable status 1’b1: timer enable status 1 means timer is enabled.

GRF_CPU_CON0
Address: Operational Base + offset (0x001a8)
CPU control register

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:14	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
13	RW	0x1	deviceen_dap Enabling access to the connected debug device or memory system 1'b0: disable 1'b1: enable
12	RW	0x0	l2rstdisable Disable automatic L2 cache invalidate at reset, active high.
11:8	RW	0x0	l1rstdisable Disable automatic data cache, instruction cache and TLB invalidate at reset. 4bits coresponding 4 cores, active high.
7:3	RO	0x0	reserved
2:0	RW	0x2	ema_mem_ctrl memory EMA signal control

GRF_CPU_CON1
Address: Operational Base + offset (0x001ac)
CPU control register

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:12	RO	0x0	reserved
11:8	RW	0x0	cfgte_a7 Controls processor state for exception handling (TE bit) at reset.
7:4	RW	0x0	vinithi_a7 Cortex-A7 vinithi bit control. Location of the exception vectors at reset. Sampled during reset. 1'b0: 0x0000_0000 1'b1: 0xffff_0000
3:0	RW	0x0	cfgend_a7 One bit for each processor. 1'b0: Little-endian 1'b1: Big-endian

GRF_CPU_CON2
Address: Operational Base + offset (0x001b0)
CPU control register

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:9	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
8	RW	0x0	cfgsdisable Disables write access to some secure GIC registers. When CFGSDISABLE is asserted, the GIC prevents writes to any register locations that control the operating state of an LSPI 1'b0: enable 1'b1: disable
7	RW	0x0	evento_clear Event output. Evento is active when one SEV instruction is executed. This bit used to clear evento signal. 1'b0: un-clear 1'b1: clear
6	RW	0x0	eventi Event input for processor wake-up from WFE state. This pin must be asserted for at least one CLKIN clock cycle. When this signal is asserted, it acts as a WFE wake-up event to all the processors in the multiprocessor device.
5	RW	0x1	dbgselfaddrv Debug self-address offset valid 1'b0: unvalid 1'b1: valid
4	RW	0x1	dbgromaddrv Debug ROM physical address valid: 1'b0: unvalid 1'b1: valid
3	RW	0x1	spniden Secure privileged non-invasive debug enable, active high.
2	RW	0x1	niden Non-invasive debug enable, active high.
1	RW	0x1	spiden Secure privileged invasive debug enable, active high.
0	RW	0x1	dbgen Debug enable, active high.

GRF_CPU_STATUS0
Address: Operational Base + offset (0x001c0)
CPU status register

Bit	Attr	Reset Value	Description
31:7	RO	0x0	reserved
6:3	RO	0x0	smpnamp_a7 Signals AMP or SMP mode for each Cortex-A7 processor. 1’b0: Asymmetric. 1’b1: Symmetric.

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Bit	Attr	Reset Value	Description
2	RO	0x0	jtagnsw_dap coresight jtagnsw signal status 1'b1: JTAG is selected. 1'b0: SWD is selected.
1	RO	0x0	jtagtop_dap coresight jtagtop signal status "1" means JTAG state machine is in one of the top four modes: test-logic-reset, run-test/idle, select-DR-scan, select-IR-scan.
0	RO	0x0	evento_rising_edge evento signal rising edge status

GRF_CPU_STATUS1
Address: Operational Base + offset (0x001c4)
CPU status register

Bit	Attr	Reset Value	Description
31:9	RO	0x0	reserved
8:5	RO	0x0	core_wfi_status Core WFI status, 4bit corresponding 4 cores.
4:1	RO	0x0	core_wfe_status Core WFE status, 4bit corresponding 4 cores.
0	RO	0x0	l2c_wfi_status L2 WFI status.

GRF_OS_REG0
Address: Operational Base + offset (0x001c8)
software OS register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	os_reg Software OS register, which can be used for general purpose.

GRF_OS_REG1
Address: Operational Base + offset (0x001cc)
software OS register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	os_reg Software OS register, which can be used for general purpose.

GRF_OS_REG2
Address: Operational Base + offset (0x001d0)
software OS register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	os_reg Software OS register, which can be used for general purpose.

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GRF_OS_REG3
Address: Operational Base + offset (0x001d4)
software OS register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	os_reg Software OS register, which can be used for general purpose.

GRF_OS_REG4
Address: Operational Base + offset (0x001d8)
software OS register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	os_reg Software OS register, which can be used for general purpose.

GRF_OS_REG5
Address: Operational Base + offset (0x001dc)
software OS register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	os_reg Software OS register, which can be used for general purpose.

GRF_OS_REG6
Address: Operational Base + offset (0x001e0)
software OS register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	os_reg Software OS register, which can be used for general purpose.

GRF_OS_REG7
Address: Operational Base + offset (0x001e4)
software OS register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	os_reg Software OS register, which can be used for general purpose.

GRF_PVTM_CON0
Address: Operational Base + offset (0x00200)
PVTM control register

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:14	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
13	RW	0x0	pvtm_func_osc_en Logic PVT monitor oscilator enable. 1'b1: enable 1'b0: disable
12	RW	0x0	pvtm_func_start Logic PVT monitor start control.
11:10	RO	0x0	reserved
9	RW	0x0	pvtm_gpu_osc_en PD_GPU PVT monitor oscilator enable. 1'b1: enable 1'b0: disable
8	RW	0x0	pvtm_gpu_start PD_GPU PVT monitor start control.
7:2	RO	0x0	reserved
1	RW	0x0	pvtm_core_osc_en PD_CORE PVT monitor oscilator enable. 1'b1: enable 1'b0: disable
0	RW	0x0	pvtm_core_start PD_CORE PVT monitor start control.

GRF_PVTM_CON1
Address: Operational Base + offset (0x00204)
PVTM control register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pvtm_core_cal_cnt PD_CORE PVT monitor calculator counter configuration.

GRF_PVTM_CON2
Address: Operational Base + offset (0x00208)
PVTM control register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pvtm_gpu_cal_cnt PD_GPU PVT monitor calculator counter configuration.

GRF_PVTM_CON3
Address: Operational Base + offset (0x0020c)
PVTM control register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pvtm_func_cal_cnt Logic PVT monitor calculator counter configuration.

GRF_PVTM_STATUS0
Address: Operational Base + offset (0x00210)
PVTM status register0

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Bit	Attr	Reset Value	Description
31:3	RO	0x0	reserved
2	RO	0x0	pvtm_func_freq_done Logic PVT monitor frequency calculate done status.
1	RO	0x0	pvtm_core_freq_done PD_CORE PVT monitor frequency calculate done status.
0	RO	0x0	pvtm_gpu_freq_done PD_GPU PVT monitor frequency calculate done status.

GRF_PVTM_STATUS1
Address: Operational Base + offset (0x00214)
PVTM status register1

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pvtm_core_freq_cnt PD_CORE PVT monitor frequency count status.

GRF_PVTM_STATUS2
Address: Operational Base + offset (0x00218)
PVTM status register2

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pvtm_gpu_freq_cnt PD_GPU PVT monitor frequency count status.

GRF_PVTM_STATUS3
Address: Operational Base + offset (0x0021c)
PVTM status register3

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pvtm_func_freq_cnt Logic PVT monitor frequency count status.

GRF_DFI_WRNUM
Address: Operational Base + offset (0x00220)
DFI write number register

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dfi_eff_wr_num The total number of write operation on DFI interface.

GRF_DFI_RDNUM
Address: Operational Base + offset (0x00224)
DFI read number register

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dfi_eff_rd_num The total number of read operation on DFI interface.

GRF_DFI_ACTNUM

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Address: Operational Base + offset (0x00228)
DFI active number register

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dfi_eff_act_num The total number of active operation on DFI interface.

GRF_DFI_TIMERVAL
Address: Operational Base + offset (0x0022c)
DFI work time

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	dfi_timer_val The total time for DFI monitor works.

GRF_NIF_FIFO0
Address: Operational Base + offset (0x00230)
NIF status register

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	nif0_fifo0 Recorded current DDR address 0. It will not be cleared by system reset.

GRF_NIF_FIFO1
Address: Operational Base + offset (0x00234)
NIF status register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	nif0_fifo1 Recorded current DDR address 1. It will not be cleared by system reset.

GRF_NIF_FIFO2
Address: Operational Base + offset (0x00238)
NIF status register

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	nif0_fifo2 Recorded current DDR address 2. It will not be cleared by system reset.

GRF_NIF_FIFO3
Address: Operational Base + offset (0x0023c)
NIF status register

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	nif0_fifo3 Recorded current DDR address 3. It will not be cleared by system reset.

GRF_USBPHY0_CON0

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Address: Operational Base + offset (0x00280)
usbphy control register

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:13	RW	0x4	squel_trigger_con bit2 ~ bit0 of squel_trigger_con 4'b0000: 112.5mV 4'b1001: 162.5mV 4'b1011: 175mV 4'b1100: 150mV(default) 4'b1110: 125mV
12:11	RW	0x0	non_driving Registers for non-driving state control. Non-driving state is controlled by op-mode by default, when bit[11] is configured with "1", user can control non-driving state trough bit[12].
10:8	RW	0x6	tx_clk_phase_con USB Tx Clock phase configure, 3'b000 represent the earliest phase, and 3'b111 the latest, single step delay is 256ps
7:5	RW	0x0	rx_clk_phase_con USB Rx Clock phase configure, 3'b000 represent the earliest phase, and 3'b111 the latest, single step delay is 256ps
4:3	RW	0x3	fls_eye_height FS/LS eye height configure, 2'b00 represent the largest slew rate, 2'b11 represent the smallest slew rate
2:0	RW	0x0	hs_eye_diag_adjust HS eye diagram adjust, open HS pre-emphasize function to increase HS slew rate, only used when large cap loading is attached. 3'b001: open pre-emphasize in sof or eop state 3'b010: open pre-emphasize in chirp state 3'b100: open pre-emphasize in non-chirp state 3'b111: always open pre-emphasize other combinations : reserved

GRF_USBPHY0_CON1
Address: Operational Base + offset (0x00284)
usbphy control register

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit

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Bit	Attr	Reset Value	Description
15:13	RW	0x7	hs_eye_height bit2 ~ bit0 of hs_eye_height. HS eye height tuning, more zeros represent bigger eye, more ones represent smaller eye
12:3	RO	0x0	reserved
2	RW	0x1	current_comp_en Enable current compensation, active high.
1	RW	0x1	res_comp_en Enable resistance compensation, active high.
0	RW	0x1	squel_trigger_con bit3 of squel_trigger_con 4'b0000: 112.5mV 4'b1001: 162.5mV 4'b1011: 175mV 4'b1100: 150mV(default) 4'b1110: 125mV

GRF_USBPHY0_CON2
Address: Operational Base + offset (0x00288)
usbphy control register

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x1	odt_compensation bit0 of odt_compensation ODT Compensation voltage reference 3'b000: 200mV 3'b001: 187.5mV(default) 3'b010: 225mV 3'b110: 175mV 3'b111: 162.5mV
14:13	RW	0x0	voltage_tolerance_adjust 5V tolerance detection reference adjust, 2'b11 represent the highest trigger point, keeping the default value is greatly appreciated.
12	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
11:10	RW	0x0	auto_compensation_bypass Auto compensation bypass, 2'b11 will bypass current and ODT compensation, customers can set the driver strength and currentmanually. For larger HS eye height, customer can give more 1'b0 for hs_eye_height; For larger HS/FS/LS slew rate, give more 1'b1 for hfs_driver_strength.
9:5	RW	0x15	hfs_driver_strength HS/FS driver strength tuning, 5'b11111 represent the largest slew rate and 5'b10000 represents the smallest slew rate.
4:0	RW	0x0a	hs_eye_height bit7 ~ bit3 of hs_eye_height. HS eye height tuning, more zeros represent bigger eye, more ones represent smaller eye.

GRF_USBPHY0_CON3

Address: Operational Base + offset (0x0028c)

usbphy control register

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RO	0x0	reserved
14	RW	0x0	vol_toleran_det_con 5V tolerance detection function controlling bit trough registers, only active when bit[65] is set 1'b1.
13:10	RO	0x0	reserved
9	RW	0x1	odt_auto_refresh A port ODT auto refresh bypass, active low, this register should only be used when auto_compensation_bypass were set to 2'b11. In bypass mode, customer can configure driver strength through hfs_driver_strength.
8	RW	0x0	bg_out_voltage_adjust BG output voltage reference adjust, keeping the default value is greatly appreciated.
7:5	RW	0x0	compen_current_ref compensation current tuning reference 3'b000: 200mV(default) 3'b001: 187.5mV 3'b010: 225mV 3'b110: 175mV 3'b111: 162.5mV

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Bit	Attr	Reset Value	Description
4:2	RW	0x0	bias_current_ref bias current tuning reference 3'b000: 400mV(default) 3'b001: 362.5mV 3'b010: 350mV 3'b101: 425mV 3'b111: 450mV
1:0	RW	0x0	odt_compensation bit2 ~ bit1 of odt_compensation. ODT Compensation voltage reference 3'b000: 200mV 3'b001: 187.5mV(default) 3'b010: 225mV 3'b110: 175mV 3'b111: 162.5mV

GRF_USBPHY0_CON4
Address: Operational Base + offset (0x00290)
usbphy control register

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:2	RO	0x0	reserved
1	RW	0x1	bypass_5v_tolerance_det Bypass 5V tolerance detection function, active high.
0	RO	0x0	reserved

GRF_USBPHY0_CON6
Address: Operational Base + offset (0x00298)
usbphy control register

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:13	RW	0x0	session_end_con session_end reference tuning
12:10	RW	0x0	b_session_con B_sessionvalid reference tuning
9:7	RW	0x0	a_session_con A_sessionvalid reference tuning
6	RW	0x0	force_vbus_valid force output vbus_valid asserted, active high

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Bit	Attr	Reset Value	Description
5	RW	0x0	force_session_end_val force output session_end asserted, active high
4	RW	0x0	force_b_session_val force output B_sessionvalid asserted, active high
3	RW	0x0	force_a_session_val force output A_sessionvalid asserted, active high
2	RW	0x1	turn_off_diff_receiver Turn off differential receiver in suspend mode to save power, active low.
1:0	RO	0x0	reserved

GRF_USBPHY0_CON7
Address: Operational Base + offset (0x0029c)
Usbphy0 control register

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RO	0x0	reserved
14:11	RW	0xd	host_discon_con HOST disconnect detection trigger point configure, only used in HOST mode. 4'b0000: 575mV 4'b0001: 600mV 4'b1001: 625mV 4'b1101: 650mV(default)
10:8	RO	0x0	reserved
7	RW	0x1	bypass_squelch_trigger Bypass squelch trigger point auto configure in chirp modes, active high.
6	RW	0x1	half_bit_pre_empha_en Half bit pre-emphasize enable, active high. 1'b1 represents half bit pre-emphasis, 1'b0 for full bit.
5:3	RO	0x0	reserved
2:0	RW	0x0	vbus_valid_con vbus_valid reference tuning

GRF_USBPHY1_CON0
Address: Operational Base + offset (0x002a0)
usbphy control register

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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:13	RW	0x4	squel_trigger_con bit2 ~ bit0 of squel_trigger_con 4'b0000: 112.5mV 4'b1001: 162.5mV 4'b1011: 175mV 4'b1100: 150mV(default) 4'b1110: 125mV
12:11	RW	0x0	non_driving Registers for non-driving state control. Non-driving state is controlled by op-mode by default, when bit[11] is configured with 1'b1, user can control non-driving state trough bit[12].
10:8	RW	0x6	tx_clk_phase_con USB Tx Clock phase configure, 3'b000 represent the earliest phase , and 3'b111 the latest, single step delay is 256ps.
7:5	RW	0x0	rx_clk_phase_con USB Rx Clock phase configure, 3'b000 represent the earliest phase, and 3'b111 the latest, single step delay is 256ps.
4:3	RW	0x3	fls_eye_height FS/LS eye height configure, 2'b00 represent the largest slew rate, 2'b11 represent the smallest slew rate.
2:0	RW	0x0	hs_eye_diag_adjust HS eye diagram adjust, open HS pre-emphasize function to increase HS slew rate, only used when large cap loading is attached. 3'b001: open pre-emphasize in sof or eop state 3'b010: open pre-emphasize in chirp state 3'b100: open pre-emphasize in non-chirp state 3'b111: always open pre-emphasize other combinations: reserved

GRF_USBPHY1_CON1

Address: Operational Base + offset (0x002a4)

usbphy control register

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit

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Bit	Attr	Reset Value	Description
15:13	RW	0x7	hs_eye_height bit2 ~ bit0 of hs_eye_height. HS eye height tuning, more zeros represent bigger eye, more ones represent smaller eye.
12:3	RO	0x0	reserved
2	RW	0x1	current_comp_en Enable current compensation, active high.
1	RW	0x1	res_comp_en Enable resistance compensation, active high.
0	RW	0x1	squel_trigger_con bit3 of squel_trigger_con 4'b0000: 112.5mV 4'b1001: 162.5mV 4'b1011: 175mV 4'b1100: 150mV(default) 4'b1110: 125mV

GRF_USBPHY1_CON2
Address: Operational Base + offset (0x002a8)
usbphy control register

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x1	odt_compensation bit0 of odt_compensation ODT Compensation voltage reference 3'b000: 200mV 3'b001: 187.5mV(default) 3'b010: 225mV 3'b110: 175mV 3'b111: 162.5mV
14:13	RW	0x0	voltage_tolerance_adjust 5V tolerance detection reference adjust, 2'b11 represent the highest trigger point, keeping the default value is greatly appreciated.
12	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
11:10	RW	0x0	auto_compensation_bypass Auto compensation bypass, 2'b11 will bypass current and ODT compensation, customers can set the driver strength and currentmanually. For larger HS eye height, customer can give more "0" for hs_eye_height; For larger HS/FS/LS slew rate, give more "1" for hfs_driver_strength.
9:5	RW	0x15	hfs_driver_strength HS/FS driver strength tuning, 5'b11111 represent the largest slew rate and 5'b10000 represents the smallest slew rate.
4:0	RW	0x0a	hs_eye_height bit7 ~ bit3 of hs_eye_height. HS eye height tuning, more zeros represent bigger eye, moreones represent smaller eye.

GRF_USBPHY1_CON3
Address: Operational Base + offset (0x002ac)
usbphy control register

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RO	0x0	reserved
14	RW	0x0	vol_toleran_det_con 5V tolerance detection function controlling bit trough registers,only active when bit[65] is set 1'b1.
13:10	RO	0x0	reserved
9	RW	0x1	odt_auto_refresh A port ODT auto refresh bypass, active low, this register shouldonly be used when auto_compensation_bypass were set to 2'b11. In bypass mode, customer can configure driver strength through hfs_driver_strength.
8	RW	0x0	bg_out_voltage_adjust BG output voltage reference adjust, keeping the default value isgreatly appreciated.
7:5	RW	0x0	compen_current_ref compensation current tuning reference 3'b000: 200mV(default) 3'b001: 187.5mV 3'b010: 225mV 3'b110: 175mV 3'b111: 162.5mV

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Bit	Attr	Reset Value	Description
4:2	RW	0x0	bias_current_ref bias current tuning reference 3'b000: 400mV(default) 3'b001: 362.5mV 3'b010: 350mV 3'b101: 425mV 3'b111: 450mV
1:0	RW	0x0	odt_compensation bit2 ~ bit1 of odt_compensation ODT Compensation voltage reference 3'b000: 200mV 3'b001: 187.5mV(default) 3'b010: 225mV 3'b110: 175mV 3'b111: 162.5mV

GRF_USBPHY1_CON4
Address: Operational Base + offset (0x002b0)
usbphy control register

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:2	RO	0x0	reserved
1	RW	0x1	bypass_5v_tolerance_det Bypass 5V tolerance detection function, active high.
0	RO	0x0	reserved

GRF_USBPHY1_CON6
Address: Operational Base + offset (0x002b8)
usbphy control register

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:13	RW	0x0	session_end_con session_end reference tuning
12:10	RW	0x0	b_session_con B_sessionvalid reference tuning
9:7	RW	0x0	a_session_con A_sessionvalid reference tuning
6	RW	0x0	force_vbus_valid force output vbus_valid asserted, active high

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Bit	Attr	Reset Value	Description
5	RW	0x0	force_session_end_val force output session_end asserted, active high
4	RW	0x0	force_b_session_val force output B_sessionvalid asserted, active high
3	RW	0x0	force_a_session_val force output A_sessionvalid asserted, active high
2	RW	0x1	turn_off_diff_receiver Turn off differential receiver in suspend mode to save power,active low.
1:0	RO	0x0	reserved

GRF_USBPHY1_CON7
Address: Operational Base + offset (0x002bc)
usbphy control register

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable. When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RO	0x0	reserved
14:11	RW	0xd	host_discon_con HOST disconnect detection trigger point configure, only used in HOST mode 4'b0000: 575mV 4'b0001: 600mV 4'b1001: 625mV 4'b1101: 650mV(default)
10:8	RO	0x0	reserved
7	RW	0x1	bypass_squelch_trigger Bypass squelch trigger point auto configure in chirp modes, active high.
6	RW	0x1	half_bit_pre_empha_en Half bit pre-emphasize enable, active high. "1" represent half bit pre-emphasis, "0" for full bit.
5:3	RO	0x0	reserved
2:0	RW	0x0	vbus_valid_con vbus_valid reference tuning

GRF_UOC_STATUS0
Address: Operational Base + offset (0x002c0)
SoC status register 0

Bit	Attr	Reset Value	Description
31:26	RW	0x00	usbhost0_stat_ehci_usbsts USB host0 ehci_usbsts bit status

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Bit	Attr	Reset Value	Description
25:15	RW	0x000	usbhost0_stat_ehci_xfer_cnt USB host0 ehci_xfer counter status
14	RW	0x0	usbhost0_stat_ehci_xfer_prdc USB host0 ehci_xfer_prdc bit status
13:10	RW	0x0	usbhost0_stat_ehci_lpsmc_state USB host0 ehci_lpsmc_state bit status
9	RW	0x0	usbhost0_stat_ehci_bufacc USB host0 ehci_bufacc bit status
8	RW	0x0	usbhost0_stat_ohci_globalsuspend USB host0 ohci_globalsuspend bit status
7	RW	0x0	Copy1 usbhost0_stat_dp_attached USB HOST0 dp_attached signal status
6	RW	0x0	usbhost0_stat_cp_detected USB HOST0 cp_detected signal status
5	RW	0x0	usbhost0_stat_dcp_attached USB HOST0 dcp_atteched signal status
4	RW	0x0	usbhost0_stat_ohci_bufacc USB HOST0 ohci_bufacc signal status
3	RW	0x0	usbhost0_stat_ohci_rmtwkp USB HOST0 ohci_rmtwkp signal status
2	RW	0x0	usbhost0_stat_ohci_drwe USB HOST0 ohci_drwe signal status
1	RW	0x0	usbhost0_stat_ohci_rwe USB HOST0 ohci_rwe signal status
0	RW	0x0	usbhost0_stat_ohci_ccs USB HOST0 ohci_ccs signal status

GRF_CHIP_TAG
Address: Operational Base + offset (0x00300)
chip tag register

Bit	Attr	Reset Value	Description
31:0	RO	0x00003136	chip_tag

GRF_MMC_DET_CNT
Address: Operational Base + offset (0x00304)
mmc0 detect filter counter register

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:0	RW	0x0fdb9	mmc_det_value sdmmc detect filter counter initial value

GRF_EFUSE_PRG_EN
Address: Operational Base + offset (0x0037c)
eFuse program register

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Bit	Attr	Reset Value	Description
31:14	RO	0x0	reserved
13	RO	0x0	eFuse_prg_en 1'b0: eFuse program disable 1'b1: eFuse program enable
12:0	RO	0x0	reserved

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Chapter 5 Embedded Processor (Cortex-A7)

5.1 Overview

The Cortex-A7 MP subsystem of the device is based on the symmetric multiprocessor (SMP) architecture, thus the quad Cortex-A7 MPU subsystem delivers higher performance and optimal power management, debug and emulation capabilities.
The Cortex-A7 MP subsystem incorporates four Cortex-A7 central processing units (CPUs), level 2(L2) cache shared between the four CPUs, and uses PL310 as L2 cache controller. Each CPU has 32KBof level 1 (L1) instruction cache, 32KB of L1 data cache, separate dedicated power domain, and includes one Neon and Vector Floating Point Unit coprocessors. The Cortex-A7 MP subsystem also includes standard CoreSight components to support SMP debug and emulation, snoop control unit(SCU), interrupt controller (GIC), and clock and reset manager.
The key features of the Cortex-A7 MP subsystem include:

- ARM Coretex-A7 based quad MPU subsystem with SMP architecture
  - Cortex-A7 core revision r0p5
  - Full implements the ARMv7-A architecture profile that includes SIMD and VFP
  - 32KB L1 I-cache and 32KB L1 D-cache per CPU
  - In-order pipeline with direct and indirect branch prediction
  - Harvard Level 1 (L1) memory system with a Memory Management Unit (MMU)
  - SCU ensures memory coherency between the 4 CPUs
  - Interrupt controller with 128 hardware interrupt inputs
- 256KB L2 cache shared between the 4 CPUs
  - Fixed line length of 64 bytes.
  - Physically indexed and tagged cache.
  - 8-way set-associative cache structure.
  - Pseudo-random cache replacement policy.

5.2 Block Diagram

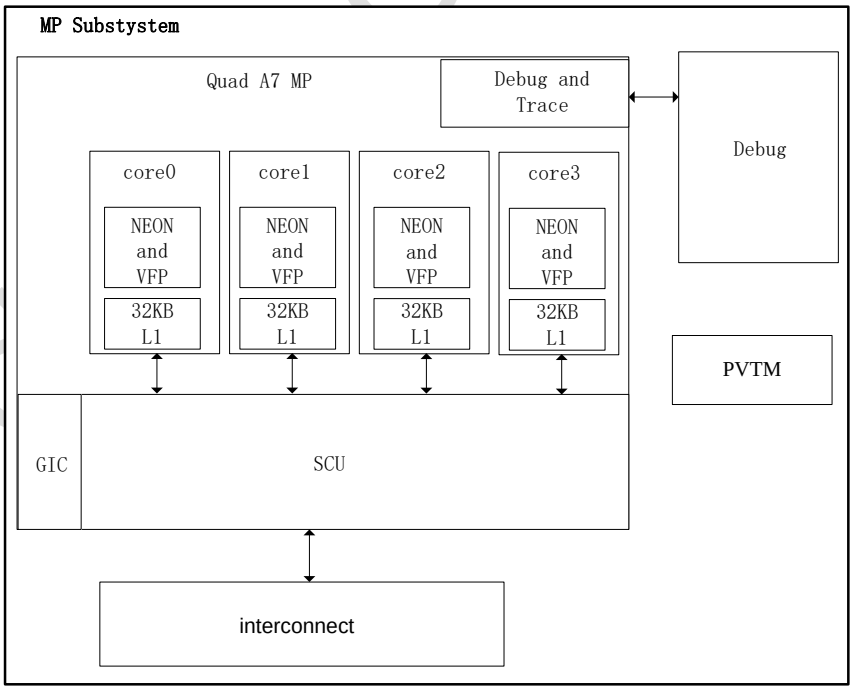


Fig. 5-1 MP Subsystem architecture

5.3 Function description

Please refer to the Cortex-A7 documents for the CPU detail description.

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Chapter 6 Embedded SRAM

6.1 Overview

The Embedded SRAM is the AXI slave device, which supports read and write access to provide system fast access data storage.

6.1.1 Features supported

- Provide 8KB access space
- Support 64bit AXI bus

6.1.2 Features not supported

- Don't support AXI lock transaction
- Don't support AXI exclusive transaction
- Don't support AXI cache function
- Don't support AXI protection function

6.2 Block Diagram

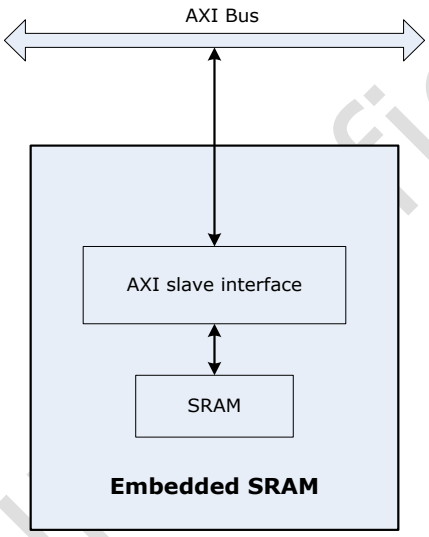


Fig. 6-1 Embedded SRAM block diagram

6.3 Function Description

6.3.1 AXI slave interface

The AXI slave interface is a bridge which translates AXI bus access to SRAM interface.

6.3.2 Embedded SRAM access path

The Embedded SRAM can only be accessed by Cortex-A7.

6.3.3 Remap

The Embedded SRAM support remapping.
Before remap, the Embedded SRAM address range is 0x1008_0000 ~ 0x1008_1fff.
After set remap, (controlled by GRF_SOC_CON0[12]), the system can still access the Embedded SRAM by the old address. At same time, the system also can access the Embedded SRAM by the new address 0x0000_0000 ~ 0x0000_1fff.

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Chapter 7 Nand Flash Controller (NandC)

7.1 Overview

Nand Flash Controller (NandC) is used to control data transmission from host to flash device or from flash device to host. NandC is connected to AHB BUS through an AHB Master and an AHB Slave. The data transmission between host and external memory can be done through AHB Master interface or AHB Slave interface.
NandC supports the following features:

- NandC AHB bus clock (hclk) is asynchronous to NandC working clock (nclk)
- Software Interface Type
  - Support directly mode
  - Support LLP(Linked List Pointer) mode
- Flash Interface Type
  - Support Asynchronous Flash Interface with 8bits datawidth ("Asyn8x" for short)
  - Support ONFI Synchronous Flash Interface ("ONFI Syn" for short)
  - Support Toggle Flash Interface ("Toggle" for short)
  - Support 4 flash devices at most
- Flash Type
  - Support Managed NAND Flash(LBA) and Raw NAND Flash(NO-LBA)
  - Support SLC/MLC/TLC Flash
- Flash Interface Timing
  - Asyn8x: configurable timing, one byte per two Nandc working clocks at the fastest speed
  - ONFI Syn: configurable timing, two bytes per two Nandc working clocks at the fastest speed
  - Toggle: configurable timing, two byte per two Nandc working clocks at the fastest speed
- Randomizer Ability
  - Support three randomizer mode with different polynomial
  - Support two randomizer width, 8bit and 16bit parallel
- BCH/ECC Ability
  - 16bit/1KB BCH/ECC: support 16bitBCH/ECC, which can detect and correct up to 16 error bits in every 1K bytes data
  - 24bit/1KB BCH/ECC: support 24bitBCH/ECC, which can detect and correct up to 24 error bits in every 1K bytes data
  - 40bit/1KB BCH/ECC: support 40bitBCH/ECC, which can detect and correct up to 40 error bits in every 1K bytes data
  - 60bit/1KB BCH/ECC: support 60bitBCH/ECC, which can detect and correct up to 60 error bits in every 1K bytes data
  - 8bit/512B BCH/ECC: support 8bitBCH/ECC, which can detect and correct up to 8 error bits in every 512 bytes data
  - 12bit/512B BCH/ECC: support 12bitBCH/ECC, which can detect and correct up to 12 error bits in every 512 bytes data
  - 20bit/512B BCH/ECC: support 20bitBCH/ECC, which can detect and correct up to 20 error bits in every 512 bytes data
  - 30bit/512B BCH/ECC: support 30bitBCH/ECC, which can detect and correct up to 30 error bits in every 512 bytes data
  - 16bit/512B BCH/ECC: support 16bitBCH/ECC, which can detect and correct up to 16 error bits in every 512 bytes data
  - 24bit/512B BCH/ECC: support 24bitBCH/ECC, which can detect and correct up to 24 error bits in every 512 bytes data
  - 40bit/512B BCH/ECC: support 40bitBCH/ECC, which can detect and correct up to 40 error bits in every 512 bytes data
  - 60bit/512B BCH/ECC: support 60bitBCH/ECC, which can detect and correct up to 60 error bits in every 512 bytes data
- Transmission Ability
  - Support 32K bytes data transmission at a time at most

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- Support two transfer working modes: Bypass or DMA
- Support two transfer codeword size for Managed NAND Flash: 1024 bytes/codeword or 512 bytes/codeword

- Internal Memory
  - 2 built-in srams, and the size is 1k bytes respectively
  - Can be accessed by other masters
  - Can be operated in ping-pong mode by other masters

7.2 Block Diagram

NandC comprises with:

- MIF: AHB Master Interface
- SIF : AHB Slave Interface
- SRIF : Sram Interface
- TRANSC : Transfer Controller
- LLPC : LLP Controller
- BCHENC : BCH Encoder
- BCHDEC : BCH Decoder
- RANDMZ : Randomizer
- FIF_GEN : Flash Interface Generation
- DLC : Delay Line Controller

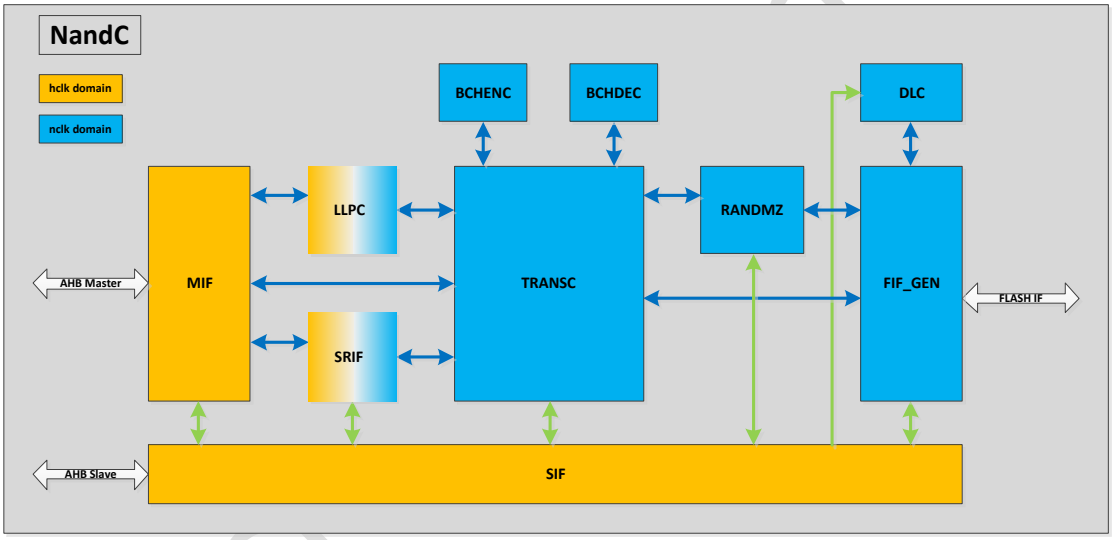


Fig. 7-1 NandC Block Diagram

7.3 Function Description

7.3.1 AHB Interface

There is an AHB master interface in NandC, which is selectable and configurable. It is responsible for transferring data from external memory to internal memory when flash program, or inverse when flash read; and transferring LLP data from external memory to internal register file when LLP is active.

There is an AHB slave interface in NandC. It is responsible for accessing registers and internal memories. The addresses of these registers and memories are listed in "Internal Address Mapping" section.

7.3.2 Flash Type/Flash Interface

Flash device with different types of interfaces is supported. These interfaces include: asynchronous 8bits flash interface, asynchronous 16bits flash interface, ONFI synchronous flash interface, toggle flash interface, and so on. You can select one of them by software (configure FMCTL) to suit for these devices. Also you can configure their timing parameters by software (configure FMWAIT_ASYN/FMWAIT_SYN) to have your desired rate.

7.3.3 Linked List Pointer Mode (LLP)

To save the software resource and improve the performance, a LLP is add, which is

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selectable. When LLP is selected, the flash operation instructions stored in external memory with specific format should be loaded for flash working. The detailed format and working flow are referred to "LLP Application" section.

7.3.4 BCH Encoder/BCH Decoder

The BCH Encoder is responsible for encoding data to be written into flash device. The max encoded length is 1133bytes, in which the data length is 1024bytes, system information is 4bytes, BCH code is 105bytes.

The BCH Decoder is responsible for decoding data read from flash device. The max decoded length is 1133bytes, in which the data length is 1024bytes, spare length is 109bytes.

7.3.5 Randomizer

To improve device lifetime, a randomizer is added in NandC. It includes two parts: Scrambler and Descrambler, which is responsible for scrambling data to be written into flash after bch encoding, and descrambling data read from flash before bch decoding.

7.3.6 Delay Line Controller

For ONFI Synchronous Flash or Toggle Flash, the data read from flash follows with a strobe signal: DQS, where a skew between them exists. To remove the skew and improve the timing between data and DQS, a Delay Line Controller is needed. It is responsible for detecting the phase of the signal similar to DQS, determining the element number to be shifted, and then shifting the DQS with the determined number.

7.4 Register Description

7.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

Table 7-1 NandC Address Mapping

Base Address[12:8]	Device	Address Length	Offset Address Range
5'b00_00x(x=0, 1)	FLR	512 BYTE	0x0000 ~ 0x01ff
5'b00_01x(x=0, 1)	SPR	512 BYTE	0x0200 ~ 0x03ff
5'b00_10x(x=0, 1)	FLR1	512 BYTE	0x0400 ~ 0x05ff
5'b00_11x(x=0, 1)	FLR2	512 BYTE	0x0600 ~ 0x07ff
5'b01_000	Flash0	256 BYTE	0x0800 ~ 0x08ff
5'b01_001	Flash1	256 BYTE	0x0900 ~ 0x09ff
5'b01_010	Flash2	256 BYTE	0x0a00 ~ 0x0aff
5'b01_011	Flash3	256 BYTE	0x0b00 ~ 0x0bff
5'b01_100	Flash4	256 BYTE	0x0c00 ~ 0x0cff
5'b01_101	Flash5	256 BYTE	0x0d00 ~ 0x0dff
5'b01_110	Flash6	256 BYTE	0x0e00 ~ 0x0eff
5'b01_111	Flash7	256 BYTE	0x0f00 ~ 0x0fff
5'b10_0xx(x=0, 1)	Sram0	1K BYTE	0x1000 ~ 0x13ff
5'b10_1xx(x=0, 1)	Sram1	1K BYTE	0x1400 ~ 0x17ff

7.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
NANDC_FMCTL	0x0000	W	0x00000200	Flash Interface Control Register
NANDC_FMWAIT_ASYN	0x0004	W	0x3f03f7ff	Flash Timing Control Register For Asynchronous Timing
NANDC_FLCTL	0x0008	W	0x00100000	Internal Transfer Control Register
NANDC_BCHCTL	0x000c	W	0x00000008	BCH Control Register
NANDC_MTRANS_CFG	0x0010	W	0x000001d0	Bus Transfer Configuration Register
NANDC_MTRANS_SADDR0	0x0014	W	0x00000000	Start Address Register For Page Data Transmission

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Name	Offset	Size	Reset Value	Description
NANDC_MTRANS_SADDR1	0x0018	W	0x00000000	Start Address Register For Spare Data Transmission
NANDC_MTRANS_STAT	0x001c	W	0x00000000	Bus Transfer Status Register
NANDC_BCHST0	0x0020	W	0x04000000	BCH Status Register For Codeword 0~1
NANDC_BCHST1	0x0024	W	0x00000000	BCH Status Register For Codeword 2~3
NANDC_BCHST2	0x0028	W	0x00000000	BCH Status Register For Codeword 4~5
NANDC_BCHST3	0x002c	W	0x00000000	BCH Status Register For Codeword 6~7
NANDC_BCHST4	0x0030	W	0x00000000	BCH Status Register For Codeword 8~9
NANDC_BCHST5	0x0034	W	0x00000000	BCH Status Register For Codeword 10~11
NANDC_BCHST6	0x0038	W	0x00000000	BCH Status Register For Codeword 12~13
NANDC_BCHST7	0x003c	W	0x00000000	BCH Status Register For Codeword 14~15
NANDC_BCHLOC0	0x0040	W	0x00000000	BCH Error Bit Location Number Register For Codeword 0~5
NANDC_BCHLOC1	0x0044	W	0x00000000	BCH Error Bit Location Number Register For Codeword 6~11
NANDC_BCHLOC2	0x0048	W	0x00000000	BCH Error Bit Location Number Register For Codeword12~15
NANDC_BCHLOC3	0x004c	W	0x00000000	Highest Bit For BCH Error Bit Location Number Register
NANDC_BCHDE0_0	0x0070	W	0x00000000	BCH decode result of 0th error bit for codeword 0
NANDC_BCHDE0_1	0x0074	W	0x00000000	BCH decode result of 1th error bit for codeword 0
NANDC_BCHDE0_2	0x0078	W	0x00000000	BCH decode result of 2th error bit for codeword 0
NANDC_BCHDE0_3	0x007c	W	0x00000000	BCH decode result of 3th error bit for codeword 0
NANDC_BCHDE0_4	0x0080	W	0x00000000	BCH decode result of 4th error bit for codeword 0
NANDC_BCHDE0_5	0x0084	W	0x00000000	BCH decode result of 5th error bit for codeword 0
NANDC_BCHDE0_6	0x0088	W	0x00000000	BCH decode result of 6th error bit for codeword 0
NANDC_BCHDE0_7	0x008c	W	0x00000000	BCH decode result of 7th error bit for codeword 0

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Name	Offset	Size	Reset Value	Description
NANDC_BCHDE0_8	0x0090	W	0x00000000	BCH decode result of 8th error bit for codeword 0
NANDC_BCHDE0_9	0x0094	W	0x00000000	BCH decode result of 9th error bit for codeword 0
NANDC_BCHDE0_10	0x0098	W	0x00000000	BCH decode result of 10th error bit for codeword 0
NANDC_BCHDE0_11	0x009c	W	0x00000000	BCH decode result of 11th error bit for codeword 0
NANDC_BCHDE0_12	0x00a0	W	0x00000000	BCH decode result of 12th error bit for codeword 0
NANDC_BCHDE0_13	0x00a4	W	0x00000000	BCH decode result of 13th error bit for codeword 0
NANDC_BCHDE0_14	0x00a8	W	0x00000000	BCH decode result of 14th error bit for codeword 0
NANDC_BCHDE0_15	0x00ac	W	0x00000000	BCH decode result of 15th error bit for codeword 0
NANDC_BCHDE0_16	0x00b0	W	0x00000000	BCH decode result of 16th error bit for codeword 0
NANDC_BCHDE0_17	0x00b4	W	0x00000000	BCH decode result of 17th error bit for codeword 0
NANDC_BCHDE0_18	0x00b8	W	0x00000000	BCH decode result of 18th error bit for codeword 0
NANDC_BCHDE0_19	0x00bc	W	0x00000000	BCH decode result of 19th error bit for codeword 0
NANDC_BCHDE0_20	0x00c0	W	0x00000000	BCH decode result of 20th error bit for codeword 0
NANDC_BCHDE0_21	0x00c4	W	0x00000000	BCH decode result of 21th error bit for codeword 0
NANDC_BCHDE0_22	0x00c8	W	0x00000000	BCH decode result of 22th error bit for codeword 0
NANDC_BCHDE0_23	0x00cc	W	0x00000000	BCH decode result of 23th error bit for codeword 0
NANDC_BCHDE1_0	0x00d0	W	0x00000000	BCH decode result of 0th error bit for codeword 1
NANDC_BCHDE1_1	0x00d4	W	0x00000000	BCH decode result of 1th error bit for codeword 1
NANDC_BCHDE1_2	0x00d8	W	0x00000000	BCH decode result of 2th error bit for codeword 1
NANDC_BCHDE1_3	0x00dc	W	0x00000000	BCH decode result of 3th error bit for codeword 1
NANDC_BCHDE1_4	0x00e0	W	0x00000000	BCH decode result of 4th error bit for codeword 1
NANDC_BCHDE1_5	0x00e4	W	0x00000000	BCH decode result of 5th error bit for codeword 1

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Name	Offset	Size	Reset Value	Description
NANDC_BCHDE1_6	0x00e8	W	0x00000000	BCH decode result of 6th error bit for codeword 1
NANDC_BCHDE1_7	0x00ec	W	0x00000000	BCH decode result of 7th error bit for codeword 1
NANDC_BCHDE1_8	0x00f0	W	0x00000000	BCH decode result of 8th error bit for codeword 1
NANDC_BCHDE1_9	0x00f4	W	0x00000000	BCH decode result of 9th error bit for codeword 1
NANDC_BCHDE1_10	0x00f8	W	0x00000000	BCH decode result of 10th error bit for codeword 1
NANDC_BCHDE1_11	0x00fc	W	0x00000000	BCH decode result of 11th error bit for codeword 1
NANDC_BCHDE1_12	0x0100	W	0x00000000	BCH decode result of 12th error bit for codeword 1
NANDC_BCHDE1_13	0x0104	W	0x00000000	BCH decode result of 13th error bit for codeword 1
NANDC_BCHDE1_14	0x0108	W	0x00000000	BCH decode result of 14th error bit for codeword 1
NANDC_BCHDE1_15	0x010c	W	0x00000000	BCH decode result of 15th error bit for codeword 1
NANDC_BCHDE1_16	0x0110	W	0x00000000	BCH decode result of 16th error bit for codeword 1
NANDC_BCHDE1_17	0x0114	W	0x00000000	BCH decode result of 17th error bit for codeword 1
NANDC_BCHDE1_18	0x0118	W	0x00000000	BCH decode result of 1th error bit for codeword 1
NANDC_BCHDE1_19	0x011c	W	0x00000000	BCH decode result of 19th error bit for codeword 1
NANDC_BCHDE1_20	0x0120	W	0x00000000	BCH decode result of 20th error bit for codeword 1
NANDC_BCHDE1_21	0x0124	W	0x00000000	BCH decode result of 21th error bit for codeword 1
NANDC_BCHDE1_22	0x0128	W	0x00000000	BCH decode result of 22th error bit for codeword 1
NANDC_BCHDE1_23	0x012c	W	0x00000000	BCH decode result of 23th error bit for codeword 1
NANDC_DLL_CTL_REG0	0x0130	W	0x00000000	DLL Control Register 0
NANDC_DLL_CTL_REG1	0x0134	W	0x00000000	DLL Control Register 1
NANDC_DLL_OBS_REG0	0x0138	W	0x00000002	DLL Status Register
NANDC_RANDMZ_CFG	0x0150	W	0x00000000	Randomizer Configure Register
NANDC_FMWAIT_SYN	0x0158	W	0x00000411	Flash Timing Control Register For Synchronous Timing
NANDC_NANDC_VER	0x0160	W	0x56363030	Nandc Version Register
NANDC_LLP_CTL	0x0164	W	0x00000000	LLP Control Register

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Name	Offset	Size	Reset Value	Description
NANDC_LLP_STAT	0x0168	W	0x00000001	LLP Status Register
NANDC_INTEN	0x016c	W	0x00000000	NandC Interrupt Enable Register
NANDC_INTCLR	0x0170	W	0x00000000	NandC Interrupt Clear Register
NANDC_INTST	0x0174	W	0x00000000	NandC Interrupt Status Register
NANDC_SPARE0_0	0x0200	W	0x00000000	System Information for codeword 0
NANDC_SPARE0_1	0x0204	W	0x00000000	Spare Data and BCH Encode Information for codeword 0
NANDC_SPARE0_2	0x0208	W	0x00000000	Spare Data and BCH Encode Information for codeword 0
NANDC_SPARE0_3	0x020c	W	0x00000000	Spare Data and BCH Encode Information for codeword 0
NANDC_SPARE0_4	0x0210	W	0x00000000	Spare Data and BCH Encode Information for codeword 0
NANDC_SPARE0_5	0x0214	W	0x00000000	Spare Data and BCH Encode Information for codeword 0
NANDC_SPARE0_6	0x0218	W	0x00000000	Spare Data and BCH Encode Information for codeword 0
NANDC_SPARE0_7	0x021c	W	0x00000000	Spare Data and BCH Encode Information for codeword 0
NANDC_SPARE0_8	0x0220	W	0x00000000	Spare Data and BCH Encode Information for codeword 0
NANDC_SPARE0_9	0x0224	W	0x00000000	Spare Data and BCH Encode Information for codeword 0
NANDC_SPARE0_10	0x0228	W	0x00000000	Spare Data and BCH Encode Information for codeword 0
NANDC_SPARE0_11	0x022c	W	0x00000000	Spare Data and BCH Encode Information for codeword 0
NANDC_SPARE1_0	0x0230	W	0x00000000	System Information for codeword 1
NANDC_SPARE1_1	0x0234	W	0x00000000	Spare Data and BCH Encode Information for codeword 1
NANDC_SPARE1_2	0x0238	W	0x00000000	Spare Data and BCH Encode Information for codeword 1
NANDC_SPARE1_3	0x023c	W	0x00000000	Spare Data and BCH Encode Information for codeword 1
NANDC_SPARE1_4	0x0240	W	0x00000000	Spare Data and BCH Encode Information for codeword 1
NANDC_SPARE1_5	0x0244	W	0x00000000	Spare Data and BCH Encode Information for codeword 1
NANDC_SPARE1_6	0x0248	W	0x00000000	Spare Data and BCH Encode Information for codeword 1
NANDC_SPARE1_7	0x024c	W	0x00000000	Spare Data and BCH Encode Information for codeword 1

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Name	Offset	Size	Reset Value	Description
NANDC_SPARE1_8	0x0250	W	0x00000000	Spare Data and BCH Encode Information for codeword 1
NANDC_SPARE1_9	0x0254	W	0x00000000	Spare Data and BCH Encode Information for codeword 1
NANDC_SPARE1_10	0x0258	W	0x00000000	Spare Data and BCH Encode Information for codeword 1
NANDC_SPARE1_11	0x025c	W	0x00000000	Spare Data and BCH Encode Information for codeword 1
NANDC_SPARE0_12	0x0260	W	0x00000000	Spare Data and BCH Encode Information for codeword 0
NANDC_SPARE0_13	0x0264	W	0x00000000	Spare Data and BCH Encode Information for codeword 0
NANDC_SPARE0_14	0x0268	W	0x00000000	Spare Data and BCH Encode Information for codeword 0
NANDC_SPARE0_15	0x026c	W	0x00000000	Spare Data and BCH Encode Information for codeword 0
NANDC_SPARE0_16	0x0270	W	0x00000000	Spare Data and BCH Encode Information for codeword 0
NANDC_SPARE0_17	0x0274	W	0x00000000	Spare Data and BCH Encode Information for codeword 0
NANDC_SPARE0_18	0x0278	W	0x00000000	Spare Data and BCH Encode Information for codeword 0
NANDC_SPARE0_19	0x027c	W	0x00000000	Spare Data and BCH Encode Information for codeword 0
NANDC_SPARE0_20	0x0280	W	0x00000000	Spare Data and BCH Encode Information for codeword 0
NANDC_SPARE0_21	0x0284	W	0x00000000	Spare Data and BCH Encode Information for codeword 0
NANDC_SPARE0_22	0x0288	W	0x00000000	Spare Data and BCH Encode Information for codeword 0
NANDC_SPARE0_23	0x028c	W	0x00000000	Spare Data and BCH Encode Information for codeword 0
NANDC_SPARE0_24	0x0290	W	0x00000000	Spare Data and BCH Encode Information for codeword 0
NANDC_SPARE0_25	0x0294	W	0x00000000	Spare Data and BCH Encode Information for codeword 0
NANDC_SPARE0_26	0x0298	W	0x00000000	Spare Data and BCH Encode Information for codeword 0
NANDC_SPARE0_27	0x029c	W	0x00000000	Spare Data and BCH Encode Information for codeword 0
NANDC_SPARE1_12	0x02a0	W	0x00000000	Spare Data and BCH Encode Information for codeword 1
NANDC_SPARE1_13	0x02a4	W	0x00000000	Spare Data and BCH Encode Information for codeword 1

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Name	Offset	Size	Reset Value	Description
NANDC_SPARE1_14	0x02a8	W	0x00000000	Spare Data and BCH Encode Information for codeword 1
NANDC_SPARE1_15	0x02ac	W	0x00000000	Spare Data and BCH Encode Information for codeword 1
NANDC_SPARE1_16	0x02b0	W	0x00000000	Spare Data and BCH Encode Information for codeword 1
NANDC_SPARE1_17	0x02b4	W	0x00000000	Spare Data and BCH Encode Information for codeword 1
NANDC_SPARE1_18	0x02b8	W	0x00000000	Spare Data and BCH Encode Information for codeword 1
NANDC_SPARE1_19	0x02bc	W	0x00000000	Spare Data and BCH Encode Information for codeword 1
NANDC_SPARE1_20	0x02c0	W	0x00000000	Spare Data and BCH Encode Information for codeword 1
NANDC_SPARE1_21	0x02c4	W	0x00000000	Spare Data and BCH Encode Information for codeword 1
NANDC_SPARE1_22	0x02c8	W	0x00000000	Spare Data and BCH Encode Information for codeword 1
NANDC_SPARE1_23	0x02cc	W	0x00000000	Spare Data and BCH Encode Information for codeword 1
NANDC_SPARE1_24	0x02d0	W	0x00000000	Spare Data and BCH Encode Information for codeword 1
NANDC_SPARE1_25	0x02d4	W	0x00000000	Spare Data and BCH Encode Information for codeword 1
NANDC_SPARE1_26	0x02d8	W	0x00000000	Spare Data and BCH Encode Information for codeword 1
NANDC_SPARE1_27	0x02dc	W	0x00000000	Spare Data and BCH Encode Information for codeword 1
NANDC_BCHDE0_24	0x0400	W	0x00000000	BCH decode result of 24th error bit for codeword 0
NANDC_BCHDE0_25	0x0404	W	0x00000000	BCH decode result of 25th error bit for codeword 0
NANDC_BCHDE0_26	0x0408	W	0x00000000	BCH decode result of 26th error bit for codeword 0
NANDC_BCHDE0_27	0x040c	W	0x00000000	BCH decode result of 27th error bit for codeword 0
NANDC_BCHDE0_28	0x0410	W	0x00000000	BCH decode result of 28th error bit for codeword 0
NANDC_BCHDE0_29	0x0414	W	0x00000000	BCH decode result of 29th error bit for codeword 0
NANDC_BCHDE0_30	0x0418	W	0x00000000	BCH decode result of 30th error bit for codeword 0
NANDC_BCHDE0_31	0x041c	W	0x00000000	BCH decode result of 31th error bit for codeword 0

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Name	Offset	Size	Reset Value	Description
NANDC_BCHDE0_32	0x0420	W	0x00000000	BCH decode result of 32th error bit for codeword 0
NANDC_BCHDE0_33	0x0424	W	0x00000000	BCH decode result of 33th error bit for codeword 0
NANDC_BCHDE0_34	0x0428	W	0x00000000	BCH decode result of 3th error bit for codeword 0
NANDC_BCHDE0_35	0x042c	W	0x00000000	BCH decode result of 35th error bit for codeword 0
NANDC_BCHDE0_36	0x0430	W	0x00000000	BCH decode result of 36th error bit for codeword 0
NANDC_BCHDE0_37	0x0434	W	0x00000000	BCH decode result of 37th error bit for codeword 0
NANDC_BCHDE0_38	0x0438	W	0x00000000	BCH decode result of 38th error bit for codeword 0
NANDC_BCHDE0_39	0x043c	W	0x00000000	BCH decode result of 39th error bit for codeword 0
NANDC_BCHDE0_40	0x0440	W	0x00000000	BCH decode result of 40th error bit for codeword 0
NANDC_BCHDE0_41	0x0444	W	0x00000000	BCH decode result of 41th error bit for codeword 0
NANDC_BCHDE0_42	0x0448	W	0x00000000	BCH decode result of 42th error bit for codeword 0
NANDC_BCHDE0_43	0x044c	W	0x00000000	BCH decode result of 43th error bit for codeword 0
NANDC_BCHDE0_44	0x0450	W	0x00000000	BCH decode result of 44th error bit for codeword 0
NANDC_BCHDE0_45	0x0454	W	0x00000000	BCH decode result of 45th error bit for codeword 0
NANDC_BCHDE0_46	0x0458	W	0x00000000	BCH decode result of 46th error bit for codeword 0
NANDC_BCHDE0_47	0x045c	W	0x00000000	BCH decode result of 47th error bit for codeword 0
NANDC_BCHDE0_48	0x0460	W	0x00000000	BCH decode result of 48th error bit for codeword 0
NANDC_BCHDE0_49	0x0464	W	0x00000000	BCH decode result of 49th error bit for codeword 0
NANDC_BCHDE0_50	0x0468	W	0x00000000	BCH decode result of 50th error bit for codeword 0
NANDC_BCHDE0_51	0x046c	W	0x00000000	BCH decode result of 51th error bit for codeword 0
NANDC_BCHDE0_52	0x0470	W	0x00000000	BCH decode result of 52th error bit for codeword 0
NANDC_BCHDE0_53	0x0474	W	0x00000000	BCH decode result of 53th error bit for codeword 0

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Name	Offset	Size	Reset Value	Description
NANDC_BCHDE0_54	0x0478	W	0x00000000	BCH decode result of 54th error bit for codeword 0
NANDC_BCHDE0_55	0x047c	W	0x00000000	BCH decode result of 55th error bit for codeword 0
NANDC_BCHDE0_56	0x0480	W	0x00000000	BCH decode result of 56th error bit for codeword 0
NANDC_BCHDE0_57	0x0484	W	0x00000000	BCH decode result of 57th error bit for codeword 0
NANDC_BCHDE0_58	0x0488	W	0x00000000	BCH decode result of 58th error bit for codeword 0
NANDC_BCHDE0_59	0x048c	W	0x00000000	BCH decode result of 59th error bit for codeword 0
NANDC_BCHDE1_24	0x0490	W	0x00000000	BCH decode result of 24th error bit for codeword 1
NANDC_BCHDE1_25	0x0494	W	0x00000000	BCH decode result of 25th error bit for codeword 1
NANDC_BCHDE1_26	0x0498	W	0x00000000	BCH decode result of 26th error bit for codeword 1
NANDC_BCHDE1_27	0x049c	W	0x00000000	BCH decode result of 27th error bit for codeword 1
NANDC_BCHDE1_28	0x04a0	W	0x00000000	BCH decode result of 28th error bit for codeword 1
NANDC_BCHDE1_29	0x04a4	W	0x00000000	BCH decode result of 29th error bit for codeword 1
NANDC_BCHDE1_30	0x04a8	W	0x00000000	BCH decode result of 30th error bit for codeword 1
NANDC_BCHDE1_31	0x04ac	W	0x00000000	BCH decode result of 31th error bit for codeword 1
NANDC_BCHDE1_32	0x04b0	W	0x00000000	BCH decode result of 32th error bit for codeword 1
NANDC_BCHDE1_33	0x04b4	W	0x00000000	BCH decode result of 33th error bit for codeword 1
NANDC_BCHDE1_34	0x04b8	W	0x00000000	BCH decode result of 34th error bit for codeword 1
NANDC_BCHDE1_35	0x04bc	W	0x00000000	BCH decode result of 35th error bit for codeword 1
NANDC_BCHDE1_36	0x04c0	W	0x00000000	BCH decode result of 3th error bit for codeword 1
NANDC_BCHDE1_37	0x04c4	W	0x00000000	BCH decode result of 37th error bit for codeword 1
NANDC_BCHDE1_38	0x04c8	W	0x00000000	BCH decode result of 38th error bit for codeword 1
NANDC_BCHDE1_39	0x04cc	W	0x00000000	BCH decode result of 39th error bit for codeword 1

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Name	Offset	Size	Reset Value	Description
NANDC_BCHDE1_40	0x04d0	W	0x00000000	BCH decode result of 40th error bit for codeword 1
NANDC_BCHDE1_41	0x04d4	W	0x00000000	BCH decode result of 41th error bit for codeword 1
NANDC_BCHDE1_42	0x04d8	W	0x00000000	BCH decode result of 42th error bit for codeword 1
NANDC_BCHDE1_43	0x04dc	W	0x00000000	BCH decode result of 43th error bit for codeword 1
NANDC_BCHDE1_44	0x04e0	W	0x00000000	BCH decode result of 44th error bit for codeword 1
NANDC_BCHDE1_45	0x04e4	W	0x00000000	BCH decode result of 45th error bit for codeword 1
NANDC_BCHDE1_46	0x04e8	W	0x00000000	BCH decode result of 46th error bit for codeword 1
NANDC_BCHDE1_47	0x04ec	W	0x00000000	BCH decode result of 47th error bit for codeword 1
NANDC_BCHDE1_48	0x04f0	W	0x00000000	BCH decode result of 48th error bit for codeword 1
NANDC_BCHDE1_49	0x04f4	W	0x00000000	BCH decode result of 49th error bit for codeword 1
NANDC_BCHDE1_50	0x04f8	W	0x00000000	BCH decode result of 50th error bit for codeword 1
NANDC_BCHDE1_51	0x04fc	W	0x00000000	BCH decode result of 51th error bit for codeword 1
NANDC_BCHDE1_52	0x0500	W	0x00000000	BCH decode result of 52th error bit for codeword 1
NANDC_BCHDE1_53	0x0504	W	0x00000000	BCH decode result of 53th error bit for codeword 1
NANDC_BCHDE1_54	0x0508	W	0x00000000	BCH decode result of 54th error bit for codeword 1
NANDC_BCHDE1_55	0x050c	W	0x00000000	BCH decode result of 55th error bit for codeword 1
NANDC_BCHDE1_56	0x0510	W	0x00000000	BCH decode result of 56th error bit for codeword 1
NANDC_BCHDE1_57	0x0514	W	0x00000000	BCH decode result of 57th error bit for codeword 1
NANDC_BCHDE1_58	0x0518	W	0x00000000	BCH decode result of 58th error bit for codeword 1
NANDC_BCHDE1_59	0x051c	W	0x00000000	BCH decode result of 59th error bit for codeword 1

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

7.4.3 Detail Register Description

NANDC_FMCTL

Address: Operational Base + offset (0x0000)

Flash Interface Control Register

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Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15	RW	0x0	syn_mode Toggle enable signal, 1 active. 0: ONFI synchronous flash. 1: Toggle synchronous flash.
14	RW	0x0	syn_clken Synchronous flash clock enable signal, 1 active. Only available in Synchronous Mode. 0: flash clock is disabled. 1: flash clock is enabled.
13	RW	0x0	tm Timing mode indication. 0: Asynchronous Mode. 1: Synchronous Mode (Toggle or ONFI Synchronous).
12	RW	0x0	dwidth Flash data bus width indication. 0: 8bits, active in both Asynchronous Mode flash and Synchronous Mode flash. 1: reserved
11:10	RO	0x0	reserved
9	RO	0x1	frdy Flash ready/busy indicate signal. 0: flash is busy. 1: flash is ready. This bit is the sample of the pin of R/Bn.
8	RW	0x0	wp Flash write protect. 0: flash program/erase disabled. 1: flash program/erase enabled. This bit is output to the pin of WPn.
7:4	RW	0x0	reserved
3	RW	0x0	fcs3 Flash memory chip 3 select control. 1: hold flash memory chip select activity. 0: flash memory chip select activity free.
2	RW	0x0	fcs2 Flash memory chip 2 select control. 1: hold flash memory chip select activity. 0: flash memory chip select activity free.
1	RW	0x0	fcs1 Flash memory chip 1 select control. 1: hold flash memory chip select activity. 0: flash memory chip select activity free.

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Bit	Attr	Reset Value	Description
0	RW	0x0	fcs0 Flash memory chip 0 select control. 1: hold flash memory chip select activity. 0: flash memory chip select activity free.

NANDC_FMWAIT_ASYN

Address: Operational Base + offset (0x0004)

Flash Timing Control Register For Asynchronous Timing

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RW	0x0	fmw_dly_en fmw_dly enable signal,1 active
29:24	RW	0x3f	fmw_dly The number of delay cycle between two codeword transmission
23:18	RO	0x0	reserved
17:12	RW	0x3f	csrw When in Asynchronous mode or Toggle address/command mode, this field specifies the number of processor clock cycles from the falling edge of CSn to the falling edge of RDn or WRn. The min value of csrw is 0.
11	RW	0x0	hard_rdy Hardware handshaking controller bit. When asserted, an external device asserts signal "RDY" to extend a wait-state access and the rest bits in this register will be ignored
10:5	RW	0x3f	rwpw When in Asynchronous mode or Toggle address/command mode, this field specifies the width of RDn or WRn in processor clock cycles, 0x0<=rwpw<=0x3f.
4:0	RW	0x1f	rwcs When in Asynchronous mode or Toggle address/command mode, this field specifies the number of processor clock cycles from the rising edge of RDn or WRn to the rising edge of CSn, 0x0<=rwcs<=0x1f.

NANDC_FLCTL

Address: Operational Base + offset (0x0008)

Internal Transfer Control Register

Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
26:22	RW	0x00	page_num Transmission codeword number in internal DMA mode when bus-mode is master-mode 1~16: 1~16 codeword. default: not support. Notes: a. Only active in internal DMA mode b. Only active when bus-mode is master-mode
21	RW	0x0	page_size Transmission codeword size in internal DMA mode 0: 1024bytes/codeword 1: 512bytes/codeword
20	RO	0x1	tr_rdy Internal DMA transmission ready indication. 0: internal DMA transmission is busy 1: internal DMA transmission is ready When reading flash, tr_rdy should not be set to 1 until all data transmission and correct finished. When programing flash, tr_rdy should not be set to 1 until all data transmission finished. Notes: Only active in internal DMA mode.
19	RO	0x0	reserved
18:12	RW	0x00	spare_size Spare byte number when lba_en=1. 0<= spare_size<=109. When spare_size>=109, it is treated as 0. Notes: The spare_size must be even number when flash is ONFI Synchronous Flash or Asynchronous Flash with 16bits data width.
11	RW	0x0	lba_en LBA mode indication, 1 active. 0: NO-LBA mode, NandC should transfer both page data and spare data in every codeword, and the page size is 1024 bytes or 512 bytes determined by BCHCTL[16](bchpage), spare size is 32 bytes or 46 bytes determined by BCHCTL[4](bchmode). 1: LBA mode, NandC should transfer both page data and spare data in every codeword, and the page size is 1024 bytes or 512 bytes determined by FLCTL[21](page_size), spare size is determined by FLCTL[17:12](spare_size). Notes: a. When lba_en is active, BCH CODEC should be disabled, spare_size and page_size are configurable. b. When lba_en is active, cor_able is inactive.

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Bit	Attr	Reset Value	Description
10	RW	0x0	cor_able Auto correct enable indication, 1 active. 0: auto correct disable 1: auto correct enable Notes: a. Only active in internal DMA mode. b. lba_en is prior to cor_able. When lba_en=1, cor_able is ignored.
9:8	RO	0x0	reserved
7	RW	0x0	flash_st_mod Mode for NandC to start internal data transmission in internal DMA mode. 0: busy mode: hardware should not start internal data transmission until flash is ready even flash_st is asserted. 1: ready mode: hardware should start internal data transmission directly when flash_st is asserted. Notes: Only active in internal DMA mode.
6:5	RW	0x0	tr_count Transmission codeword number in internal DMA mode when bus-mode is slave-mode 00: 0 codeword need transferred 01: 1 codeword need transferred 10: 2 codeword need transferred 11: not supported Notes: a. Only active in internal DMA mode. b. Only active when bus-mode is slave-mode.
4	RW	0x0	st_addr Start buffer address. 0: start transfer from sram0 1: start transfer from sram1 Notes: Only active in internal DMA mode.
3	RW	0x0	bypass NandC internal DMA bypass indication. 0: bypass the internal DMA, data are transferred to/from flash by direct path. 1: internal DMA active, data are transferred to/from flash by internal DMA.

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Bit	Attr	Reset Value	Description
2	RW	0x0	flash_st Start signal for NandC to transfer data between flash and internal buffer in internal DMA mode. When asserted, it will auto cleared. 0: not start transmission 1: start transmission Notes: Only active in internal DMA mode
1	RW	0x0	flash_rdn Indicate data flow direction. 0: NandC read data from flash. 1: NandC write data to flash
0	RW	0x0	flash_rst NandC software reset indication. When asserted, it will auto cleared. 0: not software reset 1: software reset Notes: flash_rst is prior to flash_st

NANDC_BCHCTL
Address: Operational Base + offset (0x000c)
BCH Control Register

Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved
26:19	RW	0x00	bchthres BCH error number threshold
18	RW	0x0	bchmode1 High bit of BCH mode selection for 40bitBCH or 60bitBCH. BchMode=bchmode1, bchmode0: 00: 16bitBCH 01: 24bitBCH 10: 40bitBCH 11: 60bitBCH
17	RO	0x0	reserved
16	RW	0x0	bchpage The data size indication when BCH is active. 0: 1024 bytes, all the 1024 bytes data in codeword are valid data to be transferred. 1: 512 bytes, 1th~512th bytes in codeword are valid data to be transferred, and 513th~1024th in codeword are invalid data stuffed with 0xff. Notes: a. Only active when data transferred in internal DMA mode. b. Only active for asynchronous flash.

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Bit	Attr	Reset Value	Description
15:8	RW	0x00	addr BCH active range selection. BCH should be active when access in range address.
7:5	RW	0x0	region BCH active region selection indication. 000: Flash memory 0 region (flash 0) 001: Flash memory 1 region (flash 1) 010: Flash memory 2 region (flash 2) 011: Flash memory 3 region (flash 3) 100: Flash memory 4 region (flash 4) 101: Flash memory 5 region (flash 5) 110: Flash memory 6 region (flash 6) 111: Flash memory 7 region (flash 7)
4	RW	0x0	bchmode0 BCH mode selection indication. BCH mode is determined by both bchmode0 and bchmode1,detailed information is showed in BCHCTL[18].
3	RW	0x1	bchepd BCH encoder/decoder power down indication. 0: BCH encoder/decoder working. 1: BCH encoder/decoder not working
2	RW	0x0	mode_addrcare BCH address care mode selection indication. 0: address care 1: address not care. Notes: This bit is just active for data transmission in bypass mode, but not for command and address transmission.
1	RO	0x0	reserved
0	RW	0x0	bchrst BCH software reset indication, When asserted, it will auto cleared. 0: not software reset 1: software reset Notes: a. BCH Decoder should be software reset before decode begin. b. bch software reset should be used with nandc software reset at the same time.

NANDC_MTRANS_CFG

Address: Operational Base + offset (0x0010)

Bus Transfer Configuration Register

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
15	W1C	0x0	ahb_rst ahb master interface software reset, auto cleared
14	RW	0x0	fl_pwd Flash power down indication, 1 active. 0: Flash power on, data transferred through master interface is data that to be written into or read from flash. 1: Flash power down, data transferred through master interface is not data that to be written into or read from flash. NandC is just used as DMA for external memory and internal memory.
13:9	RW	0x00	incr_num AHB Master incr num indication. incr_num=1~16. When burst=001, software should configure incr_num. Notes: Only active for master-mode.
8:6	RW	0x7	burst AHB Master burst type indication: 000 : Single transfer 011 : 4-beat burst 101 : 8-beat Burst 111 : 16-beat burst default : not supported Notes: Only active for master-mode.
5:3	RW	0x2	hsize AHB Master data size indication: 000 : 8 bits 001 : 16 bits 010 : 32 bits default : not supported Notes: Only active for master-mode.
2	RW	0x0	bus_mode Bus interface selection. 0: Slave interface, flash data is transferred through slave interface 1: Master interface, flash data is transferred through master interface

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Bit	Attr	Reset Value	Description
1	RW	0x0	ahb_wr Data transfer direction through master interface. 0: read direction(internal memory ->external memory) 1: write direction (internal memory->external memory) Notes: a. Only active for master-mode. b. When read flash(flash_rdn=0), ahb_wr=1; when program flash(flash_rdn=1), ahb_wr=0.
0	W1C	0x0	ahb_wr_st Start indication for loading data from external memory to internal memory or storing data from internal memory to external memory through master. When asserted, it will auto cleared. Notes: a. Only active for master-mode and fl_pwd=1. b. When fl_pwd=0, flash is active, NandC start to transfer data through master interface if flash_st=1 c. When fl_pwd=1, flash is not active, NandC start to transfer data through master interface if ahb_wr_st=1

NANDC_MTRANS_SADDR0
Address: Operational Base + offset (0x0014)
Start Address Register For Page Data Transmission

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	saddr0 Start address for page data transmission. Notes: a. Only active for master-mode. b. Should be aligned with hsize in MTRANS_CFG[5:3].

NANDC_MTRANS_SADDR1
Address: Operational Base + offset (0x0018)
Start Address Register For Spare Data Transmission

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	saddr1 Start address for spare data. Notes: a. Only active for master-mode. b. Should be aligned with hsize in MTRANS_CFG[5:3].

NANDC_MTRANS_STAT
Address: Operational Base + offset (0x001c)
Bus Transfer Status Register

Bit	Attr	Reset Value	Description
31:21	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
20:16	RO	0x00	mtrans_cnt finished counter for codeword transmission through Master interface Notes: Only active for master-mode.
15:0	RO	0x0000	bus_err Bus error indication for codeword0~15. [0] : bus error for codeword 0 …… [15] : bus error for codeword 15 Notes: Only active for master-mode.

NANDC_BCHST0
Address: Operational Base + offset (0x0020)
BCH Status Register For Codeword 0~1

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RO	0x0	err_hnum1_h1 Highest bit of err_hnum1
29	RO	0x0	err_tnum1_h1 Highest bit of err_tnum1
28	RO	0x0	err_hnum0_h1 Highest bit of err_hnum0
27	RO	0x0	err_tnum0_h1 Highest bit of err_tnum0
26	RO	0x1	bchrdy Ready indication for bch encoder/decoder, 1 active. 0: bch encoder/decoder is busy 1: bch encoder/decoder is ready
25:21	RO	0x00	err_hnum1_l5 Lower 5 bits of number of error bits found in first 512bytes of 1st backup codeword
20:16	RO	0x00	err_tnum1_l5 Lower 5 bits of number of error bits found in 1st backup codeword
15	RO	0x0	fail1 Indication for the 1st backup codeword decoded failed or not. 0: decode successfully 1: decode fail
14	RO	0x0	done1 Indication for finishing decoding the 1st backup codeword 0: not finished 1: finished

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Bit	Attr	Reset Value	Description
13	RO	0x0	errf1 Indication for error found in 1st backup codeword. 0: no error 1: error found
12:8	RO	0x00	err_hnum0_l5 Lower 5 bits of number of error bits found in first 512bytes of current backup codeword
7:3	RO	0x00	err_tnum0_l5 Lower 5 bits of number of error bits found in current backup codeword
2	RO	0x0	fail0 Indication for current backup codeword decode failed or not 0: decode successfully 1: decode fail
1	RO	0x0	done0 Indication for finishing decoding the current backup codeword. 0: not finished 1: finished
0	RO	0x0	errf0 Indication for error found in current backup codeword. 0: no error 1: error found

NANDC_BCHST1
Address: Operational Base + offset (0x0024)
BCH Status Register For Codeword 2~3

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RO	0x0	err_hnum3_h1 Highest bit of err_hnum3
29	RO	0x0	err_tnum3_h1 Highest bit of err_tnum3
28	RO	0x0	err_hnum2_h1 Highest bit of err_hnum2
27	RO	0x0	err_tnum2_h1 Highest bit of err_tnum2
26	RO	0x0	reserved
25:21	RO	0x00	err_hnum3_l5 Lower 5 bits of number of error bits found in first 512bytes of 3th backup codeword
20:16	RO	0x00	err_tnum3_l5 Lower 5 bits of number of error bits found in 3th backup codeword

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Bit	Attr	Reset Value	Description
15	RO	0x0	fail3 Indication for the 3th backup codeword decoded failed or not. 0: decode successfully 1: decode fail
14	RO	0x0	done3 Indication for finishing decoding the 3th backup codeword 0: not finished 1: finished
13	RO	0x0	errf3 Indication for error found in 3th backup codeword. 0: no error 1: error found
12:8	RO	0x00	err_hnum2_l5 Lower 5 bits of number of error bits found in first 512bytes of 2th backup codeword
7:3	RO	0x00	err_tnum2_l5 Lower 5 bits of number of error bits found in 2th backup codeword
2	RO	0x0	fail2 Indication for 2th backup codeword decode failed or not 0: decode successfully 1: decode fail
1	RO	0x0	done2 Indication for finishing decoding the 2th backup codeword. 0: not finished 1: finished
0	RO	0x0	errf2 Indication for error found in 2th backup codeword. 0: no error 1: error found

NANDC_BCHST2
Address: Operational Base + offset (0x0028)
BCH Status Register For Codeword 4~5

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	bchst_cwd4_cwd5 BCHST information for 4th and 5th backup codeword. Bit assignment is similar to BCHST1 register. For more description, please refer to BCHST1 register.

NANDC_BCHST3
Address: Operational Base + offset (0x002c)
BCH Status Register For Codeword 6~7

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	bchst_cwd6_cwd7 BCHST information for 6th and 7th backup codeword. Bit assignment is similar to BCHST1 register. For more description, please refer to BCHST1 register.

NANDC_BCHST4
Address: Operational Base + offset (0x0030)
BCH Status Register For Codeword 8~9

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	bchst_cwd8_cwd9 BCHST information for 8th and 9th backup codeword. Bit assignment is similar to BCHST1 register. For more description, please refer to BCHST1 register.

NANDC_BCHST5
Address: Operational Base + offset (0x0034)
BCH Status Register For Codeword 10~11

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	bchst_cwd10_cwd11 BCHST information for 10th and 11th backup codeword. Bit assignment is similar to BCHST1 register. For more description, please refer to BCHST1 register.

NANDC_BCHST6
Address: Operational Base + offset (0x0038)
BCH Status Register For Codeword 12~13

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	bchst_cwd12_cwd13 BCHST information for 12th and 13th backup codeword. Bit assignment is similar to BCHST1 register. For more description, please refer to BCHST1 register.

NANDC_BCHST7
Address: Operational Base + offset (0x003c)
BCH Status Register For Codeword 14~15

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	bchst_cwd14_cwd15 BCHST information for 14th and 15th backup codeword. Bit assignment is similar to BCHST1 register. For more description, please refer to BCHST1 register.

NANDC_BCHLOC0
Address: Operational Base + offset (0x0040)
BCH Error Bit Location Number Register For Codeword 0~5

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Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:25	RO	0x00	err_loc5_l5 Lower 5 bits of number of 8bit error location in 5th backup codeword
24:20	RO	0x00	err_loc4_l5 Lower 5 bits of number of 8bit error location in 4th backup codeword
19:15	RO	0x00	err_loc3_l5 Lower 5 bits of number of 8bit error location in 3rd backup codeword
14:10	RO	0x00	err_loc2_l5 Lower 5 bits of number of 8bit error location in 2nd backup codeword
9:5	RO	0x00	err_loc1_l5 Lower 5 bits of number of 8bit error location in 1st backup codeword
4:0	RO	0x00	err_loc0_l5 Lower 5 bits of number of 8bit error location in current backup codeword

NANDC_BCHLOC1

Address: Operational Base + offset (0x0044)

BCH Error Bit Location Number Register For Codeword 6~11

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:25	RO	0x00	err_loc11_l5 Lower 5 bits of number of 8bit error location in 11th backup codeword
24:20	RO	0x00	err_loc10_l5 Lower 5 bits of number of 8bit error location in 10th backup codeword
19:15	RO	0x00	err_loc9_l5 Lower 5 bits of number of 8bit error location in 9th backup codeword
14:10	RO	0x00	err_loc8_l5 Lower 5 bits of number of 8bit error location in 8th backup codeword
9:5	RO	0x00	err_loc7_l5 Lower 5 bits of number of 8bit error location in 7th backup codeword
4:0	RO	0x00	err_loc6_l5 Lower 5 bits of number of 8bit error location in 6th backup codeword

NANDC_BCHLOC2

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Address: Operational Base + offset (0x0048)
BCH Error Bit Location Number Register For Codeword12~15

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:15	RO	0x00	err_loc15_l5 Lower 5 bits of number of 8bit error location in 15th backup codeword
14:10	RO	0x00	err_loc14_l5 Lower 5 bits of number of 8bit error location in 4th backup codeword
9:5	RO	0x00	err_loc13_l5 Lower 5 bits of number of 8bit error location in 13th backup codeword
4:0	RO	0x00	err_loc12_l5 Lower 5 bits of number of 8bit error location in 12th backup codeword

NANDC_BCHLOC3
Address: Operational Base + offset (0x004c)
Highest Bit For BCH Error Bit Location Number Register

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15	RO	0x0	err_loc15_h1 High bit for numbers of 8bit error location in 15th codeword
14	RO	0x0	err_loc14_h1 High bit for numbers of 8bit error location in 14th codeword
13	RO	0x0	err_loc13_h1 High bit for numbers of 8bit error location in 13th codeword
12	RO	0x0	err_loc12_h1 High bit for numbers of 8bit error location in 12th codeword
11	RO	0x0	err_loc11_h1 High bit for numbers of 8bit error location in 11th codeword
10	RO	0x0	err_loc10_h1 High bit for numbers of 8bit error location in 10th codeword
9	RO	0x0	err_loc9_h1 High bit for numbers of 8bit error location in 9th codeword
8	RO	0x0	err_loc8_h1 High bit for numbers of 8bit error location in 8th codeword
7	RO	0x0	err_loc7_h1 High bit for numbers of 8bit error location in 7th codeword
6	RO	0x0	err_loc6_h1 High bit for numbers of 8bit error location in 6th codeword
5	RO	0x0	err_loc5_h1 High bit for numbers of 8bit error location in 5th codeword
4	RO	0x0	err_loc4_h1 High bit for numbers of 8bit error location in 4th codeword

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Bit	Attr	Reset Value	Description
3	RO	0x0	err_loc3_h1 High bit for numbers of 8bit error location in 3th codeword
2	RO	0x0	err_loc2_h1 High bit for numbers of 8bit error location in 2th codeword
1	RO	0x0	err_loc1_h1 High bit for numbers of 8bit error location in 1th codeword
0	RO	0x0	err_loc0_h1 High bit for numbers of 8bit error location in 0th codeword

NANDC_BCHDE0_0
Address: Operational Base + offset (0x0070)
BCH decode result of 0th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:8	RO	0x000	offset The offset byte address of the error bit. The value is 11bit, which is the byte offset address in the codeword. The address can be divided into different part for different use, showed as follows. 0 ~1023: page data 1024~1027: system information 1028~1055: bch information for 16bitBCH 1028~1069: bch information for 24bitBCH 1028~1097: bch information for 40bitBCH 1028~1132: bch information for 60bitBCH
7:0	RO	0x00	err_val The error value of corresponding error byte

NANDC_BCHDE0_1
Address: Operational Base + offset (0x0074)
BCH decode result of 1th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_1 decode result of 1th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_2
Address: Operational Base + offset (0x0078)
BCH decode result of 2th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
18:0	RO	0x00000	bchde0_2 decode result of 2th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_3
Address: Operational Base + offset (0x007c)
BCH decode result of 3th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_3 decode result of 3th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_4
Address: Operational Base + offset (0x0080)
BCH decode result of 4th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_4 decode result of 4th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_5
Address: Operational Base + offset (0x0084)
BCH decode result of 5th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_5 decode result of 5th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_6
Address: Operational Base + offset (0x0088)
BCH decode result of 6th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_6 decode result of 6th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

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NANDC_BCHDE0_7
Address: Operational Base + offset (0x008c)
BCH decode result of 7th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_7 decode result of 7th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_8
Address: Operational Base + offset (0x0090)
BCH decode result of 8th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_8 decode result of 8th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_9
Address: Operational Base + offset (0x0094)
BCH decode result of 9th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_9 decode result of 9th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_10
Address: Operational Base + offset (0x0098)
BCH decode result of 10th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_10 decode result of 10th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_11
Address: Operational Base + offset (0x009c)
BCH decode result of 11th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
18:0	RO	0x00000	bchde0_11 decode result of 11th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_12
Address: Operational Base + offset (0x00a0)
BCH decode result of 12th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_12 decode result of 12th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_13
Address: Operational Base + offset (0x00a4)
BCH decode result of 13th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_13 decode result of 13th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_14
Address: Operational Base + offset (0x00a8)
BCH decode result of 14th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_14 decode result of 14th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_15
Address: Operational Base + offset (0x00ac)
BCH decode result of 15th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_15 decode result of 15th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

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NANDC_BCHDE0_16
Address: Operational Base + offset (0x00b0)
BCH decode result of 16th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_16 decode result of 16th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_17
Address: Operational Base + offset (0x00b4)
BCH decode result of 17th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_17 decode result of 17th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_18
Address: Operational Base + offset (0x00b8)
BCH decode result of 18th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_18 decode result of 18th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_19
Address: Operational Base + offset (0x00bc)
BCH decode result of 19th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_19 decode result of 1th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_20
Address: Operational Base + offset (0x00c0)
BCH decode result of 20th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
18:0	RO	0x00000	bchde0_20 decode result of 20th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_21
Address: Operational Base + offset (0x00c4)
BCH decode result of 21th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_21 decode result of 21th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_22
Address: Operational Base + offset (0x00c8)
BCH decode result of 22th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_22 decode result of 22th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_23
Address: Operational Base + offset (0x00cc)
BCH decode result of 23th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_23 decode result of 23th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE1_0
Address: Operational Base + offset (0x00d0)
BCH decode result of 0th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
18:8	RO	0x000	offset The offset byte address of the error bit. The value is 11bit, which is the byte offset address in the codeword. The address can be divided into different part for different use, showed as follows. 0 ~1023: page data 1024~1027: system information 1028~1055: bch information for 16bitBCH 1028~1069: bch information for 24bitBCH 1028~1097: bch information for 40bitBCH 1028~1132: bch information for 60bitBCH
7:0	RO	0x00	err_val The error value of corresponding error byte

NANDC_BCHDE1_1
Address: Operational Base + offset (0x00d4)
BCH decode result of 1th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_1 decode result of 1th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_2
Address: Operational Base + offset (0x00d8)
BCH decode result of 2th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_2 decode result of 2th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_3
Address: Operational Base + offset (0x00dc)
BCH decode result of 3th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_3 decode result of 3th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

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NANDC_BCHDE1_4
Address: Operational Base + offset (0x00e0)
BCH decode result of 4th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_4 decode result of 4th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_5
Address: Operational Base + offset (0x00e4)
BCH decode result of 5th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_5 decode result of 5th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_6
Address: Operational Base + offset (0x00e8)
BCH decode result of 6th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_6 decode result of 6th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_7
Address: Operational Base + offset (0x00ec)
BCH decode result of 7th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_7 decode result of 7th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_8
Address: Operational Base + offset (0x00f0)
BCH decode result of 8th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
18:0	RO	0x00000	bchde1_8 decode result of 8th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_9
Address: Operational Base + offset (0x00f4)
BCH decode result of 9th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_9 decode result of 9th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_10
Address: Operational Base + offset (0x00f8)
BCH decode result of 10th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_10 decode result of 10th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_11
Address: Operational Base + offset (0x00fc)
BCH decode result of 11th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_11 decode result of 11th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_12
Address: Operational Base + offset (0x0100)
BCH decode result of 12th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_12 decode result of 12th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

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NANDC_BCHDE1_13
Address: Operational Base + offset (0x0104)
BCH decode result of 13th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_13 decode result of 13th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_14
Address: Operational Base + offset (0x0108)
BCH decode result of 14th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_14 decode result of 14th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_15
Address: Operational Base + offset (0x010c)
BCH decode result of 15th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_15 decode result of 15th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_16
Address: Operational Base + offset (0x0110)
BCH decode result of 16th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_16 decode result of 16th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_17
Address: Operational Base + offset (0x0114)
BCH decode result of 17th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
18:0	RO	0x00000	bchde1_17 decode result of 17th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_18
Address: Operational Base + offset (0x0118)
BCH decode result of 1th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_18 decode result of 18th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_19
Address: Operational Base + offset (0x011c)
BCH decode result of 19th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_19 decode result of 19th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_20
Address: Operational Base + offset (0x0120)
BCH decode result of 20th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_20 decode result of 20th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_21
Address: Operational Base + offset (0x0124)
BCH decode result of 21th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_21 decode result of 21th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

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NANDC_BCHDE1_22
Address: Operational Base + offset (0x0128)
BCH decode result of 22th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_22 decode result of 22th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_23
Address: Operational Base + offset (0x012c)
BCH decode result of 23th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_23 decode result of 23th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_DLL_CTL_REG0
Address: Operational Base + offset (0x0130)
DLL Control Register 0

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:16	RW	0x00	dll_dqs_dly_bypass Holds the read DQS delay setting when the DLL is operating in bypass mode.
15:8	RW	0x00	dll_dqs_dly Holds the read DQS delay setting when the DLL is operating in normal mode. Typically, this value is 1/4 of a clock cycle. Each increment of this field represents 1/128th of a clock cycle.
7:0	RW	0x00	dll_start_point DLL Start Point Control. This value is loaded into the DLL at initialization and is the value at which the DLL will begin searching for a lock. Each increment of this field represents 1/128th of a clock cycle.

NANDC_DLL_CTL_REG1
Address: Operational Base + offset (0x0134)
DLL Control Register 1

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
11:4	RW	0x00	dll_incr DLL Increment Value. This sets the increment used by the DLL when searching for a lock. It is recommended keeping this field small (around 0x4) to keep the steps gradual
3:2	RW	0x0	dll_qtren Quarter flag of DLL, active in no-bypass mode. 01:1/4 fclk, dqs_dly=128. 10:1/8 fclk, dqs_dly=64. Default: dqs_dly=dll_dqs_dly(DLL_CTL_REG0[15:8]). When dll_qtr='b01 or 'b10, software not need to configure dll_dqs_dly , and hardware should delay the input signal for 1/4 or 1/8 fclk cycle time; When dll_qtr=0, software need to configure dll_dqs_dly
1	RW	0x0	dll_bypass DLL Bypass Control, 1active 0: dll not bypass, dll_dqs_dleay= dqs_dly 1: dll bypass, dll_dqs_dleay= dll_dqs_dly_bypass
0	RW	0x0	dll_start Start signal for DLL, 1 active. Notes: It will keep high until dll disabled.

NANDC_DLL_OBS_REG0
Address: Operational Base + offset (0x0138)
DLL Status Register

Bit	Attr	Reset Value	Description
31:17	RO	0x0	reserved
16:9	RO	0x00	dll_dqs_delay_value Report the delay value for the read DQS signal
8:1	RO	0x01	dll_lock_value Reports the DLL encoder value from the master DLL to the slave DLL's. The slaves use this value to set up their delays for the clk_wr and read DQS signals.
0	RO	0x0	dll_lock DLL Lock indication: 0: DLL has not locked 1: DLL is locked.

NANDC_RANDMZ_CFG
Address: Operational Base + offset (0x0150)
Randomizer Configure Register

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Bit	Attr	Reset Value	Description
31	RW	0x0	randmz_en Randomizer enable indication, 1 active. 0: Randomizer active 1: Randomizer not active Notes: a. Not active when data transmission in bypass mode. b. Just active for data, but not for address and command. c. Not active when BchPage=1.
30	RW	0x0	randmz_mode Randomizer mode: 0- Polynomial=1+x^18+x^23 1- Polynomial=1+x^14+x^15
29:23	RO	0x0	reserved
22:0	RW	0x000000	randmz_seed The seed for randomizer(initial value)

NANDC_FMWAIT_SYN
Address: Operational Base + offset (0x0158)
Flash Timing Control RegisterFor Synchronous Timing

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18	RW	0x0	ssyn_xle_sel ALE/CLE selection signal for ONFI synchronous flash: 0: ALE/CLE aligned to the falling edge of WRN 1: ALE/CLE aligned to the center of WRN low level
17:15	RO	0x0	reserved
14:9	RW	0x02	pst Write/Read Postamble time for ONFI synchronous mode or Toggle data mode. When write, this field specifies the number of processor clock cycles from last falling edge of valid DQSo to valid DQSi, determined by flash When read, this field specifies the number of processor clock cycles from valid RDn to valid DQSi, determined by flash
8:3	RW	0x02	pre Write/Read Preamble time for ONFI synchronous mode or Toggle data mode. This field specifies the number of processor clock cycles from valid RDn to valid DQSi, determined by flash
2:0	RW	0x1	fclk Half hclk cycle number for flash clock for ONFI synchronous mode or Toggle data mode

NANDC_NANDC_VER
Address: Operational Base + offset (0x0160)

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Nandc Version Register

Bit	Attr	Reset Value	Description
31:0	RO	0x56363030	version Version indication for NANDC

NANDC_LLP_CTL

Address: Operational Base + offset (0x0164)

LLP Control Register

Bit	Attr	Reset Value	Description
31:6	RW	0x0000000	llp_loc Starting address for LLI0, 64byte align
5:3	RO	0x0	reserved
2	RW	0x0	llp_rst Reset signal for LLP. When asserted, it will auto cleared.
1	RW	0x0	llp_mode 0- current LLI only has FOP 1-current LLI has both CFG and FOP
0	RW	0x0	llp_en Enable signal for LLP 0-LLP disable 1-LLP enable

NANDC_LLP_STAT

Address: Operational Base + offset (0x0168)

LLP Status Register

Bit	Attr	Reset Value	Description
31:6	RO	0x0000000	llp_stat latest LLI_LOC finished, 64byte align
5:2	RO	0x0	reserved
1	RO	0x0	llp_err error status for llp load or execute 0-llp is correct 1-llp is error
0	RO	0x1	llp_rdy ready status for all llp load 0-llp load is busy 1-llp load is ready

NANDC_INTEN

Address: Operational Base + offset (0x016c)

NandC Interrupt Enable Register

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
3	RW	0x0	bchfail_int_en Enable for bch fail interrupt. 0-interrupt disable 1-interrupt enable When bchfail_int_en is active, an interrupt is generated if bch decode failed
2	RW	0x0	bcherr_int_en Enable for bch error interrupt. 0-interrupt disable 1-interrupt enable When bcherr_int_en is active, an interrupt is generated if bch decode error bit is larger than bchthres(BCHCTL[26:19])
1	RW	0x0	frdy_int_en Enable for flash_rdy interrupt 0-interrupt disable 1-interrupt enable When frdy_int_en is active, an interrupt is generated if flash R/B# changes from 0 to 1
0	RW	0x0	dma_int_en Enable for internal DMA transfer finished interrupt 0-interrupt disable 1-interrupt enable When dma_int_en is active, an interrupt is generated if page_num(FLCTL[26:22]) of flash data transfer in DMA mode is finished

NANDC_INTCLR
Address: Operational Base + offset (0x0170)
NandC Interrupt Clear Register

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3	RW	0x0	bchfail_int_clr Clear for bch decode fail interrupt. When asserted, this bit will be auto cleared. 0-interrupt cleared 1-interrupt not cleared
2	RW	0x0	bcherr_int_clr Clear for bch error interrupt. When asserted, this bit will be auto cleared. 0-interrupt cleared 1-interrupt not cleared

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Bit	Attr	Reset Value	Description
1	RW	0x0	frdy_int_clr Clear for flash_rdy interrupt. When asserted, this bit will be auto cleared. 0-interrupt cleared 1-interrupt not cleared
0	RW	0x0	dma_int_clr Clear for internal DMA transfer finished interrupt. When asserted, this bit will be auto cleared. 0-interrupt cleared 1-interrupt not cleared

NANDC_INTST
Address: Operational Base + offset (0x0174)
NandC Interrupt Status Register

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3	RO	0x0	bchfail_int_stat Status for bch decode fail interrupt, high active
2	RO	0x0	bcherr_int_stat Status for bch error interrupt, high active
1	RO	0x0	frdy_int_stat Status for flash_rdy interrupt, high active
0	RO	0x0	dma_int_stat Status for internal DMA transfer finished interrupt, high active

NANDC_SPARE0_0
Address: Operational Base + offset (0x0200)
System Information for codeword 0

Bit	Attr	Reset Value	Description
31:24	RW	0x00	system_3 the 4th system byte of codeword 0
23:16	RW	0x00	system_2 the 3rd system byte of codeword 0
15:8	RW	0x00	system_1 the 2nd system byte of codeword 0
7:0	RW	0x00	system_0 the 1st system byte of codeword 0

NANDC_SPARE0_1
Address: Operational Base + offset (0x0204)
Spare Data and BCH Encode Information for codeword 0

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Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH0_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH0_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH0_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH0_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE0_2
Address: Operational Base + offset (0x0208)
Spare Data and BCH Encode Information for codeword 0

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH0_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH0_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25

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Bit	Attr	Reset Value	Description
15:8	RW	0x00	BCH0_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH0_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE0_3
Address: Operational Base + offset (0x020c)
Spare Data and BCH Encode Information for codeword 0

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH0_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH0_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH0_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH0_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE0_4
Address: Operational Base + offset (0x0210)
Spare Data and BCH Encode Information for codeword 0

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Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH0_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH0_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH0_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH0_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE0_5
Address: Operational Base + offset (0x0214)
Spare Data and BCH Encode Information for codeword 0

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH0_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH0_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25

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Bit	Attr	Reset Value	Description
15:8	RW	0x00	BCH0_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH0_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE0_6
Address: Operational Base + offset (0x0218)
Spare Data and BCH Encode Information for codeword 0

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH0_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH0_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH0_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH0_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE0_7
Address: Operational Base + offset (0x021c)
Spare Data and BCH Encode Information for codeword 0

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Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH0_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH0_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH0_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH0_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE0_8
Address: Operational Base + offset (0x0220)
Spare Data and BCH Encode Information for codeword 0

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH0_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH0_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25

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Bit	Attr	Reset Value	Description
15:8	RW	0x00	BCH0_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH0_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE0_9
Address: Operational Base + offset (0x0224)
Spare Data and BCH Encode Information for codeword 0

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH0_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH0_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH0_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH0_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE0_10
Address: Operational Base + offset (0x0228)
Spare Data and BCH Encode Information for codeword 0

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Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH0_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH0_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH0_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH0_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE0_11
Address: Operational Base + offset (0x022c)
Spare Data and BCH Encode Information for codeword 0

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH0_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH0_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25

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Bit	Attr	Reset Value	Description
15:8	RW	0x00	BCH0_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH0_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE1_0
Address: Operational Base + offset (0x0230)
System Information for codeword 1

Bit	Attr	Reset Value	Description
31:24	RW	0x00	system_3 the 4th system byte of codeword 1
23:16	RW	0x00	system_2 the 3rd system byte of codeword 1
15:8	RW	0x00	system_1 the 2nd system byte of codeword 1
7:0	RW	0x00	system_0 the 1st system byte of codeword 1

NANDC_SPARE1_1
Address: Operational Base + offset (0x0234)
Spare Data and BCH Encode Information for codeword 1

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH1_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH1_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25

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Bit	Attr	Reset Value	Description
15:8	RW	0x00	BCH1_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH1_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE1_2
Address: Operational Base + offset (0x0238)
Spare Data and BCH Encode Information for codeword 1

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH1_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH1_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH1_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH1_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE1_3
Address: Operational Base + offset (0x023c)
Spare Data and BCH Encode Information for codeword 1

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Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH1_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH1_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH1_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH1_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE1_4
Address: Operational Base + offset (0x0240)
Spare Data and BCH Encode Information for codeword 1

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH1_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH1_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25

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Bit	Attr	Reset Value	Description
15:8	RW	0x00	BCH1_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH1_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE1_5
Address: Operational Base + offset (0x0244)
Spare Data and BCH Encode Information for codeword 1

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH1_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH1_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH1_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH1_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE1_6
Address: Operational Base + offset (0x0248)
Spare Data and BCH Encode Information for codeword 1

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Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH1_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH1_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH1_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH1_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE1_7
Address: Operational Base + offset (0x024c)
Spare Data and BCH Encode Information for codeword 1

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH1_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH1_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25

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Bit	Attr	Reset Value	Description
15:8	RW	0x00	BCH1_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH1_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE1_8
Address: Operational Base + offset (0x0250)
Spare Data and BCH Encode Information for codeword 1

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH1_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH1_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH1_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH1_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE1_9
Address: Operational Base + offset (0x0254)
Spare Data and BCH Encode Information for codeword 1

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Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH1_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH1_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH1_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH1_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE1_10
Address: Operational Base + offset (0x0258)
Spare Data and BCH Encode Information for codeword 1

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH1_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH1_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25

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Bit	Attr	Reset Value	Description
15:8	RW	0x00	BCH1_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH1_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE1_11
Address: Operational Base + offset (0x025c)
Spare Data and BCH Encode Information for codeword 1

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH1_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH1_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH1_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH1_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE0_12
Address: Operational Base + offset (0x0260)
Spare Data and BCH Encode Information for codeword 0

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Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH0_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH0_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH0_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH0_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE0_13
Address: Operational Base + offset (0x0264)
Spare Data and BCH Encode Information for codeword 0

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH0_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH0_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25

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Bit	Attr	Reset Value	Description
15:8	RW	0x00	BCH0_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH0_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE0_14
Address: Operational Base + offset (0x0268)
Spare Data and BCH Encode Information for codeword 0

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH0_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH0_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH0_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH0_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE0_15
Address: Operational Base + offset (0x026c)
Spare Data and BCH Encode Information for codeword 0

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Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH0_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH0_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH0_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH0_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE0_16
Address: Operational Base + offset (0x0270)
Spare Data and BCH Encode Information for codeword 0

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH0_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH0_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25

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Bit	Attr	Reset Value	Description
15:8	RW	0x00	BCH0_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH0_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE0_17
Address: Operational Base + offset (0x0274)
Spare Data and BCH Encode Information for codeword 0

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH0_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH0_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH0_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH0_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE0_18
Address: Operational Base + offset (0x0278)
Spare Data and BCH Encode Information for codeword 0

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Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH0_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH0_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH0_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH0_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE0_19
Address: Operational Base + offset (0x027c)
Spare Data and BCH Encode Information for codeword 0

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH0_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH0_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25

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Bit	Attr	Reset Value	Description
15:8	RW	0x00	BCH0_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH0_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE0_20
Address: Operational Base + offset (0x0280)
Spare Data and BCH Encode Information for codeword 0

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH0_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH0_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH0_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH0_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE0_21
Address: Operational Base + offset (0x0284)
Spare Data and BCH Encode Information for codeword 0

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Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH0_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH0_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH0_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH0_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE0_22
Address: Operational Base + offset (0x0288)
Spare Data and BCH Encode Information for codeword 0

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH0_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH0_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25

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Bit	Attr	Reset Value	Description
15:8	RW	0x00	BCH0_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH0_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE0_23
Address: Operational Base + offset (0x028c)
Spare Data and BCH Encode Information for codeword 0

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH0_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH0_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH0_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH0_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE0_24
Address: Operational Base + offset (0x0290)
Spare Data and BCH Encode Information for codeword 0

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Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH0_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH0_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH0_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH0_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE0_25
Address: Operational Base + offset (0x0294)
Spare Data and BCH Encode Information for codeword 0

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH0_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH0_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25

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Bit	Attr	Reset Value	Description
15:8	RW	0x00	BCH0_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH0_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE0_26
Address: Operational Base + offset (0x0298)
Spare Data and BCH Encode Information for codeword 0

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH0_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH0_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH0_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH0_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE0_27
Address: Operational Base + offset (0x029c)
Spare Data and BCH Encode Information for codeword 0

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Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH0_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH0_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH0_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH0_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE1_12
Address: Operational Base + offset (0x02a0)
Spare Data and BCH Encode Information for codeword 1

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH1_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH1_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25

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Bit	Attr	Reset Value	Description
15:8	RW	0x00	BCH1_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH1_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE1_13
Address: Operational Base + offset (0x02a4)
Spare Data and BCH Encode Information for codeword 1

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH1_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH1_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH1_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH1_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE1_14
Address: Operational Base + offset (0x02a8)
Spare Data and BCH Encode Information for codeword 1

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Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH1_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH1_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH1_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH1_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE1_15
Address: Operational Base + offset (0x02ac)
Spare Data and BCH Encode Information for codeword 1

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH1_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH1_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25

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Bit	Attr	Reset Value	Description
15:8	RW	0x00	BCH1_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH1_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE1_16
Address: Operational Base + offset (0x02b0)
Spare Data and BCH Encode Information for codeword 1

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH1_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH1_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH1_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH1_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE1_17
Address: Operational Base + offset (0x02b4)
Spare Data and BCH Encode Information for codeword 1

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Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH1_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH1_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH1_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH1_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE1_18
Address: Operational Base + offset (0x02b8)
Spare Data and BCH Encode Information for codeword 1

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH1_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH1_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25

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Bit	Attr	Reset Value	Description
15:8	RW	0x00	BCH1_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH1_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE1_19
Address: Operational Base + offset (0x02bc)
Spare Data and BCH Encode Information for codeword 1

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH1_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH1_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH1_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH1_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE1_20
Address: Operational Base + offset (0x02c0)
Spare Data and BCH Encode Information for codeword 1

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Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH1_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH1_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH1_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH1_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE1_21
Address: Operational Base + offset (0x02c4)
Spare Data and BCH Encode Information for codeword 1

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH1_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH1_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25

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Bit	Attr	Reset Value	Description
15:8	RW	0x00	BCH1_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH1_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE1_22
Address: Operational Base + offset (0x02c8)
Spare Data and BCH Encode Information for codeword 1

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH1_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH1_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH1_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH1_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE1_23
Address: Operational Base + offset (0x02cc)
Spare Data and BCH Encode Information for codeword 1

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Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH1_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH1_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH1_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH1_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE1_24
Address: Operational Base + offset (0x02d0)
Spare Data and BCH Encode Information for codeword 1

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH1_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH1_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25

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Bit	Attr	Reset Value	Description
15:8	RW	0x00	BCH1_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH1_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE1_25
Address: Operational Base + offset (0x02d4)
Spare Data and BCH Encode Information for codeword 1

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH1_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH1_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH1_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH1_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE1_26
Address: Operational Base + offset (0x02d8)
Spare Data and BCH Encode Information for codeword 1

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Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH1_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH1_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
15:8	RW	0x00	BCH1_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH1_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_SPARE1_27
Address: Operational Base + offset (0x02dc)
Spare Data and BCH Encode Information for codeword 1

Bit	Attr	Reset Value	Description
31:24	RW	0x00	BCH1_4x_3 (4x+3)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25
23:16	RW	0x00	BCH1_4x_2 (4x+2)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~9 40bitBCH: x=0~16 60bitBCH: x=0~25

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Bit	Attr	Reset Value	Description
15:8	RW	0x00	BCH1_4x_1 (4x+1)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~25
7:0	RW	0x00	BCH1_4x_0 (4x+0)th byte of bch spare bits 16bitBCH: x=0~6 24bitBCH: x=0~10 40bitBCH: x=0~17 60bitBCH: x=0~26

NANDC_BCHDE0_24
Address: Operational Base + offset (0x0400)
BCH decode result of 24th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_24 decode result of 24th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_25
Address: Operational Base + offset (0x0404)
BCH decode result of 25th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_25 decode result of 25th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_26
Address: Operational Base + offset (0x0408)
BCH decode result of 26th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_26 decode result of 26th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_27
Address: Operational Base + offset (0x040c)

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BCH decode result of 27th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_27 decode result of 27th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_28
Address: Operational Base + offset (0x0410)
BCH decode result of 28th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_28 decode result of 28th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_29
Address: Operational Base + offset (0x0414)
BCH decode result of 29th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_29 decode result of 29th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_30
Address: Operational Base + offset (0x0418)
BCH decode result of 30th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_30 decode result of 30th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_31
Address: Operational Base + offset (0x041c)
BCH decode result of 31th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
18:0	RO	0x00000	bchde0_31 decode result of 31th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_32
Address: Operational Base + offset (0x0420)
BCH decode result of 32th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_3 decode result of 3th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_33
Address: Operational Base + offset (0x0424)
BCH decode result of 33th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_33 decode result of 33th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_34
Address: Operational Base + offset (0x0428)
BCH decode result of 3th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_34 decode result of 34th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_35
Address: Operational Base + offset (0x042c)
BCH decode result of 35th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_35 decode result of 35th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

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NANDC_BCHDE0_36
Address: Operational Base + offset (0x0430)
BCH decode result of 36th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_36 decode result of 36th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_37
Address: Operational Base + offset (0x0434)
BCH decode result of 37th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_37 decode result of 37th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_38
Address: Operational Base + offset (0x0438)
BCH decode result of 38th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_38 decode result of 38th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_39
Address: Operational Base + offset (0x043c)
BCH decode result of 39th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_39 decode result of 39th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_40
Address: Operational Base + offset (0x0440)
BCH decode result of 40th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
18:0	RO	0x00000	bchde0_40 decode result of 40th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_41
Address: Operational Base + offset (0x0444)
BCH decode result of 41th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_41 decode result of 41th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_42
Address: Operational Base + offset (0x0448)
BCH decode result of 42th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_42 decode result of 4th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_43
Address: Operational Base + offset (0x044c)
BCH decode result of 43th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_43 decode result of 43th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_44
Address: Operational Base + offset (0x0450)
BCH decode result of 44th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_44 decode result of 44th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

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NANDC_BCHDE0_45
Address: Operational Base + offset (0x0454)
BCH decode result of 45th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_45 decode result of 45th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_46
Address: Operational Base + offset (0x0458)
BCH decode result of 46th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_46 decode result of 46th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_47
Address: Operational Base + offset (0x045c)
BCH decode result of 47th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_47 decode result of 47th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_48
Address: Operational Base + offset (0x0460)
BCH decode result of 48th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_48 decode result of 48th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_49
Address: Operational Base + offset (0x0464)
BCH decode result of 49th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
18:0	RO	0x00000	bchde0_49 decode result of 49th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_50
Address: Operational Base + offset (0x0468)
BCH decode result of 50th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_50 decode result of 50th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_51
Address: Operational Base + offset (0x046c)
BCH decode result of 51th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_51 decode result of 51th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_52
Address: Operational Base + offset (0x0470)
BCH decode result of 52th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_52 decode result of 52th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_53
Address: Operational Base + offset (0x0474)
BCH decode result of 53th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_53 decode result of 53th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

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NANDC_BCHDE0_54
Address: Operational Base + offset (0x0478)
BCH decode result of 54th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_54 decode result of 54th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_55
Address: Operational Base + offset (0x047c)
BCH decode result of 55th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_55 decode result of 55th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_56
Address: Operational Base + offset (0x0480)
BCH decode result of 56th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_56 decode result of 56th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_57
Address: Operational Base + offset (0x0484)
BCH decode result of 57th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_57 decode result of 57th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_58
Address: Operational Base + offset (0x0488)
BCH decode result of 58th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
18:0	RO	0x00000	bchde0_58 decode result of 58th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE0_59
Address: Operational Base + offset (0x048c)
BCH decode result of 59th error bit for codeword 0

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde0_59 decode result of 59th error bit for codeword 0. Bit assignment is similar to BCHDE0_0 register. For more description, please refer to BCHDE0_0 register.

NANDC_BCHDE1_24
Address: Operational Base + offset (0x0490)
BCH decode result of 24th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_24 decode result of 24th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_25
Address: Operational Base + offset (0x0494)
BCH decode result of 25th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_25 decode result of 25th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_26
Address: Operational Base + offset (0x0498)
BCH decode result of 26th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_26 decode result of 26th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

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NANDC_BCHDE1_27
Address: Operational Base + offset (0x049c)
BCH decode result of 27th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_27 decode result of 27th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_28
Address: Operational Base + offset (0x04a0)
BCH decode result of 28th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_28 decode result of 28th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_29
Address: Operational Base + offset (0x04a4)
BCH decode result of 29th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_29 decode result of 2th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_30
Address: Operational Base + offset (0x04a8)
BCH decode result of 30th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_30 decode result of 30th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_31
Address: Operational Base + offset (0x04ac)
BCH decode result of 31th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
18:0	RO	0x00000	bchde1_31 decode result of 31th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_32
Address: Operational Base + offset (0x04b0)
BCH decode result of 32th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_32 decode result of 32th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_33
Address: Operational Base + offset (0x04b4)
BCH decode result of 33th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_33 decode result of 33th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_34
Address: Operational Base + offset (0x04b8)
BCH decode result of 34th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_34 decode result of 34th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_35
Address: Operational Base + offset (0x04bc)
BCH decode result of 35th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_35 decode result of 35th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

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NANDC_BCHDE1_36
Address: Operational Base + offset (0x04c0)
BCH decode result of 3th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_36 decode result of 36th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_37
Address: Operational Base + offset (0x04c4)
BCH decode result of 37th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_37 decode result of 37th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_38
Address: Operational Base + offset (0x04c8)
BCH decode result of 38th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_38 decode result of 38th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_39
Address: Operational Base + offset (0x04cc)
BCH decode result of 39th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_39 decode result of 39th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_40
Address: Operational Base + offset (0x04d0)
BCH decode result of 40th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
18:0	RO	0x00000	bchde1_40 decode result of 40th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_41
Address: Operational Base + offset (0x04d4)
BCH decode result of 41th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_41 decode result of 41th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_42
Address: Operational Base + offset (0x04d8)
BCH decode result of 42th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_42 decode result of 42th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_43
Address: Operational Base + offset (0x04dc)
BCH decode result of 43th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_43 decode result of 43th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_44
Address: Operational Base + offset (0x04e0)
BCH decode result of 44th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_44 decode result of 44th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

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NANDC_BCHDE1_45
Address: Operational Base + offset (0x04e4)
BCH decode result of 45th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_45 decode result of 45th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_46
Address: Operational Base + offset (0x04e8)
BCH decode result of 46th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_46 decode result of 46th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_47
Address: Operational Base + offset (0x04ec)
BCH decode result of 47th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_47 decode result of 47th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_48
Address: Operational Base + offset (0x04f0)
BCH decode result of 48th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_48 decode result of 48th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_49
Address: Operational Base + offset (0x04f4)
BCH decode result of 49th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
18:0	RO	0x00000	bchde1_49 decode result of 49th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_50
Address: Operational Base + offset (0x04f8)
BCH decode result of 50th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_50 decode result of 50th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_51
Address: Operational Base + offset (0x04fc)
BCH decode result of 51th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_51 decode result of 51th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_52
Address: Operational Base + offset (0x0500)
BCH decode result of 52th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_52 decode result of 52th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_53
Address: Operational Base + offset (0x0504)
BCH decode result of 53th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_53 decode result of 53th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

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NANDC_BCHDE1_54
Address: Operational Base + offset (0x0508)
BCH decode result of 54th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_54 decode result of 54th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_55
Address: Operational Base + offset (0x050c)
BCH decode result of 55th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_55 decode result of 55th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_56
Address: Operational Base + offset (0x0510)
BCH decode result of 56th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_56 decode result of 56th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_57
Address: Operational Base + offset (0x0514)
BCH decode result of 57th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_57 decode result of 57th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_58
Address: Operational Base + offset (0x0518)
BCH decode result of 58th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
18:0	RO	0x00000	bchde1_58 decode result of 58th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

NANDC_BCHDE1_59
Address: Operational Base + offset (0x051c)
BCH decode result of 59th error bit for codeword 1

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	bchde1_59 decode result of 59th error bit for codeword 1. Bit assignment is similar to BCHDE1_0 register. For more description, please refer to BCHDE1_0 register.

7.5 Interface Description

Table 7-2 NandC Interface Description

Module Pin	IO	Pad Name	IOMUX Setting
flash_wp	O	IO_NANDwp_EMMCpwren_GPIO2a5	GPIO2A_IOMUX[11:10]= 2'b01
flash_ale	O	IO_NANDale_SPI1clk_GPIO2a0	GPIO2A_IOMUX[1:0]= 2'b01
flash_cle	O	IO_NANDcle_GPIO2a1	GPIO2A_IOMUX[3:2]= 2'b01
flash_wrn	O	IO_NANDwrn_SFCcsn0_GPIO2a2	GPIO2A_IOMUX[5:4]= 2'b01
flash_rdn	O	IO_NANDrdn_SFCcsn1_GPIO2a3	GPIO2A_IOMUX[7:6]= 2'b01
flash_dqs	I/O	IO_NANDdqs_EMMCclkout_GPIO2a7	GPIO2A_IOMUX[15:14]= 2'b01
flash_rdy	I	IO_NANDrdy_EMMCcmd1_SFCclk_GPIO2a4	GPIO2A_IOMUX[9:8]= 2'b01
flash_csn0	O	IO_NANDcs0_GPIO2a6	GPIO2A_IOMUX[12]= 1'b1
flash_csn1	O	IO_NANDcs1_GPIO0c7	GPIO0C_IOMUX[14]= 1'b1
flash_csn2	O	IO_NANDcs2_EMMCcmd_GPIO1c6	GPIO1C_IOMUX[13:12]= 2'b01
flash_csn3	O	IO_NANDcs3_EMMCrstnout_GPIO1c7	GPIO1C_IOMUX[15:14]= 2'b01
flash_data0	I/O	IO_NANDd0_EMMCd0_SFCd0_GPIO1d0	GPIO1D_IOMUX[1:0]= 2'b01
flash_data1	I/O	IO_NANDd1_EMMCd1_SFCd1_GPIO1d1	GPIO1D_IOMUX[3:2]= 2'b01
flash_data2	I/O	IO_NANDd2_EMMCd2_SFCd2_GPIO1d2	GPIO1D_IOMUX[5:4]= 2'b01
flash_data3	I/O	IO_NANDd3_EMMCd3_SFCd3_GPIO1d3	GPIO1D_IOMUX[7:6]= 2'b01
flash_data4	I/O	IO_NANDd4_EMMCd4_SPI1rxd1_GPIO1d4	GPIO1D_IOMUX[9:8]= 2'b01
flash_data5	I/O	IO_NANDd5_EMMCd5_SPI1txd1_GPIO1d5	GPIO1D_IOMUX[11:10]= 2'b01
flash_data6	I/O	IO_NANDd6_EMMCd6_SPI1csn0_GPIO1d6	GPIO1D_IOMUX[13:12]= 2'b01
flash_data7	I/O	IO_NANDd7_EMMCd7_SPI1csn1_GPIO1d7	GPIO1D_IOMUX[15:14]= 2'b01

Notes: I=input, O=output, I/O=input/output, bidirectional

Furthermore, different IOs are selected and connected to different flash interface, which is shown as follows.

Table 7-3 NandC Interface Connection

Module Pin	Direction	Flash Interface		
		Asyn8x	ONFI	Toggle
flash_csni(i=0~3)	O	√	√	√
flash_wp	O	√	√	√
flash_ale	O	√	√	√
flash_cle	O	√	√	√
flash_wrn	O	√	√	√
flash_rdn	O	√	√	√
flash_data[7:0]	I/O	√	√	√
flash_dqs	I/O	-	√	√
flash_rdy	I	√	√	√

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7.6 Application Notes

7.6.1 Clock Description

There are two clock domains in the NandC. One is hclk, and the other is nclk.

- AHB slave bus uses the hclk to configure the NandC registers.
- AHB master bus uses the hclk to transmit the data between the external memory and internal sram.
- NandC use nclk to transmit the data between the nand flash and internal sram.

All the flash interface timing configuration is relative to the nclk.

7.6.2 BCHST/BCHLOC/BCHDE/SPARE Application

1. BCHST

There are 16 BCHST-registers in NandC to store 32 codeword's BCH decode status(bchst) information. Every register stores 2 codeword's bchst information except BCHST0, which not only includes bchst information, but also includes one bit for *bchrdy*.

Let bchst_cwd0~bchst_cwd31 be the bchst information for 32 codewords. In BCHST-registers, the latest codeword's bchst is stored into bchst_cwd0, and the former is shifted into bchst_cwd1. That is, bchst_cwd0→ bchst_cwd1 →……→bchst_cwd31. Therefore, for example, if 32 codewords are decoded, then bchst_cwd0 is the bch decode status for codeword31, and bchst_cwd31 is the bch decode status for codeword0.

bchst_cwd0 = {BCHST0[28],BCHST0[12:8],BCHST0[27],BCHST0[7:3],BCHST0[2:0]}
bchst_cwd1 = {BCHST0[30],BCHST0[25:21],BCHST0[29],BCHST0[20:16],BCHST0[15:13]} bchst_cwd2 = {BCHST1[28],BCHST1[12:8],BCHST1[27],BCHST1[7:3],BCHST1[2:0]} bchst_cwd3 = {BCHST1[30],BCHST1[25:21],BCHST1[29],BCHST1[20:16],BCHST1[15:13]} bchst_cwd4 = {BCHST2[28],BCHST2[12:8] ,BCHST2[27],BCHST2[7:3],BCHST2[2:0]} bchst_cwd5 = {BCHST2[30],BCHST2[25:21],BCHST2[29],BCHST2[20:16],BCHST2[15:13]} bchst_cwd6 = {BCHST3[28],BCHST3[12:8] ,BCHST3[27],BCHST3[7:3],BCHST3[2:0]} bchst_cwd7 = {BCHST3[30],BCHST3[25:21],BCHST3[29],BCHST3[20:16],BCHST3[15:13]} bchst_cwd8 = {BCHST4[28],BCHST4[12:8] ,BCHST4[27],BCHST4[7:3],BCHST4[2:0]} bchst_cwd9 = {BCHST4[30],BCHST4[25:21],BCHST4[29],BCHST4[20:16],BCHST4[15:13]}
bchst_cwd10 = {BCHST5[28],BCHST5[12:8] ,BCHST5[27],BCHST5[7:3],BCHST5[2:0]}
bchst_cwd11 = {BCHST5[30],BCHST5[25:21],BCHST5[29],BCHST5[20:16],BCHST5[15:13]}
bchst_cwd12 = {BCHST6[28],BCHST6[12:8] ,BCHST6[27],BCHST6[7:3],BCHST6[2:0]}
bchst_cwd13 = {BCHST6[30],BCHST6[25:21],BCHST6[29],BCHST6[20:16],BCHST6[15:13]}
bchst_cwd14 = {BCHST7[28],BCHST7[12:8] ,BCHST7[27],BCHST7[7:3],BCHST7[2:0]}
bchst_cwd15 = {BCHST7[30],BCHST7[25:21],BCHST7[29],BCHST7[20:16],BCHST7[15:13]}
bchst_cwd16 = {BCHST8[28],BCHST8[12:8],BCHST8[27],BCHST8[7:3],BCHST8[2:0]}
bchst_cwd17 = {BCHST8[30],BCHST8[25:21],BCHST8[29],BCHST8[20:16],BCHST8[15:13]}
bchst_cwd18 = {BCHST9[28],BCHST9[12:8],BCHST9[27],BCHST9[7:3],BCHST9[2:0]}
bchst_cwd19 = {BCHST9[30],BCHST9[25:21],BCHST9[29],BCHST9[20:16],BCHST9[15:13]}
bchst_cwd20 = {BCHST10[28],BCHST10[12:8] ,BCHST10[27],BCHST10[7:3],BCHST10[2:0]}
bchst_cwd21 = {BCHST10[30],BCHST10[25:21],BCHST10[29],BCHST10[20:16],BCHST10[15:13]}
bchst_cwd22 = {BCHST11[28],BCHST11[12:8] ,BCHST11[27],BCHST11[7:3],BCHST11[2:0]}
bchst_cwd23 = {BCHST11[30],BCHST11[25:21],BCHST11[29],BCHST11[20:16],BCHST11[15:13]}
bchst_cwd24 = {BCHST12[28],BCHST12[12:8] ,BCHST12[27],BCHST12[7:3],BCHST12[2:0]}
bchst_cwd25 = {BCHST12[30],BCHST12[25:21],BCHST12[29],BCHST12[20:16],BCHST12[15:13]}

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bchst_cwd26 =
{BCHST13[28],BCHST13[12:8] ,BCHST13[27],BCHST13[7:3],BCHST13[2:0]}
bchst_cwd27 =
{BCHST13[30],BCHST13[25:21],BCHST13[29],BCHST13[20:16],BCHST13[15:13]}
bchst_cwd28 =
{BCHST14[28],BCHST14[12:8] ,BCHST14[27],BCHST14[7:3],BCHST14[2:0]}
bchst_cwd29 =
{BCHST14[30],BCHST14[25:21],BCHST14[29],BCHST14[20:16],BCHST14[15:13]}
bchst_cwd30 =
{BCHST15[28],BCHST15[12:8] ,BCHST15[27],BCHST15[7:3],BCHST15[2:0]}
bchst_cwd31 =
{BCHST15[30],BCHST15[25:21],BCHST15[29],BCHST15[20:16],BCHST15[15:13]}

2. BCHLOC

There are 7 BCHLOC-registers in NandC to store 32 codeword's bch decode location(bchloc) information.

Let bchloc_cwd0~bchloc_cwd31 be the bchloc information for the 32 codeword. In BCHLOC registers, the latest codeword's bchloc is stored into bchloc_cwd0, and the former is shifted into bchloc_cwd1. That is, bchloc_cwd0→bchloc_cwd1→……→bchloc_cwd31. Therefore, for example, if 32 codeword are decoded, then bchloc_cwd0 is the bch decode status for codeword31, and bchloc_cwd31 is the bch decode status for codeword0.

bchloc_cwd0 = {BCHLOC6[0], BCHLOC0[4:0]}
bchloc_cwd1 = {BCHLOC6[1], BCHLOC0[9:5]}
bchloc_cwd2 = {BCHLOC6[2], BCHLOC0[14:10]}
bchloc_cwd3 = {BCHLOC6[3], BCHLOC0[19:15]}
bchloc_cwd4 = {BCHLOC6[4], BCHLOC0[24:20]}
bchloc_cwd5 = {BCHLOC6[5], BCHLOC0[29:25]}
bchloc_cwd6 = {BCHLOC6[6], BCHLOC1[4:0]}
bchloc_cwd7 = {BCHLOC6[7], BCHLOC1[9:5]}
bchloc_cwd8 = {BCHLOC6[8], BCHLOC1[14:10]}
bchloc_cwd9 = {BCHLOC6[9], BCHLOC1[19:15]}
bchloc_cwd10 = {BCHLOC6[10], BCHLOC1[24:20]}
bchloc_cwd11 = {BCHLOC6[11], BCHLOC1[29:25]}
bchloc_cwd12 = {BCHLOC6[12], BCHLOC2[4:0]}
bchloc_cwd13 = {BCHLOC6[13], BCHLOC2[9:5]}
bchloc_cwd14 = {BCHLOC6[14], BCHLOC2[14:10]}
bchloc_cwd15 = {BCHLOC6[15], BCHLOC2[19:15]}
bchloc_cwd16 = {BCHLOC6[16], BCHLOC2[24:20]}
bchloc_cwd17 = {BCHLOC6[17], BCHLOC2[29:25]}
bchloc_cwd18 = {BCHLOC6[18], BCHLOC3[4:0]}
bchloc_cwd19 = {BCHLOC6[19], BCHLOC3[9:5]}
bchloc_cwd20 = {BCHLOC6[20], BCHLOC3[14:10]}
bchloc_cwd21 = {BCHLOC6[21], BCHLOC3[19:15]}
bchloc_cwd22 = {BCHLOC6[22], BCHLOC3[24:20]}
bchloc_cwd23 = {BCHLOC6[23], BCHLOC3[29:25]}
bchloc_cwd24 = {BCHLOC6[24], BCHLOC4[4:0]}
bchloc_cwd25 = {BCHLOC6[25], BCHLOC4[9:5]}
bchloc_cwd26 = {BCHLOC6[26], BCHLOC4[14:10]}
bchloc_cwd27 = {BCHLOC6[27], BCHLOC4[19:15]}
bchloc_cwd28 = {BCHLOC6[28], BCHLOC4[24:20]}
bchloc_cwd29 = {BCHLOC6[29], BCHLOC4[29:25]}
bchloc_cwd30 = {BCHLOC6[30], BCHLOC5[4:0]}
bchloc_cwd31 = {BCHLOC6[31], BCHLOC5[9:5]}

3. BCHDE

BCHDE includes two register-groups, BCHDE0 and BCHDE1. Each group has 60 registers: BCHDE0_0~BCHDE0_59 and BCHDE1_0~BCHDE1_59. BCHDE0_n(n=0~59) is the decode information of the nth error bit for codeword in sram0, and BCHDE1_n(n=0~59) is the decode information of the nth error bit for codeword in sram1.

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The needed number of BCHDE registers is determined by bchmode. That is:
a. When 16bitBCH selected, BCHDEm_0 ~ BCHDEm_15 are available
b. When 24bitBCH selected, BCHDEm_0 ~ BCHDEm_23 are available
c. When 40bitBCH selected, BCHDEm_0 ~ BCHDEm_39 are available
d. When 60bitBCH selected, BCHDEm_0 ~ BCHDEm_59 are available

4. SPARE

SPARE includes two register-groups, SPARE0 and SPARE1. Each group has 28 registers: SPARE0_0~SPARE0_27 and SPARE1_0~SPARE1_27.
When in bch encoding, SPARE0_0 stores system information for codeword in sram0, SPARE0_n(n=1~27) stores encode information for codeword in sram0; SPARE1_0 stores system information for codeword in sram1, SPARE1_n(n=1~27) stores encode information for codeword in sram1.
When in bch decoding, SPARE0_n(n=0~27) stores the spare data read from flash for codeword in sram0; SPARE1_n(n=0~27) stores the spare data read from flash for codeword in sram1.
The needed number of BCHDE registers is determined by bchmode. That is:
a. When 16bitBCH selected, spare data=28bytes, SPAREm_0~SPAREm_7 are available
b. When 24bitBCH selected, spare data=42bytes, SPAREm_0~SPAREm_10 and SPAREm_11[15:0] are available
c. When 40bitBCH selected, spare data=70bytes, SPAREm_0~SPAREm_17 and SPAREm_18[15:0] are available
d. When 60bitBCH selected, spare data=105bytes, SPAREm_0~SPAREm_26 and SPAREm_27[7:0] are available

7.6.3 Bus Mode Application

MTRANS_CFG[2] determines whether the data load/store between internal memory and external memory is through slave interface or master interface.

1. Slave Mode

When MTRANS_CFG[2]=0, slave is selected. i. e. , flash data load/store between internal memory and external memory is through slave interface by cpu or external DMA.
In this mode, software should store page data into internal memory and spare data into SPARE registers before starting flash program operation; and should load page data from internal memory and spare data from SPARE registers after finishing flash read operation.
In this mode, MTRANS_CFG, MTRANS_SADDR0 and MTRANS_SADDR1 are unused. The transfer codeword number is determined by FLCTL[6:5], and the maximum number is 2.
The judgment condition for finishing data transfer is FLCTL[20]. When FLCTL[20] is high, it means that data transfer is finished.

2. Master Mode

When MTRANS_CFG[2]=1, master is selected. i. e. , flash data load/store between internal memory and external memory is through master interface.
In this mode, software should initialize page data and spare data into external memory, and set their addresses in MTRANS_SADDR0 and MTRANS_SADDR1 respectively before starting flash program operation. Similarly, software should configure MTRANS_SADDR0 and MTRANS_SADDR1 respectively before starting flash read operation and could read data from addresses in MTRANS_SADDR0 and MTRANS_SADDR1 after NandC transfer finish.
In this mode, MTRANS_CFG, MTRANS_SADDR0 and MTRANS_SADDR1 are used. The transfer codeword number is determined by FLCTL[26:22], and the maximum number is 16.
The judgment condition for finishing data transfer is FLCTL[20]. When FLCTL[20] is high, it means that data transmission is finished.
When MTRANS_CFG[2]=1, page data and spare data are stored in the continuous space of external memory respectively.
For page data, source address is named Saddr0, specified in MTRANS_SADDR0. The space can be divided into many continuous units, and the unit size(named PUnit) is 1024 bytes or 512 bytes determined by FLCTL[21] and FLCTL[11]:
a. when FLCTL[11]=0, PUnit is always equal to 1024 bytes
b. when FLCTL[11]=1 and FLCTL[21]=0, PUnit is equal to 1024 bytes
c. when FLCTL[11]=1 and FLCTL[21]=1, PUnit is equal to 512 bytes

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For spare data, source address is named Saddr1, specified in MTRANS_SADDR1. The space can be divided into many continuous units, and the unit size(named SUnit) is 64 bytes or 128 bytes determined by BCHCTL[18], FLCTL[11] and FLCTL[21]:

a. When FLCTL[11]=0 and BCHCTL[18]=0, SUnit is equal to 64 bytes
b. When FLCTL[11]=0 and BCHCTL[18]=1, SUnit is equal to 128 bytes
c. When FLCTL[11]=1 and FLCTL[21]=0, SUnit is equal to 128 bytes
d. When FLCTL[11]=1 and FLCTL[21]=1, SUnit is equal to 64 bytes

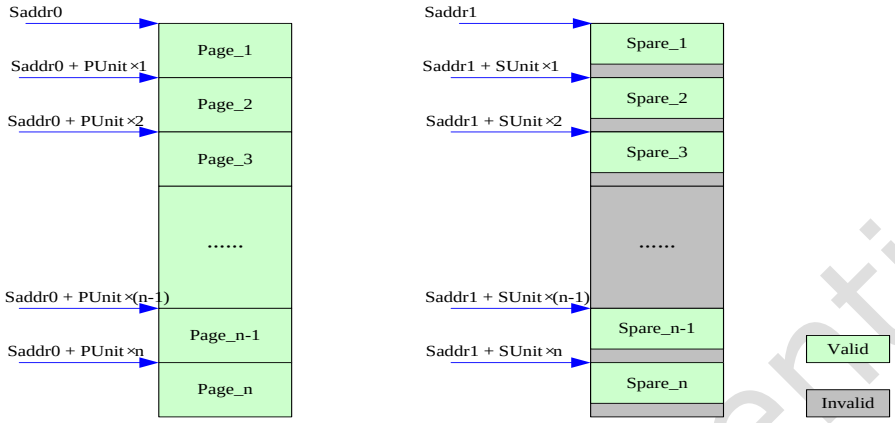


Fig. 7-2 NandC Address Assignment

The detailed format for page data and spare data in every unit is shown in following figures.

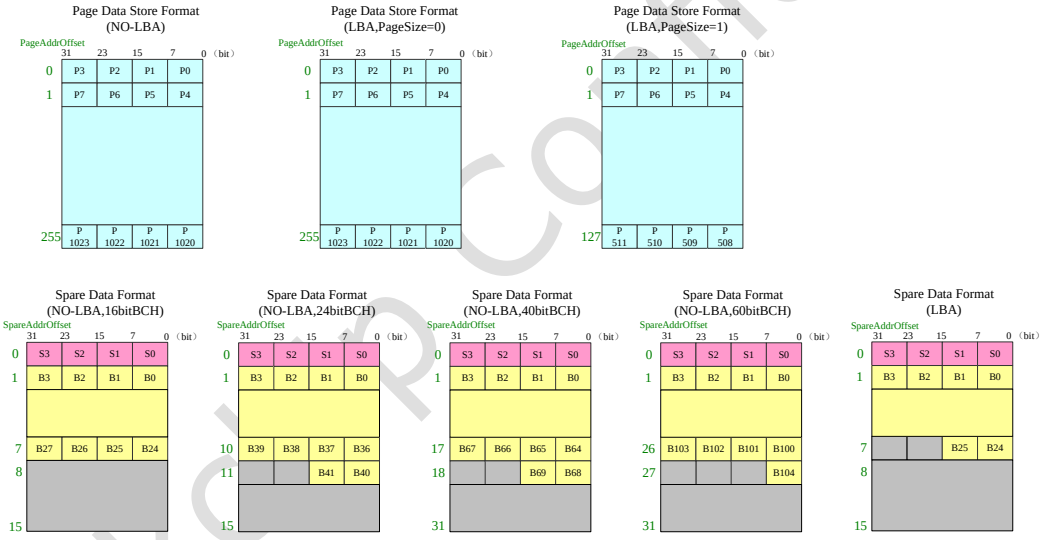


Fig. 7-3 NandC Data Format

7.6.4 BchPage Application

BCHCTL[16] determines whether codeword size for page data is 1024 bytes or 512 bytes when FLCTL[11] is 0.

1. 1024bytes

When BCHCTL[16]=0, BchPage=0, hardware needs to write 1024 bytes page data and spare data into flash or read 1024 bytes page data and spare data from flash. All the 1024 bytes page data and spare data are encoded when writing or decoded when reading.

2. 512bytes

When BCHCTL[16]=1, BchPage=1, hardware needs to write 512 bytes page data and spare data into flash or read 512 bytes page data and spare data from flash.

In this mode, the page data unit size for BCH encoder and BCH decoder still is 1024byte. So to support BCH encoder and decoder, software should configure page data as follows: 1th~512th bytes are invalid data which must be stuffed with 0xff, 513th~1024th bytes arevalid page data.

However, Randomizer function is not supported under this condition.

7.6.1 PageSize/SpareSize Application

FLCTL[21] determines whether the codeword size is 1024 bytes or 512 bytes when

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FLCTL[11] is 1.

1. Big Page

When FLCTL[11]=0(LbaEn=0), the flash to be operated is Raw NAND Flash. Every codeword size is 1024 bytes and FLCTL[21] should always be set to 0, and the PageStep in external memory is 1024 bytes if bus mode is master mode.

At this mode, the spare size and SpareStep in external memory are determined by BCH Mode as follows:

BCH Mode=16bitBCH: spare size=(28+4)bytes , SpareStep=64bytes
BCH Mode=24bitBCH: spare size=(42+4)bytes , SpareStep=64bytes
BCH Mode=40bitBCH: spare size=(70+4)bytes , SpareStep=128bytes
BCH Mode=60bitBCH: spare size=(105+4)bytes, SpareStep=128bytes

2. Small Page

When FLCTL[11]=1, LbaEn=1, the flash to be operated is Managed NAND Flash. Every codeword size could be 1024 bytes or 512 bytes according to FLCTL[21]. If FLCTL[21]=0, codeword size is 1024 bytes, PageStep in external memory is 1024 bytes, and SpareStep is 128bytes. If FLCTL[21]=1, codeword size is 512 bytes, PageStep in external memory is 512 bytes, and SpareStep is 64 bytes.

At this mode, the spare size is configured in FLCTL[18:12], and the max available number is 109.

In the summary, the total data size in every codeword for flash or for software including page data and spare data, is determined by BCHCTL[16], FLCTL[11], FLCTL[21], BCHCTL[4], BCHCTL[18]. Their relationship is shown as follows.

Table 7-4 NandC Page/Spare size for flash

page/spare size for software		page size /codeword	spare size /codeword
FLCTL[11]=0	16bitECC	1024 byte	(4+28)byte
	24bitECC	1024 byte	(4+42)byte
	40bitECC	1024 byte	(4+70)byte
	60bitECC	1024 byte	(4+105)byte
FLCTL[11]=1	FLCTL[21]=0	1024 byte	FLCTL[18:12]
	FLCTL[21]=1	512 byte	FLCTL[18:12]

Notes: that "page/spare size for flash" means that hardware should transfer these numbers of bytes in every codeword to or from flash.

7.6.2 Randomizer Application

RANDMZ_CFG[31] determines whether randomizer is enable or not. When RANDMZ_CFG[31] equals to 1, randomizer is active. Data should be scrambled before written into flash, and descrambled after read from flash.

RANDMZ_CFG[30:29] determines the randomizer polynomial.

When RANDMZ_CFG[30:29]=2'b00, Samsung randomizer, Polynomial = 1+x+x^15. RANDMZ_CFG[14:0] is the seed for randomizer.

When RANDMZ_CFG[30:29]=2'b01, TOSHIBA randomizer. RANDMZ_CFG[19:0] is the seed agitation register for randomizer. RANDMZ_CFG[23:20] is the basic seed start point for every page. RANDMZ_CFG[28:24] is the basic seed rotation bits for every 16 page.

When RANDMZ_CFG[30:29]=2'b10, Samsung randomizer, Polynomial = 1+x^14+x^15. RANDMZ_CFG[14:0] is the seed for randomizer.

The data unit for randomizer is one codeword(data+spare).

However, Randomizer is just available for data transfer by internal DMA mode, but not by for bypass mode. Furthermore, it should not be enable if BCHCTL[16]=0 (BchPage=512bytes).

7.6.3 DLL Application

When Toggle Flash or ONFI Synchronous Flash interface is active, DLL should be used to adjust DQS input with DQ when reading flash.

There are 2 registers for DLL configuration(DLL_CFG_REG0 and DLL_CFG_REG1), and 1 register for DLL status(DLL_OBS_REG0).

The usage guide is as follows:

If bypass mode is used, you should set *dll_bypass* in DLL_CFG_REG1[1] to 1, and set *dll_dqs_dly_bypass* in DLL_CFG_REG0[23:16] to determine the dll element number needed. And then set *dll_start* in DLL_CFG_REG1[0] to 1 to start the DLL.

If auto adjusting is used, you should set *dll_bypass* in DLL_CFG_REG1[1] to 0, and set the *dll_start_point* in DLL_CFG_REG0[7:0] and *dll_incr* in DLL_CFG_REG1[11:4]. You also

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should set the adjusting mode *dll_qtren* in DLL_CFG_REG1[3:2] to compute the dll element number needed. If *dll_qtren*=2'b00, the dll element number is determined by *dll_dqs_dly* in DLL_CFG_REG0[15:8]; otherwise, it is 1/4 or 1/8 of the total number of dll elements used for *dll_qtren*=2'b01 or *dll_qtren*=2'b10 separately. The last step is to set *dll_start* in DLL_CFG_REG1[0] to 1 to start the DLL.
If you want to monitor the dll working status, you could read DLL_OBS_REG0. If DLL_OBS_REG0[0]=0, it means that DLL is not locked, and still in detecting status. Otherwise, it means that DLL is locked, and *dll_lock_value* in DLL_OBS_REG0[8:1] is the total number of dll elements used, *dll_dqs_delay_value* in DLL_OBS_REG0[16:9] is the total number of DQS delay used.

7.6.4 NandC Interrupt Application

NandC has 1 interrupt output signal and 4 interrupt sources: dma finish interrupt source, flash ready interrupt source, bch error interrupt source, bchfail interrupt source. When one or more of these interrupt source are enabled, NandC interrupt is asserted if one or more interrupt source is high. Software can determine the interrupt source by reading INTST and clear interrupt by writing corresponding bit in INTCLR.

7.6.5 LLP Application

LLP is used in NandC to store and execute instruction groups configured in external memory by software. When LLPCTL[0]=1, LLP is active, NandC will load instruction groups stored in {LLPCTL[31:6], 6'h0} and execute them. Next instruction groups should not be loaded until current instruction execution finished.

1. LLP Structure

The structure of LLP is shown as follows:

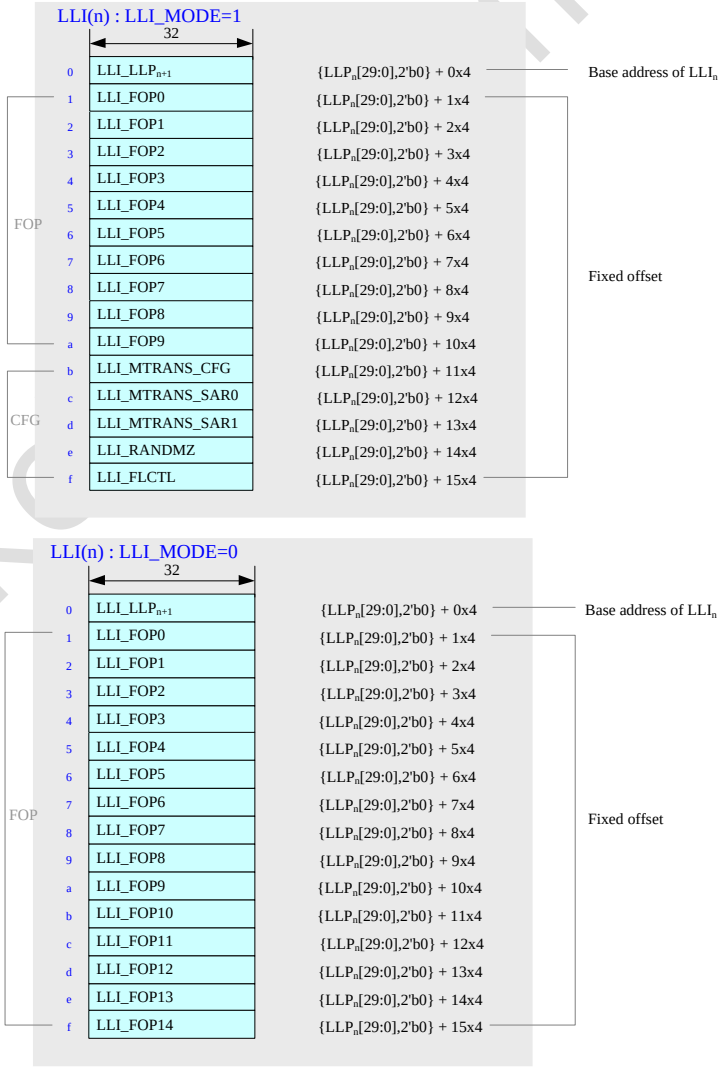


Fig. 7-4 NandC LLP Data Format

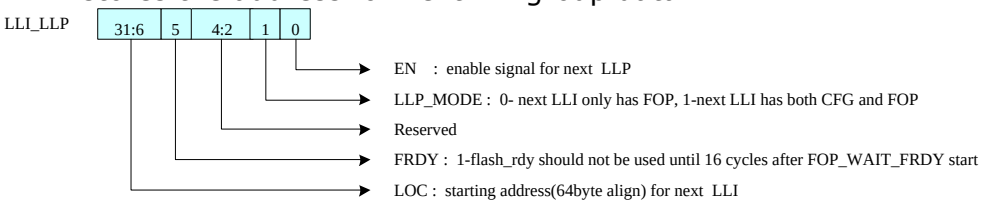
LLI_MODE is determined by LLPCTL[1]. If current operation is flash program or flash read,

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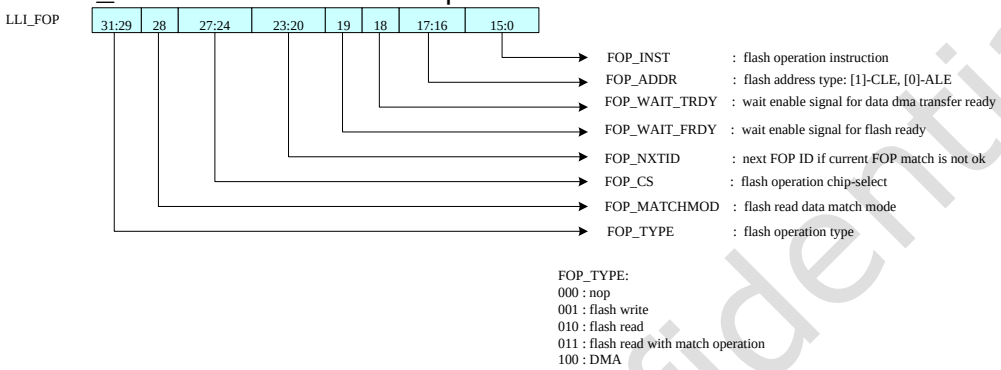
then LLI_MODE=1 is need; otherwise, LLI_MODE=0 is workable.
In addition, you could do more than one flash operation in one LLP group, but you should not separate one flash operation into two LLI groups.

2. LLI Format

a. LLI_LLPn+1 stores the address for next LLI group data



b. LLI_FOP0~LLI_FOP14 store the flash operation instruction



When FOP_TYPE=3'b011, match operation is active, and the PATTERN is LLI_FOP[15:0]. It is matched when "RDATA|PATTERN=PATTERN" with FOP_MATCHMOD=0, or when "RDATA&PATTERN=PATTERN" with FOP_MATCHMOD=1.

c. LLI_MTRANS_CFG/LLI_MTRANS_SADDR0/LLI_MTRANS_SADDR1/ LLI_RANDMZ/ LLI_FLCTL store the configuration for MTRANS_CFG/ MTRANS_SADDR0/MTRANS_SADDR1/RANDMZ/FLCTL.

3. LLP Working Mode

There are two working modes for LLP:

a. Normal mode: LLPCTL[0] is kept to 1 until all LLP loading and executing finished. Software can monitor the progress by LLPSTAT[31:6], LLPSTAT[0].

b. Pause mode: LLPCTL[0] is changed from 1 to 0 during LLP loading or LLP executing. NandC should not stop working until current LLP executing finished. Software can monitor the progress by LLPSTAT[31:6], LLPSTAT[0].

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Chapter 8 Power Management Unit (PMU)

8.1 Overview

In order to meet high performance and low power requirements, a power management unit is designed for saving power when PX3 SE in low power mode. The PX3 SE PMU is dedicated for managing the power of the whole chip.

8.1.1 Features

PMU supports the following features:

- Support 2 voltage domains including VD_CORE, VD_LOGIC
- Support 4 separate power domains in the whole chip, which can be power up/down by software based on different application scenes
- In low power mode, the pmu could power up/down vd_core by hardware
- Support CORTEX-A7 core source clock gating in low power mode
- Support Logic Bus source clock gating in low power mode
- Support global interrupt disable in low power mode
- Support pd_pmu clock switch to 32KHz or pvtm clock in low power mode
- Support DDR self-refresh in low power mode
- Support DDR controller clock auto gating in low power mode
- Support to send idle requests to all NIU in the SoC (details will be described later)
- A group of configurable counter in PMU for HW control (such as PMIC, Core power up/down and so on)
- Support varies configurable wakeup source for low power mode

8.2 Block Diagram

8.2.1 Power Domain Partition

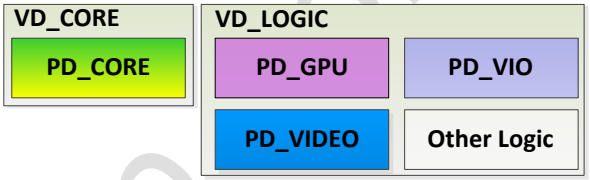


Fig. 8-1 Power Domain Partition

The above diagram describes the power domain and voltage domain partition, and the following table lists all the power domains.

Table 8-1 PX3 SE Power Domain and Voltage Domain Summary

Voltage Domain	Power Domain	Description
VD_CORE	PD_CORE	A7 logic
VD_LOGIC	PD_BUS	include pd_bus, pd_peri and other system control unit (GRF, CRU and so on)
	PD_VIO	Video input/output system, include VOP, VIP, IEP, RGA, EBC, MIPI-DSI, HDMI
	PD_VIDEO	Video Encode&Decode , include VEPU，VDPU
	PD_GPU	GPU

8.2.2 PMU Block Diagram

The following figure is the PMU block diagram. The PMU includes the 3 following sections:

- APB interface and register, which can accept the system configuration
- Low Power State Control, which generate low power control signals.
- Power Switch Control, which control all power domain switch

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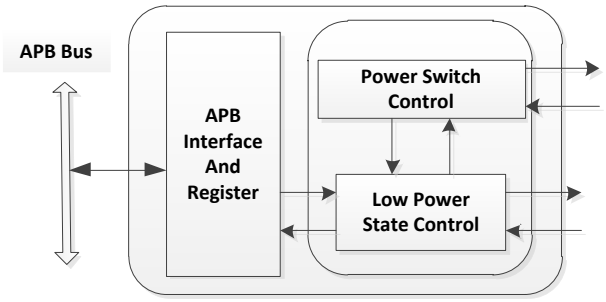


Fig. 8-2 PMU Block Diagram

8.3 Power Switch Timing Requirement

The following table describe the switch time for power down and power up progress of each power domain. This table gives the time range, and each power domain switch time will be more than the min time and less than the max time.

Table 8-2 Power Switch Timing

Power domain	type	Power down Switch Timing①(ns)	Power up Switch Timing①(ns)
PD_CORE	min	170.3	132.4
	max	306.7	237.5
	max	199.0	156.1
PD_VIO	min	280.6	217.5
	max	518.5	407.8
PD_VIDEO	min	315.4	244.2
	max	586.2	460.4
PD_GPU	min	470.2	364
	max	871.4	684.1

Notes: The power switch timing is just the chip power electrical parameter, this is not the parameter for the
software to determine the power domain status. The software need to check each power domain status
register to determine the power status.

8.4 Function Description

8.4.1 Normal Mode

First of all, we define two modes of power for chip, normal mode and low power mode.
In normal mode, the PMU can power off/on all power domain (except pd_core) by setting PMU_PWRDN_CON register. At same, pmu can send idle request for every power domain by setting PMU_IDLE_REQ register.
Don't set pd_core power off or send idle_req_core and idle_req_sys in normal mode. This will cause the system to not work properly.
Basically, there are 2 configurations that software can do in normal mode to save power.

- Configure DDR to self-refresh, DDR IO retention and DDR IO power off
- Power down power domains

The first one will save power consumption of using DDR controller and DDR IO. For avoiding confliction, the software must make sure the execution code of this step is not in DDR.
The second one will save power of the power domain which software is shutting down.

8.4.2 Low Power Mode

PMU can work in the Low Power Mode by setting bit[0] of PMU_PWRMODE_CON register. After setting the register, PMU would enter the Low Power mode .In the low power mode, pmu will auto power on/off the specified power domain, send idle req to specified power domain, disable/enable config bus clock and so on. All of above are configurable by setting corresponding registers.

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Table 8-3 Low Power State

Num	Hardware State	Descriptions of Flow	Corresponding Registers
0	NORMAL	Normal Status	
1	TRANS_NO_FIN	Wait transfer to finish	Bit[22:16] of PMU_PWRMODE_CON
2	SREF_ENTER	Enter to self refresh	Bit[8:7] of PMU_PWRMODE_CON
3	CORE_CLK_DIS	Core clock gating	Bit[1] of PMU_PWRMODE_CON
4	BUS_CLK_DIS	Cfg bug clock disable	Bit[2] of PMU_PWRMODE_CON
5	CLOCK_LF	Switch to 32KHz or pvtm	Bit[5] of PMU_PWRMODE_CON
6	CORE_PWRDN	Vd core power down	Bit[4] of PMU_PWRMODE_CON
7	WAIT_WAKEUP	Wait wakeup	
8	WAIT_24M	Wait 24MHz stable	Bit[6] of PMU_PWRMODE_CON
9	CLOCK_HF	Switch to 24MHz	
10	BUS_CLK_EN	Cfg bus clock enable	
11	CORE_CLK_EN	Core clock enable	
12	SREF_EXIT	Exit self refresh	
13	CORE_PWRUP	Vd core power up	
14	TRANS_RESTORE	Restore transfer	

The Low Power mode have three steps:

- Enter Low Power mode, there are some sub-steps in the enter step, every sub-step can be enable/disable by setting the corresponding register.
- Wait wakeup, there is only armint wakeup source by setting PMU_WAKEUP_CFG[0] register
- Exit Low Power mode, the sub-step are executed depend on whether they were executed in enter low power step.

8.4.3 Wakeup Source

There is only one wakeup source, armint which can trigger PMU from power mode to normal mode.

If software expect PMU be woken up from power mode it should be enabled by write 1 to PMU_WAKEUP_CFG[0] register before entering into power mode.

8.5 Register Description

8.5.1 Registers Summary

Name	Offset	Size	Reset Value	Description
PMU_WAKEUP_CFG	0x0000	W	0x00000000	PMU wake-up source configuration register
PMU_PWRDN_CON	0x0004	W	0x00000000	System power gating configuration register
PMU_PWRDN_ST	0x0008	W	0x00000000	System power gating status register
PMU_IDLE_REQ	0x000c	W	0x00000000	PMU Noc idle req control
PMU_IDLE_ST	0x0010	W	0x00000000	PMU Noc idle status
PMU_PWRMODE_CON	0x0014	W	0x00000000	PMU configuration register in power mode flow
PMU_PWR_STATE	0x0018	W	0x00000000	PMU Low power mode state
PMU_OSC_CNT	0x001c	W	0x00005dc0	24MHz OSC stabilization counter threshold
PMU_CORE_PWRDWN_CNT	0x0020	W	0x00005dc0	CORE domain power down waiting counter in sleep mode

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Name	Offset	Size	Reset Value	Description
PMU_CORE_PWRUP_CNT	0x0024	W	0x00005dc0	CORE domain power up waiting counter in sleep mode
PMU_SFT_CON	0x0028	W	0x00000000	PMU Software control in normal mode
PMU_DDR_SREF_ST	0x002c	W	0x00000000	PMU DDR self refresh status
PMU_INT_CON	0x0030	W	0x00000000	PMU interrupt configuration register
PMU_INT_ST	0x0034	W	0x00000000	PMU interrupt status register
PMU_SYS_REG0	0x0038	W	0x00000000	PMU system register0
PMU_SYS_REG1	0x003c	W	0x00000000	PMU system register1
PMU_SYS_REG2	0x0040	W	0x00000000	PMU system register2
PMU_SYS_REG3	0x0044	W	0x00000000	PMU system register3

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

8.5.2 Detail Register Description

PMU_WAKEUP_CFG

Address: Operational Base + offset (0x0000)
PMU wakeup source configuration register

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	armint_wakeup_en ARM interrupt wake-up enable 1'b0: disable 1'b1: enable

PMU_PWRDN_CON

Address: Operational Base + offset (0x0004)
System power gating configuration register

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3	RW	0x0	PD_VIO_DWN_EN Power domain VIO power down enable 1'b0: power on 1'b1: power off
2	RW	0x0	PD_VIDEO_DWN_EN Power domain VIDEO power down enable 1'b0: power on 1'b1: power off
1	RW	0x0	PD_GPU_DWN_EN Power domain GPU power down enable 1'b0: power on 1'b1: power off
0	RW	0x0	CORE_PWROFF_EN software conifg power off pd_core 1'b1: power off 1'b0: not power off

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PMU_PWRDN_ST
Address: Operational Base + offset (0x0008)
System power gating status register

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3	RW	0x0	pd_vio_pwr_st Power domain VIO power status 1'b0: power on 1'b1: power off
2	RW	0x0	pd_video_pwr_st Power domain VIDEO power status 1'b0: power on 1'b1: power off
1	RW	0x0	pd_gpu_pwr_st Power domain GPU power status 1'b0: power on 1'b1: power off
0	RW	0x0	pd_core_pwr_st Power domain core power status 1'b0: power on 1'b1: power off

PMU_IDLE_REQ
Address: Operational Base + offset (0x000c)
PMU Noc idle requirement control

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7	RW	0x0	idle_req_crypto_cfg software config crypto domain flush transaction request 1'b1: idle req 1'b0: not idle req
6	RW	0x0	idle_req_msch_cfg software config msch domain flush transaction request 1'b1: idle req 1'b0: not idle req
5	RW	0x0	idle_req_sys_cfg software config system domain flush transaction request 1'b1: idle req 1'b0: not idle req
4	RW	0x0	idle_req_core_cfg software config core domain flush transaction request 1'b1: idle req 1'b0: not idle req
3	RW	0x0	idle_req_gpu_cfg software config gpu domain flush transaction request 1'b1: idle req 1'b0: not idle req

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Bit	Attr	Reset Value	Description
2	RW	0x0	idle_req_vio_cfg software config vio domain flush transaction request 1'b1: idle req 1'b0: not idle req
1	RW	0x0	idle_req_video_cfg software config video domain flush transaction request 1'b1: idle req 1'b0: not idle req
0	RW	0x0	idle_req_peri_cfg software config peri domain flush transaction request 1'b1: idle req 1'b0: not idle req

PMU_IDLE_ST

Address: Operational Base + offset (0x0010)

PMU Noc idle status

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23	RW	0x0	idle_ack_crypto crypto domain flush transaction acknowledge 1'b0: no ack 1'b1: ack
22	RW	0x0	idle_ack_msch msch domain flush transaction acknowledge 1'b0: no ack 1'b1: ack
21	RW	0x0	idle_ack_sys sys domain flush transaction acknowledge 1'b0: no ack 1'b1: ack
20	RW	0x0	idle_ack_core core domain flush transaction acknowledge 1'b0: no ack 1'b1: ack
19	RW	0x0	idle_ack_gpu gpu domain flush transaction acknowledge 1'b0: no ack 1'b1: ack
18	RW	0x0	idle_ack_vio vio domain flush transaction acknowledge 1'b0: no ack 1'b1: ack
17	RW	0x0	idle_ack_video video domain flush transaction acknowledge 1'b0: no ack 1'b1: ack

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Bit	Attr	Reset Value	Description
16	RW	0x0	idle_ack_peri peri domain flush transaction acknowledge 1'b0: no ack 1'b1: ack
15:8	RO	0x0	Reserved
7	RW	0x0	IDLE_CRYPTO crypto domain flush transaction finish(idle) 1'b0: no finish 1'b1: finish
6	RW	0x0	IDLE_MSCH msch domain flush transaction finish(idle) 1'b0: no finish 1'b1: finish
5	RW	0x0	IDLE_SYS sys domain flush transaction finish(idle) 1'b0: no finish 1'b1: finish
4	RW	0x0	IDLE_CORE core domain flush transaction finish(idle) 1'b0: no finish 1'b1: finish
3	RW	0x0	IDLE_GPU gpu domain flush transaction finish(idle) 1'b0: no finish 1'b1: finish
2	RW	0x0	IDLE_VIO vio domain flush transaction finish(idle) 1'b0: no finish 1'b1: finish
1	RW	0x0	IDLE_VIDEO video domain flush transaction finish(idle) 1'b0: no finish 1'b1: finish
0	RW	0x0	IDLE_PERI peri domain flush transaction finish(idle) 1'b0: no finish 1'b1: finish

PMU_PWRMODE_CON

Address: Operational Base + offset (0x0014)

PMU configuration register in power mode flow

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
23	RW	0x0	clr_peri issue idle_req_peri in low power mode 1'b0: not issue 1'b1: issue
22	RW	0x0	clr_video issue idle_req_video in low power mode 1'b0: not issue 1'b1: issue
21	RW	0x0	clr_vio issue idle_req_vio in low power mode 1'b0: not issue 1'b1: issue
20	RW	0x0	clr_gpu issue idle_req_gpu in low power mode 1'b0: not issue 1'b1: issue
19	RW	0x0	clr_core issue idle_req_core in low power mode 1'b0: not issue 1'b1: issue
18	RW	0x0	clr_sys issue idle_req_sys in low power mode 1'b0: not issue 1'b1: issue
17	RW	0x0	clr_msch issue idle_req_msch in low power mode 1'b0: not issue 1'b1: issue
16	RW	0x0	clr_crypto issue idle_req_crypto in low power mode 1'b0: not issue 1'b1: issue
15:10	RW	0x0	ddr0io_ret_de_req ddr0io retention de-assert request 1'b0: de-assert request 1'b1: not de-assert request
9	RW	0x0	pmu_int_en pmuint enable 1'b1: enable 1'b0: disable
8	RW	0x0	ddr_gating_en ddrc auto gating in low power mode 1'b0: disable 1'b1: enable

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Bit	Attr	Reset Value	Description
7	RW	0x0	sref_enter_en DDR enter self-refresh enable in low power mode 1'b0: disable DDR enter self-refresh 1'b1: enable DDR enter self-refresh
6	RW	0x0	wait_osc_24m wait 24MHz OSC when wakeup in low power mode 1'b0: disable 1'b1: enable
5	RW	0x0	pmu_use_lf pmu domain clock switch to low clock enable 1'b0: not switch to low clock 1'b1: switch to low clock
4	RW	0x0	core_pd_en core power off enable in low power mode 1'b0: core power on 1'b1: core power off
3	RW	0x0	global_int_disable Global interrupt disable 1'b0: enable global interrupt 1'b1: disable global interrupt
2	RW	0x0	clk_bus_src_gate_en config bus clock source gating enable in idle mode 1'b0: enable 1'b1: disable
1	RW	0x0	clk_core_src_gate_en A7 core clock source gating enable in idle mode 1'b0: enable 1'b1: disable
0	RW	0x0	power_mode_en power mode flow enable 1'b0: disable 1'b1: enable

PMU_PWR_STATE
Address: Operational Base + offset (0x0018)
PMU low power mode state

Bit	Attr	Reset Value	Description
31:15	RO	0x0	reserved
14	RW	0x0	TRANS_RESTORE noc trans restore 1'b0: state not happened 1'b1: state happened
13	RW	0x0	CORE_PWRUP pd core power up state 1'b0: state not happened 1'b1: state happened

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Bit	Attr	Reset Value	Description
12	RW	0x0	SREF_EXIT ddr exit self-refresh 1'b0: state not happened 1'b1: state happened
11	RW	0x0	CORE_CLK_EN pd_core source clock enable 1'b0: state not happened 1'b1: state happened
10	RW	0x0	BUS_CLK_EN config bus source clock enable 1'b0: state not happened 1'b1: state happened
9	RW	0x0	CLOCK_HF pd_pmu switch to normal clock 1'b0: state not happened 1'b1: state happened
8	RW	0x0	WAIT_24M wait 24M osc stable 1'b0: state not happened 1'b1: state happened
7	RW	0x0	WAIT_WAKEUP wati wakeup state 1'b0: state not happened 1'b1: state happened
6	RW	0x0	CORE_PWRDN pd core down state 1'b0: state not happened 1'b1: state happened
5	RW	0x0	CLOCK_LF pd_pmu switch to low speed clock 1'b0: state not happened 1'b1: state happened
4	RW	0x0	BUS_CLK_DIS config bus source clock disable 1'b0: state not happened 1'b1: state happened
3	RW	0x0	CORE_CLK_DIS pd_core source clock disable 1'b0: state not happened 1'b1: state happened
2	RW	0x0	SREF_ENTER ddrselfrefresh enter 1'b0: state not happened 1'b1: state happened

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Bit	Attr	Reset Value	Description
1	RW	0x0	TRANS_NO_FIN transfer no finish 1'b0: state not happened 1'b1: state happened
0	RW	0x0	NORMAL normal state 1'b0: state not happened 1'b1: state happened

PMU_OSC_CNT
Address: Operational Base + offset (0x001c)
24MHz OSC stabilization counter threshold

Bit	Attr	Reset Value	Description
31:0	RW	0x05dc0	osc_stabl_cnt_thresh 24MHz OSC stabilization counter threshold

PMU_CORE_PWRDWN_CNT
Address: Operational Base + offset (0x0020)
CORE domain power down waiting counter in sleep mode

Bit	Attr	Reset Value	Description
31:0	RW	0x05dc0	core_pwrdwn_cnt_thresh CORE domain power down waiting counter threshold

PMU_CORE_PWRUP_CNT
Address: Operational Base + offset (0x0024)
CORE domain power up waiting counter in sleep mode

Bit	Attr	Reset Value	Description
31:0	RW	0x05dc0	core_pwrup_cnt_thresh CORE domain power up waiting counter threshold

PMU_SFT_CON
Address: Operational Base + offset (0x0028)
PMU Software control in normal mode

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4	RW	0x0	low_clk_sel low clock in low power mode select 1'b0: clock pvtm 1'b1: 32KHz clock
3	RW	0x0	pmu_lf_ena_cfg software config PMU domain clock switch to low clock 1'b1: switch to low speed clock 1'b0: not switch
2	RW	0x0	upctl_c_sysreq_cfg software config enter DDR self-refresh by low power interface 1'b1: request enter self-refresh 1'b0: not enter self-refresh

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Bit	Attr	Reset Value	Description
1	RW	0x0	clk_bus_src_gating_cfg config bus source clock disable 1'b1: disable 1'b0: enable
0	RW	0x0	clk_core_src_gating_cfg pd core source clock disable 1'b1: disable 1'b0: enable

PMU_DDR_SREF_ST

Address: Operational Base + offset (0x002c)

PMU_DDR self-refresh status

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x0	upctl_c_sysack DDR enter self-refresh acknowledge 1'b0: no ack 1'b1: ack
0	RW	0x0	upctl_c_active DDR enter self-refresh 1'b0: no active 1'b1: active

PMU_INT_CON

Address: Operational Base + offset (0x0030)

PMU interrupt configuration register

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5	RW	0x0	pd_core_int_en Power domain core power switch interrupt enable 1'b0: disable 1'b1: enable
4	RW	0x0	pd_gpu_int_en Power domain gpu power switch interrupt enable 1'b0: disable 1'b1: enable
3	RW	0x0	pd_video_int_en Power domain video power switch interrupt enable 1'b0: disable 1'b1: enable
2	RW	0x0	pd_vio_int_en Power domain vio power switch interrupt enable 1'b0: disable 1'b1: enable

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Bit	Attr	Reset Value	Description
1	RW	0x0	wakeup_int_en wakeup status interrupt enable 1'b0: disable 1'b1: enable
0	RW	0x0	armint_wakeup_int_en ARM interrupt wakeup status interrupt enable 1'b0: disable 1'b1: enable

PMU_INT_ST
Address: Operational Base + offset (0x0034)
PMU interrupt status register

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5	RW	0x0	pd_core_int_st Power domain core power switch status 1'b0: no power switch happen 1'b1: power switch happen
4	RW	0x0	pd_gpu_int_st Power domain gpu power switch status 1'b0: no power switch happen 1'b1: power switch happen
3	RW	0x0	pd_video_int_st Power domain video power switch status 1'b0: no power switch happen 1'b1: power switch happen
2	RW	0x0	pd_vio_int_st Power domain vio power switch status 1'b0: no power switch happen 1'b1: power switch happen
1	RW	0x0	pwrmode_wakeup_event_trig power mode flow wakeup 1'b0: no wakeup 1'b1: wakeup
0	RW	0x0	armint_wakeup_event_trig ARM interrupt wake-up enent trigger 1'b0: no wakeup 1'b1: wakeup

PMU_SYS_REG0
Address: Operational Base + offset (0x0038)
PMU system register0

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pmu_sys_reg0 PMU system register0

PMU_SYS_REG1

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Address: Operational Base + offset (0x003c)
PMU system register1

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pmu_sys_reg1 PMU system register1

PMU_SYS_REG2
Address: Operational Base + offset (0x0040)
PMU system register2

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pmu_sys_reg2 PMU system register2

PMU_SYS_REG3
Address: Operational Base + offset (0x0044)
PMU system register3

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pmu_sys_reg3 PMU system register3

8.6 Timing Diagram

8.6.1 Each domain power switch timing

The following figure is the each domain power down and power up timing.

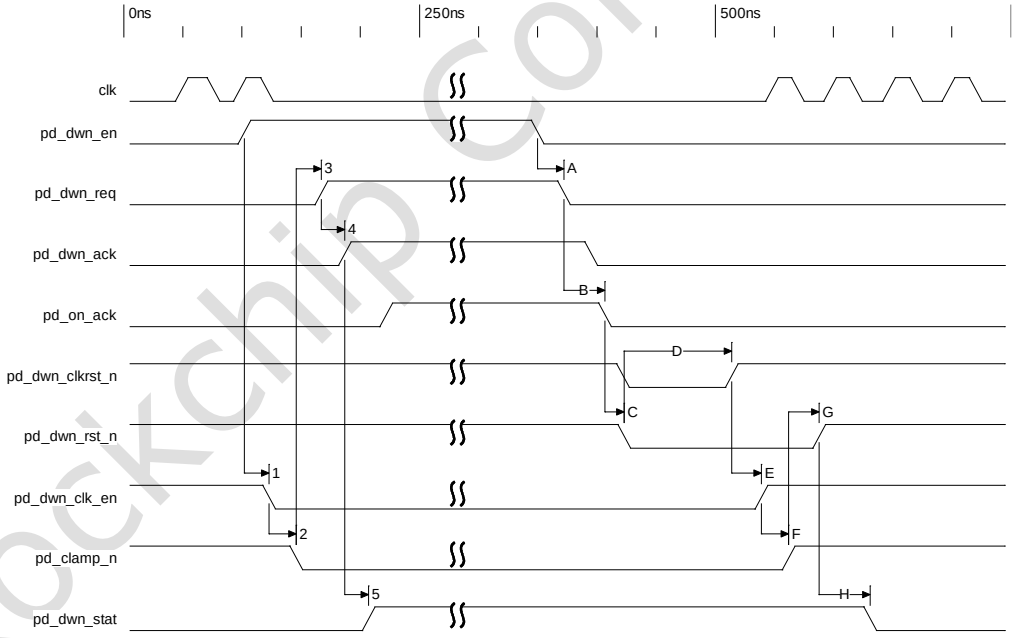


Fig. 8-3 Each Domain in Power Switch Timing

8.7 Application Notes

8.7.1 Recommend configurations for power mode

The PMU is a design with great flexibilities, but just for facilities and inheritances, a group of recommend configurations will be shown below for software. And for convenience, we will define several modes.
The PX3 SE can support some recommended power modes, for example::

- normal
- idle mode
- sleep mode

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The following table lists the detailed description of the modes.

Table 8-4 Descriptions for Recommended Power Modes

Item	Mode1(IDLE)	Mode(SLEEP)	Configurable
Core	Standby	Power Down	
Logic Clock	Enable	Disable	Yes
Logic Clock Source	24MHz	32KHz/PVTM	Yes
PLL	Working	Power Down	Yes
DDR	Working	Self-refresh	Yes

Normal mode

In this mode, you can power off/on or enable/disable the following power domain to save power: PD_VIO/PD_VIDEO/PD_GPU

Idle mode

This mode is used when the core do not have load for a shot while such as waiting for interrupt and the software want to save power by gating Cortex-A7 source clock.

In idle mode, core1/2/3 of Cortex-A7 should be either power off or in WFI/WFE state. The core0 of A7 should be in WFI/WFE state. The configurations of core clock source gating and disable global interrupt are presented. The Cortex-A7 can waked up by an interrupt.

Sleep mode

The sleep mode can power off all power domains except TOP Logic. The VD_CORE is turned off externally, and other domains power off by software.

In sleep mode the clock of PD_PMU can be switched from 24MHz to low speed clock optionally by hardware. The low speed clock can be selected from clock pvtm and 32KHz clock.

In sleep mode all PLLs power down mandatorily to save power by software.

In sleep mode OSC can be disabled optionally by software.

In sleep mode DDR self-refresh can be issued by hardware mandatorily.

8.7.2 System Registers

PMU support 4 words register: PMU_SYS_REG0, PMU_SYS_REG1, PMU_SYS_REG2, PMU_SYS_REG3. These registers are always on no matter what low power mode. So software can use these registers to retain some information which is useful after wakeup from any mode.

8.7.3 Configuration Constraint

In order to shut down the power domains correctly, the software must obey the rules bellow:

- Send NIU request to the NIU in power domain that you want to shut down.
- Querying PMU_IDLE_ST register to get the information until the pacific NIU is in idle state.
- Send power request to the power domain through PMU_PWRDN_CON register.
- Querying PMU_PWRDN_ST register to make sure the pacific power domain is power down.

The power domains controlled only by software are showing below:

PD_VIO, PD_GPU, PD_VIDEO.

So you must power off these power domains before enter low power mode if you need.

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Chapter 9 Timer

9.1 Overview

Timer is a programmable timer peripheral. This component is an APB slave device. There are 6 Timers (TIMER0~TIMER5).
All timers count up from a lower programmed value to a higher programmed value and generate an interrupt when the counter reaches the programmed value.
Timer supports the following features:

- Two operation modes: free-running and user-defined count
- Maskable for each individual interrupt.

9.2 Block Diagram

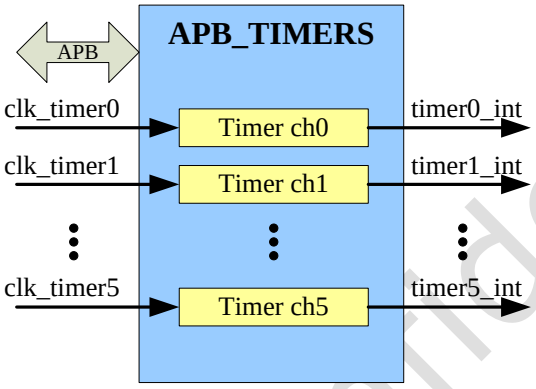


Fig. 9-1 Timer Block Diagram

The above figure shows the architecture of the APB timers (include six programmable timer channels) that in the peripheral subsystem. The Stimers that in the cpu subsystem only include two programmable timer channels.

9.3 Function Description

9.3.1 Timer clock

The timer clock is 24MHz OSC.

9.3.2 Programming sequence

1. Initialize the timer by the TIMERn_CONTROLREG register(0≤n≤5 for TIMER:
   - Disable the timer by writing a "0" to the timer enable bit (bit 0). Accordingly, the timer_en output signal is de-asserted.
   - Program the timer mode—user-defined or free-running—by writing a "0" or "1" respectively, to the timer mode bit (bit 1).
   - Set the interrupt mask as either masked or not masked by writing a "0" or "1" respectively, to the timer interrupt mask bit (bit 2).
2. Load the timer count value into the TIMERn_LOAD_COUNT0 ~TIMERn_ LOAD_COUNT03 register.
3. Enable the timer by writing a "1" to bit 0 of TIMERn_CONTROLREG.

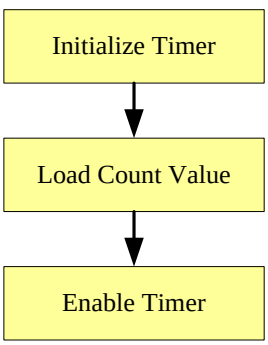


Fig. 9-2 Timer Usage Flow

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9.3.3 Loading a timer count value

The initial value for each timer is TIMERn_LOAD_COUNT3 and TIMERn_ LOAD_COUNT2. The count register will count up to the value loaded in the register TIMERn_LOAD_COUNT1 and TIMERn_ LOAD_COUNT0. Two events can cause a timer to load zero:

- Timer is enabled after reset or disabled.
- Timer counts up to the value stored in TIMERn_LOAD_COUNT1 and TIMERn_ LOAD_COUNT0, when timer is configured into free-running mode.

9.3.4 Timer mode selection

- User-defined count mode: Timer loads TIMERn_LOAD_COUNT3 and TIMERn_ LOAD_COUNT2 as initial value. When the timer counts up to the value in TIMERn_LOAD_COUNT1 and TIMERn_LOAD_COUNT0, it will not automatically reload the count register. User need to disable timer firstly and follow the programming sequence to make timer work again.
- Free-running mode: Timer loads the TIMERn_LOAD_COUNT3 and TIMERn_LOAD_COUNT2 register as initial value. Timer will automatically reload the count register, when timer counts up to the value in TIMERn_LOAD_COUNT1 and TIMERn_LOAD_COUNT0.

9.4 Register Description

This section describes the control/status registers of the design. Software should read and write these registers using 32-bits accesses.

9.4.1 Registers Summary

Name	Offset	Size	Reset Value	Description
TIMERn_LOAD_COUNT0	0x0000	W	0x00000000	Timer n higher Load Count Register
TIMERn_LOAD_COUNT1	0x0004	W	0x00000000	Timer n higher Load Count Register
TIMERn_CURRENT_VALUE0	0x0008	W	0x00000000	Timer n Current Value Register
TIMERn_CURRENT_VALUE1	0x000c	W	0x00000000	Timer n Current Value Register
TIMERn_LOAD_COUNT2	0x0010	W	0x00000000	Timer n lower Load Count Register
TIMERn_LOAD_COUNT3	0x0014	W	0x00000000	Timer n lower Load Count Register
TIMERn_INTSTATUS	0x0018	W	0x00000000	Timer Interrupt Stauts Register
TIMERn_CONTROLREG	0x001c	W	0x00000000	Timer n Control Register

Notes:
*(1) Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*
(2) 0≤n≤5 for TIMER
(3) Base address:

- *TIMER0: 0x20044000*
- *TIMER1: 0x20044020*
- *TIMER2: 0x20044040*
- *TIMER3: 0x20044060*
- *TIMER4: 0x20044080*
- *TIMER5: 0x200440a0*

9.4.2 Detail Register Description

TIMERn_LOAD_COUNT0

Address: Operational Base + offset (0x00)
Timer n High Load Count Register

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	load_count_low bits Low 32 bits value to be loaded into Timer n.

TIMERn_LOAD_COUNT1
Address: Operational Base + offset (0x04)
Timer n High Load Count Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	load_count_high bits High 32 bits value to be loaded into Timer n.

TIMERn_CURRENT_VALUE0
Address: Operational Base + offset (0x08)
Timer n Current Value Register

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	current_cnt_lowbits Low 32 bits of current value of timer n.

TIMERn_CURRENT_VALUE1
Address: Operational Base + offset (0x0c)
Timer n Current Value Register

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	current_cnt_highbits High 32 bits of current value of timer n.

TIMERn_LOAD_COUNT2
Address: Operational Base + offset (0x10)
Timer n Low Load Count Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	load_count_low bits Low 32 bits value to be loaded into Timer n.

TIMERn_LOAD_COUNT3
Address: Operational Base + offset (0x14)
Timer n Low Load Count Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	load_count_high bits High 32 bits value to be loaded into Timer n.

TIMERn_INTSTATUS
Address: Operational Base + offset (0x18)
Timer Interrupt Stauts Register

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
0	W1C	0x0	int_pd This register contains the interrupt status for timer n. Write 1 to this register will clear the interrupt.

TIMERn_CONTROLREG
Address: Operational Base + offset (0x1c)
Timer n Control Register

Bit	Attr	Reset Value	Description
31:3	RO	0x0	reserved
2	RW	0x0	int_en Timer interrupt mask 0: mask 1: not mask
1	RW	0x0	timer_mode Timer mode. 0: free-running mode 1: user-defined count mode
0	RW	0x0	timer_en Timer enable. 0: disable 1: enable

9.5 Application Notes

In the chip, the timer_clk is from 24MHz OSC, asynchronous to the pclk. When user disables the timer enable bit(bit 0 of TIMERn_CONTROLREG), the timer_en output signal is de-asserted, and timer_clk will stop. When user enables the timer, the timer_en signal is asserted and timer_clk will start running.
The application is only allowed to re-config registers when timer_en is low.

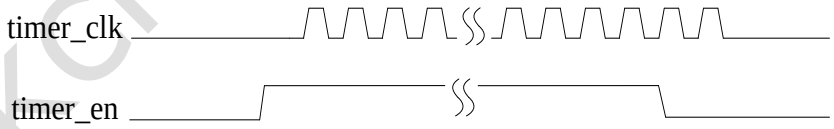


Fig. 9-3 Timing between timer_en and timer_clk

Please refer to "Function Description" section for the timer usage flow.

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Chapter 10 Generic Interrupt Controller (GIC)

10.1 Overview

The generic interrupt controller (GIC) in this device has two interfaces, the distributor interface connects to the interrupt source, and the CPU interface connects to Cortex-A7. It supports the following features:

- Supports 128hardware interrupt inputs
- Masking of any interrupts
- Prioritization of interrupts
- Distribution of the interrupts to the target Cortex-A7 processor(s)
- Generation of interrupts by software
- Supports Security Extensions

10.2 Block Diagram

Below diagram shows the block diagram of GIC.

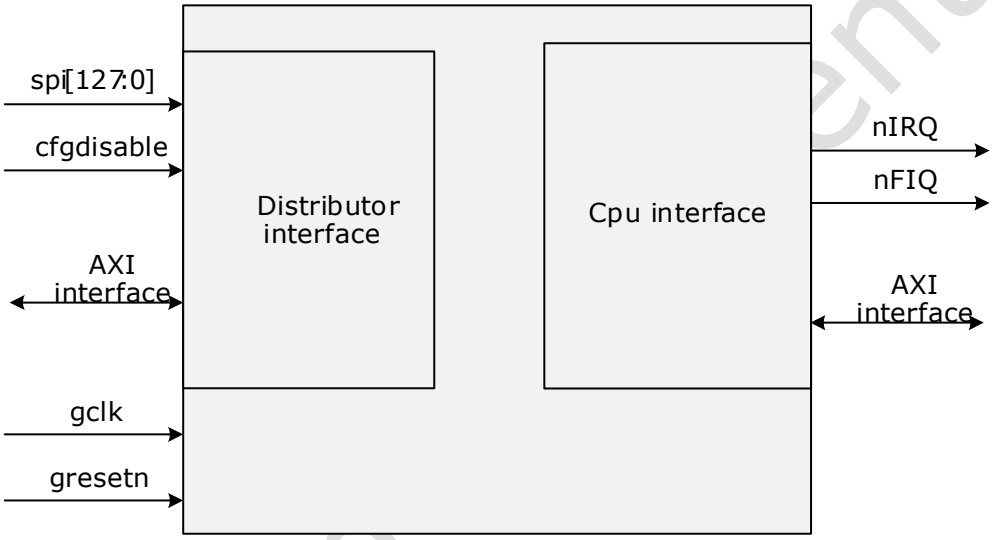


Fig. 10-1 Block diagram of GIC

The diagram shows that GIC has two AXI interfaces independently and has two base address for these two interfaces.

10.3 Function Description

Please refer to the GIC400 documents for the detail description.

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Chapter 11 DMA Controller (DMAC)

11.1 Overview

This device supports one Direct Memory Access (DMA) Controller, DMAC. The DMAC supports transfers between memory and memory, peripheral and memory.
The DMAC supports the following features:

- An instruction set that provides flexibility for programming DMA transfers
- A single AXI master interface with 64-bit bus width that performs the DMA transfers
- Dual APB slave interfaces, designated as secure and non-secure, for accessing registers in the DMAC
- Supports TrustZone technology
- Supports multiple transfer types: memory-to-memory, memory-to-peripheral, peripheral-to-memory, scatter-gather
- Supports 8 DMA channels, with programmable security state for each DMA channel
- Supports 16 peripheral requests
- Supports 32 depth of the internal data buffer
- Supports 1 interrupt and 1 abort

Following table shows the DMAC request mapping scheme.

Table 11-1 DMAC Request Mapping Table

Req number	Source	Polarity
0	I2S_2ch_tx	High level
1	I2S_2ch_rx	High level
2	UART0 tx	High level
3	UART0 rx	High level
4	UART1 tx	High level
5	UART1 rx	High level
6	UART2 tx	High level
7	UART2 rx	High level
8	SPI tx	High level
9	SPI rx	High level
10	SDMMC	High level
11	SDIO	High level
12	EMMC	High level
13	SPDIF	High level
14	I2S_8ch tx	High level
15	I2S_8ch rx	High level

The DMAC supports incrementing-address burst and fixed-address burst. But in the case of access SPI and UART at byte or halfword size, DMAC only support fixed-address burst and the address must be aligned to word.

11.2 Block Diagram

Following figure shows the block diagram of DMAC.

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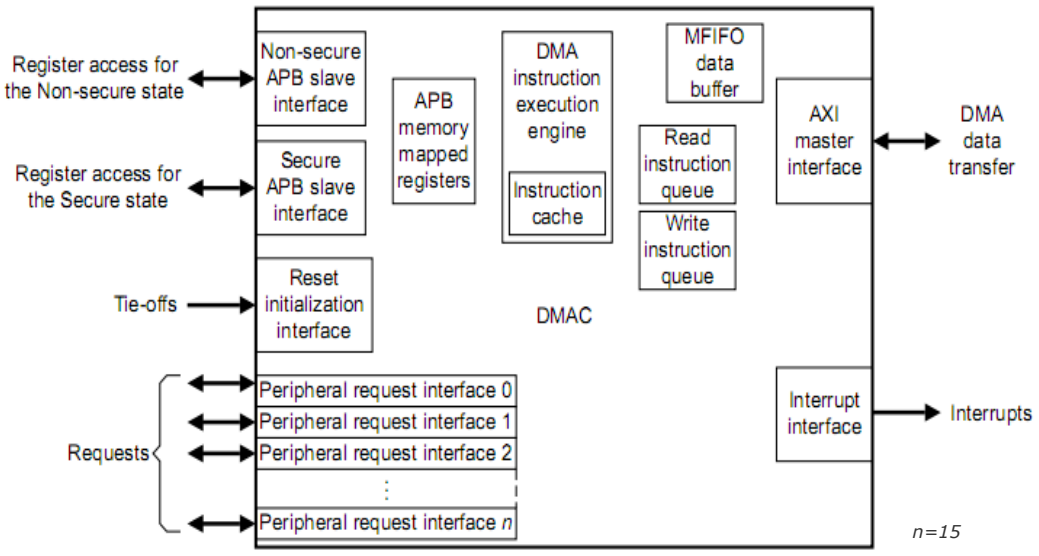


Fig. 11-1 Block diagram of DMAC

11.3 Function Description

11.3.1 Introduction

The DMAC contains an instruction processing block that enables it to process program code that controls a DMA transfer. The program code is stored in a region of system memory that the DMAC accesses using its AXI interface. The DMAC stores instructions temporarily in a cache.

DMAC supports 8 channels, each channel capable of supporting a single concurrent thread of DMA operation. In addition, a single DMA manager thread exists, and you can use it to initialize the DMA channel threads. The DMAC executes up to one instruction for each AXI clock cycle. To ensure that it regularly executes each active thread, it alternates by processing the DMA manager thread and then a DMA channel thread. It uses a round-robin process when selecting the next active DMA channel thread to execute.

The DMAC uses variable-length instructions that consist of one to six bytes. It provides a separate Program Counter (PC) register for each DMA channel. When a thread requests an instruction from an address, the cache performs a look-up. If a cache hit occurs, then the cache immediately provides the data. Otherwise, the thread is stalled while the DMAC uses the AXI interface to perform a cache line fill. If an instruction is greater than 4 bytes, or spans the end of a cache line, the DMAC performs multiple cache accesses to fetch the instruction.

When a cache line fill is in progress, the DMAC enables other threads to access the cache, but if another cache miss occurs, this stalls the pipeline until the first line fill is complete.

When a DMA channel thread executes a load or store instruction, the DMAC adds the instruction to the relevant read or write queue. The DMAC uses these queues as an instruction storage buffer prior to it issuing the instructions on the AXI bus. The DMAC also contains a Multi First-In-First-Out (MFIFO) data buffer that it uses to store data that it reads, or writes, during a DMA transfer.

11.3.2 Operating states

Following figure shows the operating states for the DMA manager thread and DMA channel threads.

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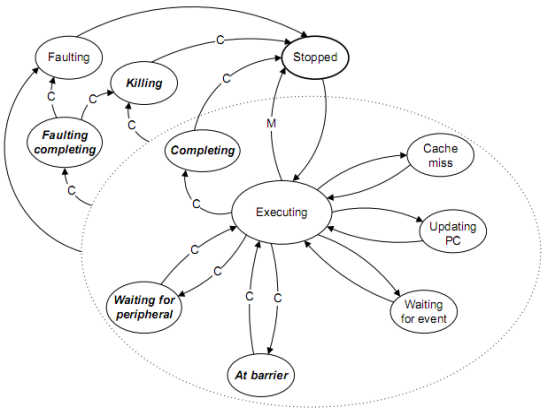


Fig. 11-2 DMAC operation states

Notes: arcs with no letter designator indicate state transitions for the DMA manager and DMA channel threads, otherwise use is restricted as follows:
C: DMA channel threads only.
M: DMA manager thread only.

After the DMAC exits from reset, it sets all DMA channel threads to the stopped state, and the status of boot_from_pc(tie-off interface of dmac) controls the DMA manager thread state:
boot_from_pc is LOW :DMA manager thread moves to the Stopped state.
boot_from_pc is HIGH :DMA manager thread moves to the Executing state.

11.4 Register Description

11.4.1 Registers Summary

Name	Offset	Size	Reset Value	Description
DMAC_DSR	0x0000	W	0x00000000	DMA Manager Status Register
DMAC_DPC	0x0004	W	0x00000000	DMA Program Counter Register
DMAC_INTEN	0x0020	W	0x00000000	Interrupt Enable Register
DMAC_EVENT_RIS	0x0024	W	0x00000000	Event-Interrupt Raw Status Register
DMAC_INTMIS	0x0028	W	0x00000000	Interrupt Status Register
DMAC_INTCLR	0x002c	W	0x00000000	Interrupt Clear Register
DMAC_FSRD	0x0030	W	0x00000000	Fault Status DMA Manager Register
DMAC_FSRC	0x0034	W	0x00000000	Fault Status DMA Channel Register
DMAC_FTRD	0x0038	W	0x00000000	Fault Type DMA Manager Register
DMAC_FTR0	0x0040	W	0x00000000	Fault Type DMA Channel Register
DMAC_FTR1	0x0044	W	0x00000000	Fault Type DMA Channel Register
DMAC_FTR2	0x0048	W	0x00000000	Fault Type DMA Channel Register
DMAC_FTR3	0x004c	W	0x00000000	Fault Type DMA Channel Register
DMAC_FTR4	0x0050	W	0x00000000	Fault Type DMA Channel Register
DMAC_FTR5	0x0054	W	0x00000000	Fault Type DMA Channel Register
DMAC_FTR6	0x0058	W	0x00000000	Fault Type DMA Channel Register
DMAC_FTR7	0x005c	W	0x00000000	Fault Type DMA Channel Register
DMAC_CSR0	0x0100	W	0x00000000	Channel Status Registers
DMAC_CPC0	0x0104	W	0x00000000	Channel Program Counter Registers

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Name	Offset	Size	Reset Value	Description
DMAC_CSR1	0x0108	W	0x00000000	Channel Status Registers
DMAC_CPC1	0x010c	W	0x00000000	Channel Program Counter Registers
DMAC_CSR2	0x0110	W	0x00000000	Channel Status Registers
DMAC_CPC2	0x0114	W	0x00000000	Channel Program Counter Registers
DMAC_CSR3	0x0118	W	0x00000000	Channel Status Registers
DMAC_CPC3	0x011c	W	0x00000000	Channel Program Counter Registers
DMAC_CSR4	0x0120	W	0x00000000	Channel Status Registers
DMAC_CPC4	0x0124	W	0x00000000	Channel Program Counter Registers
DMAC_CSR5	0x0128	W	0x00000000	Channel Status Registers
DMAC_CPC5	0x012c	W	0x00000000	Channel Program Counter Registers
DMAC_CSR6	0x0130	W	0x00000000	Channel Status Registers
DMAC_CPC6	0x0134	W	0x00000000	Channel Program Counter Registers
DMAC_CSR7	0x0138	W	0x00000000	Channel Status Registers
DMAC_CPC7	0x013c	W	0x00000000	Channel Program Counter Registers
DMAC_SAR0	0x0400	W	0x00000000	Source Address Registers
DMAC_DAR0	0x0404	W	0x00000000	Destination Address Registers
DMAC_CCR0	0x0408	W	0x00000000	Channel Control Registers
DMAC_LC0_0	0x040c	W	0x00000000	Loop Counter 0 Registers
DMAC_LC1_0	0x0410	W	0x00000000	Loop Counter 1 Registers
DMAC_SAR1	0x0420	W	0x00000000	Source Address Registers
DMAC_DAR1	0x0424	W	0x00000000	Destination Address Registers
DMAC_CCR1	0x0428	W	0x00000000	Channel Control Registers
DMAC_LC0_1	0x042c	W	0x00000000	Loop Counter 0 Registers
DMAC_LC1_1	0x0430	W	0x00000000	Loop Counter 1 Registers
DMAC_SAR2	0x0440	W	0x00000000	Source Address Registers
DMAC_DAR2	0x0444	W	0x00000000	Destination Address Registers
DMAC_CCR2	0x0448	W	0x00000000	Channel Control Registers
DMAC_LC0_2	0x044c	W	0x00000000	Loop Counter 0 Registers
DMAC_LC1_2	0x0450	W	0x00000000	Loop Counter 1 Registers
DMAC_SAR3	0x0460	W	0x00000000	Source Address Registers
DMAC_DAR3	0x0464	W	0x00000000	Destination Address Registers
DMAC_CCR3	0x0468	W	0x00000000	Channel Control Registers
DMAC_LC0_3	0x046c	W	0x00000000	Loop Counter 0 Registers
DMAC_LC1_3	0x0470	W	0x00000000	Loop Counter 1 Registers
DMAC_SAR4	0x0480	W	0x00000000	Source Address Registers
DMAC_DAR4	0x0484	W	0x00000000	Destination Address Registers

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Name	Offset	Size	Reset Value	Description
DMAC_CCR4	0x0488	W	0x00000000	Channel Control Registers
DMAC_LC0_4	0x048c	W	0x00000000	Loop Counter 0 Registers
DMAC_LC1_4	0x0490	W	0x00000000	Loop Counter 1 Registers
DMAC_SAR5	0x04a0	W	0x00000000	Source Address Registers
DMAC_DAR5	0x04a4	W	0x00000000	Destination Address Registers
DMAC_CCR5	0x04a8	W	0x00000000	Channel Control Registers
DMAC_LC0_5	0x04ac	W	0x00000000	Loop Counter 0 Registers
DMAC_LC1_5	0x04b0	W	0x00000000	Loop Counter 1 Registers
DMAC_SAR6	0x04c0	W	0x00000000	Source Address Registers
DMAC_DAR6	0x04c4	W	0x00000000	Destination Address Registers
DMAC_CCR6	0x04c8	W	0x00000000	Channel Control Registers
DMAC_LC0_6	0x04cc	W	0x00000000	Loop Counter 0 Registers
DMAC_LC1_6	0x04d0	W	0x00000000	Loop Counter 1 Registers
DMAC_SAR7	0x04e0	W	0x00000000	Source Address Registers
DMAC_DAR7	0x04e4	W	0x00000000	Destination Address Registers
DMAC_CCR7	0x04e8	W	0x00000000	Channel Control Registers
DMAC_LC0_7	0x04ec	W	0x00000000	Loop Counter 0 Registers
DMAC_LC1_7	0x04f0	W	0x00000000	Loop Counter 1 Registers
DMAC_DBGSTATUS	0x0d00	W	0x00000000	Debug Status Register
DMAC_DBGCMD	0x0d04	W	0x00000000	Debug Command Register
DMAC_DBGINST0	0x0d08	W	0x00000000	Debug Instruction-0 Register
DMAC_DBGINST1	0x0d0c	W	0x00000000	Debug Instruction-1 Register
DMAC_CR0	0x0e00	W	0x00047051	Configuration Register 0
DMAC_CR1	0x0e04	W	0x00000057	Configuration Register 1
DMAC_CR2	0x0e08	W	0x00000000	Configuration Register 2
DMAC_CR3	0x0e0c	W	0x00000000	Configuration Register 3
DMAC_CR4	0x0e10	W	0x00000006	Configuration Register 4
DMAC_CRDn	0x0e14	W	0x02094733	DMA Configuration Register
DMAC_WD	0x0e80	W	0x00000000	DMA Watchdog Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

11.4.2 Detail Register Description

DMAC_DSR

Address: Operational Base + offset (0x0000)

DMA Manager Status Register

Bit	Attr	Reset Value	Description
31:10	RO	0x0	reserved
9	RO	0x0	Provides the security status of the DMA manager thread: 1'b0: DMA manager operates in the Secure state 1'b1: DMA manager operates in the Non-secure state

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Bit	Attr	Reset Value	Description
8:4	RO	0x00	When the DMA manager thread executes a DMAWFE instruction, it waits for the following event to occur: 5'b00000: event[0] 5'b00001: event[1] 5'b00010: event[2] …… 5'b11111: event[31]
3:0	RO	0x0	The operating state of the DMA manager: 4'b0000: Stopped 4'b0001: Executing 4'b0010: Cache miss 4'b0011: Updating PC 4'b0100: Waiting for event 4'b0101~4'b1110: reserved 4'b1111: Faulting

DMAC_DPC
Address: Operational Base + offset (0x0004)
DMA Program Counter Register

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	Program counter for the DMA manager thread

DMAC_INTEN
Address: Operational Base + offset (0x0020)
Interrupt Enable Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Program the appropriate bit to control how the DMAC responds when it executes DMASEV: Bit[N]=1'b0: If the DMAC executes DMASEV for the event-interrupt resource N then the DMAC signals event N to all of the threads. Set bit[N] to 0 if your system design does not use irq[N] to signal an interrupt request. Bit[N]=1'b1: If the DMAC executes DMASEV for the event-interrupt resource N then the DMAC sets irq[N] HIGH. Set bit[N] to 1 if your system designer requires irq[N] to signal an interrupt request.

DMAC_EVENT_RIS
Address: Operational Base + offset (0x0024)
Event-Interrupt Raw Status Register

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	Returns the status of the event-interrupt resources: Bit[N]=1'b0: Event N is inactive or irq[N] is LOW Bit[N]=1'b1: Event N is active or irq[N] is HIGH

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DMAC_INTMIS
Address: Operational Base + offset (0x0028)
Interrupt Status Register

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	Provides the status of the interrupts that are active in the DMAC: Bit[N]=1'b0: Interrupt N is inactive and therefore irq[N] is LOW Bit[N]=1'b1: Interrupt N is active and therefore irq[N] is HIGH

DMAC_INTCLR
Address: Operational Base + offset (0x002c)
Interrupt Clear Register

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	Controls the clearing of the irq outputs: Bit[N]=1'b0: The status of irq[N] does not change Bit[N]=1'b1: The DMAC sets irq[N] LOW if the INTEN Register programs the DMAC to signal an interrupt. Otherwise, the status of irq[N] does not change.

DMAC_FSRD
Address: Operational Base + offset (0x0030)
Fault Status DMA Manager Register

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	Provides the fault status of the DMA manager: 1'b0: the DMA manager thread is not in the Faulting state 1'b1: the DMA manager thread is in the Faulting state

DMAC_FSRC
Address: Operational Base + offset (0x0034)
Fault Status DMA Channel Register

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	Each bit provides the fault status of the corresponding channel: Bit[N]=1'b0: No fault is present on DMA channel N. Bit[N]=1'b1: DMA channel N is in the Faulting or Faulting completing state.

DMAC_FTRD
Address: Operational Base + offset (0x0038)
Fault Type DMA Manager Register

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
30	RO	0x0	If the DMA manager aborts, this bit indicates if the erroneous instruction was read from the system memory or from the debug interface: 1'b0: instruction that generated an abort was read from system memory 1'b1: instruction that generated an abort was read from the debug interface
29:17	RO	0x0	reserved
16	RO	0x0	Indicates the AXI response that the DMAC receives on the RRESP bus, after the DMA manager performs an instruction fetch: 1'b0: OKAY response 1'b1: EXOKAY, SLVERR, or DECERR response
15:6	RO	0x0	reserved
5	RO	0x0	Indicates if the DMA manager was attempting to execute DMAWFE or DMASEV with inappropriate security permissions: 1'b0: DMA manager has appropriate security to execute DMAWFE or DMASEV 1'b1: a DMA manager thread in the Non-secure state attempted to execute either DMAWFE to wait for a secure event, DMASEV to create a secure event or secure interrupt
4	RO	0x0	Indicates if the DMA manager was attempting to execute DMAGO with inappropriate security permissions: 1'b0: DMA manager has appropriate security to execute DMAGO 1'b1: DMA manager thread in the Non-secure state attempted to execute DMAGO to create a DMA channel operating in the Secure state
3:2	RO	0x0	reserved
1	RO	0x0	Indicates if the DMA manager was attempting to execute an instruction operand that was not valid for the configuration of the DMAC: 1'b0: valid operand 1'b1: invalid operand
0	RW	0x0	Indicates if the DMA manager was attempting to execute an undefined instruction: 1'b0: defined instruction 1'b1: undefined instruction

DMAC_FTR0~DMAC_FTR7

Address: Operational Base + offset (0x0040)
Operational Base+0x44
Operational Base+0x48
Operational Base+0x4C
Operational Base+0x50
Operational Base+0x54
Operational Base+0x58
Operational Base+0x5C

Fault Type DMA Channel Register

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Bit	Attr	Reset Value	Description
31	RO	0x0	Indicates if the DMA channel has locked-up because of resource starvation: 1'b0: DMA channel has adequate resources 1'b1: DMA channel has locked-up because of insufficient resources This fault is an imprecise abort.
30	RO	0x0	If the DMA channel aborts, this bit indicates if the erroneous instruction was read from the system memory or from the debug interface: 1'b0: instruction that generated an abort was read from system memory 1'b1: instruction that generated an abort was read from the debug interface This fault is an imprecise abort but the bit is only valid when a precise abort occurs.
29:19	RO	0x0	reserved
18	RO	0x0	Indicates the AXI response that the DMAC receives on the RRESP bus, after the DMA channel thread performs a data read: 1'b0: OKAY response 1'b1: EXOKAY, SLVERR, or DECERR response This fault is an imprecise abort
17	RO	0x0	Indicates the AXI response that the DMAC receives on the BRESP bus, after the DMA channel thread performs a data write: 1'b0: OKAY response 1'b1: EXOKAY, SLVERR, or DECERR response This fault is an imprecise abort.
16	RO	0x0	Indicates the AXI response that the DMAC receives on the RRESP bus, after the DMA channel thread performs an instruction fetch: 1'b0: OKAY response 1'b1: EXOKAY, SLVERR, or DECERR response This fault is a precise abort.
15:14	RO	0x0	reserved
13	RO	0x0	Indicates if the MFIFO did not contain the data to enable the DMAC to perform the DMAST: 1'b0: MFIFO contains all the data to enable the DMAST to complete 1'b1: previous DMALDs have not put enough data in the MFIFO to enable the DMAST to complete This fault is a precise abort.

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Bit	Attr	Reset Value	Description
12	RO	0x0	Indicates if the MFIFO prevented the DMA channel thread from executing DMALD or DMAST. Depending on the instruction: DMALD 1'b0: MFIFO contains sufficient space 1'b1: MFIFO is too small to hold the data that DMALD requires DMAST 1'b0: MFIFO contains sufficient data 1'b1: MFIFO is too small to store the data to enable DMAST to complete This fault is an imprecise abort
11:8	RO	0x0	reserved
7	RO	0x0	Indicates if a DMA channel thread, in the Non-secure state, attempts to program the CCRn Register to perform a secure read or secure write: 1'b0: a DMA channel thread in the Non-secure state is not violating the security permissions 1'b1: a DMA channel thread in the Non-secure state attempted to perform a secure read or secure write This fault is a precise abort.
6	RO	0x0	Indicates if a DMA channel thread, in the Non-secure state, attempts to execute DMAWFP, DMALDP, DMASTP, or DMAFLUSHP with inappropriate security permissions: 1'b0: a DMA channel thread in the Non-secure state is not violating the security permissions 1'b1: a DMA channel thread in the Non-secure state attempted to execute either: ● DMAWFP to wait for a secure peripheral ● DMALDP or DMASTP to notify a secure peripheral ● DMAFLUSHP to flush a secure peripheral This fault is a precise abort.
5	RO	0x0	Indicates if the DMA channel thread attempts to execute DMAWFE or DMASEV with inappropriate security permissions: 1'b0: a DMA channel thread in the Non-secure state is not violating the security permissions 1'b1: a DMA channel thread in the Non-secure state attempted to execute either: ● DMAWFE to wait for a secure event ● DMASEV to create a secure event or secure interrupt This fault is a precise abort.
4:2	RO	0x0	reserved
1	RO	0x0	Indicates if the DMA channel thread was attempting to execute an instruction operand that was not valid for the configuration of the DMAC: 1'b0: valid operand 1'b1: invalid operand This fault is a precise abort.

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Bit	Attr	Reset Value	Description
0	RO	0x0	Indicates if the DMA channel thread was attempting to execute an undefined instruction: 1'b0: defined instruction 1'b1: undefined instruction This fault is a precise abort.

DMAC_CSR0~DMAC_CSR7

Address: Operational Base+0x100
Operational Base+0x108
Operational Base+0x110
Operational Base+0x118
Operational Base+0x120
Operational Base+0x128
Operational Base+0x130
Operational Base+0x138

Channel Status Registers

Bit	Attr	Reset Value	Description
31:22	RO	0x0	reserved
21	RO	0x0	The channel non-secure bit provides the security of the DMA channel: 1'b0: DMA channel operates in the Secure state 1'b1: DMA channel operates in the Non-secure state
20:16	RO	0x0	reserved
15	RO	0x0	When the DMA channel thread executes DMAWFP this bit indicates if the peripheral operand was set: 1'b0: DMAWFP executed with the peripheral operand not set 1'b1: DMAWFP executed with the peripheral operand set
14	RO	0x0	When the DMA channel thread executes DMAWFP this bit indicates if the burst or single operand were set: 1'b0: DMAWFP executed with the single operand set 1'b1: DMAWFP executed with the burst operand set
13:9	RO	0x0	reserved
8:4	RO	0x00	If the DMA channel is in the Waiting for event state or the Waiting for peripheral state then these bits indicate the event or peripheral number that the channel is waiting for: 5'b00000: DMA channel is waiting for event, or peripheral, 0 5'b00001: DMA channel is waiting for event, or peripheral, 1 5'b00010: DMA channel is waiting for event, or peripheral, 2 … 5'b11111: DMA channel is waiting for event, or peripheral, 31

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Bit	Attr	Reset Value	Description
3:0	RO	0x0	The channel status encoding is: 4'b0000: Stopped 4'b0001: Executing 4'b0010: Cache miss 4'b0011: Updating PC 4'b0100: Waiting for event 4'b0101: At barrier 4'b0110: reserved 4'b0111: Waiting for peripheral 4'b1000: Killing 4'b1001: Completing 4'b1010-4'b1101: reserved 4'b1110: Faulting completing 4'b1111: Faulting

DMAC_CPC0~DMAC_CPC7

Address: Operational Base+0x104
Operational Base+0x10C
Operational Base+0x114
Operational Base+0x11c
Operational Base+0x124
Operational Base+0x12C
Operational Base+0x134
Operational Base+0x13C

Channel Program Counter Registers

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	Program counter for the DMA channel thread

DMAC_SAR0~DMAC_SAR7

Address: Operational Base+0x400
Operational Base+0x420
Operational Base+0x440
Operational Base+0x460
Operational Base+0x480
Operational Base+0x4A0
Operational Base+0x4C0
Operational Base+0x4E0

Source Address Registers

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	Address of the source data for DMA channel

DMAC_DAR0~DMAC_DAR7

Address: Operational Base+0x404
Operational Base+0x424
Operational Base+0x444
Operational Base+0x464
Operational Base+0x484
Operational Base+0x4A4
Operational Base+0x4C4
Operational Base+0x4E4

Destination Address Registers

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	Address of the Destination data for DMA channel

DMAC_CCR0~DMAC_CCR7

Address: Operational Base+0x408
Operational Base+0x428
Operational Base+0x448
Operational Base+0x468
Operational Base+0x488
Operational Base+0x4A8
Operational Base+0x4C8
Operational Base+0x4E8

Channel Control Registers

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:25	RO	0x0	Programs the state of AWCACHE[3,1:0]a when the DMAC writes the destination data: Bit [27] 1'b0: AWCACHE[3] is LOW 1'b1: AWCACHE[3] is HIGH Bit [26] 1'b0: AWCACHE[1] is LOW 1'b1: AWCACHE[1] is HIGH Bit [25] 1'b0: AWCACHE[0] is LOW 1'b1: AWCACHE[0] is HIGH
24:22	RO	0x0	Programs the state of AWPROT[2:0]a when the DMAC writes the destination data: Bit [24] 1'b0: AWPROT[2] is LOW 1'b1: AWPROT[2] is HIGH Bit [23] 1'b0: AWPROT[1] is LOW 1'b1: AWPROT[1] is HIGH Bit [22] 1'b0: AWPROT[0] is LOW 1'b1: AWPROT[0] is HIGH
21:18	RO	0x0	For each burst, these bits program the number of data transfers that the DMAC performs when it writes the destination data: 4'b0000: 1 data transfer 4'b0001: 2 data transfers 4'b0010: 3 data transfers … 4'b1111: 16 data transfers. The total number of bytes that the DMAC writes out of the MFIFO when it executes a DMAST instruction is the product of dst_burst_len and dst_burst_size

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Bit	Attr	Reset Value	Description
17:15	RO	0x0	For each beat within a burst, it programs the number of bytes that the DMAC writes to the destination: 3'b000: writes 1 byte per beat 3'b001: writes 2 bytes per beat 3'b010: writes 4 bytes per beat 3'b011: writes 8 bytes per beat 3'b100: writes 16 bytes per beat 3'b101~3'b111: reserved. The total number of bytes that the DMAC writes out of the MFIFO when it executes a DMAST instruction is the product of dst_burst_len and dst_burst_size.
14	RO	0x0	Programs the burst type that the DMAC performs when it writes the destination data: 1'b0: Fixed-address burst. The DMAC signals AWBURST[0] LOW. 1'b1: Incrementing-address burst. The DMAC signals AWBURST[0] HIGH.
13:11	RO	0x0	Set the bits to control the state of ARCACHE[2:0]a when the DMAC reads the source data: Bit [13] 1'b0: ARCACHE[2] is LOW 1'b1: ARCACHE[2] is HIGH Bit [12] 1'b0: ARCACHE[1] is LOW 1'b1: ARCACHE[1] is HIGH Bit [11] 1'b0: ARCACHE[0] is LOW 1'b1: ARCACHE[0] is HIGH
10:8	RO	0x0	Programs the state of ARPROT[2:0]a when the DMAC reads the source data: Bit [10] 1'b0: ARPROT[2] is LOW 1'b1: ARPROT[2] is HIGH Bit [9] 1'b0: ARPROT[1] is LOW 1'b1: ARPROT[1] is HIGH Bit [8] 1'b0: ARPROT[0] is LOW 1'b1: ARPROT[0] is HIGH

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Bit	Attr	Reset Value	Description
7:4	RO	0x0	For each burst, these bits program the number of data transfers that the DMAC performs when it reads the source data: b0000: 1 data transfer 4'b0001: 2 data transfers 4'b0010: 3 data transfers … 4'b1111: 16 data transfers The total num4'ber of bytes that the DMAC reads into the MFIFO when it executes a DMALD instruction is the product of src_burst_len and src_burst_size.
3:1	RO	0x0	For each beat within a burst, it programs the number of bytes that the DMAC reads from the source: 3'b000: reads 1 byte per beat 3'b001: reads 2 bytes per beat 3'b010: reads 4 bytes per beat 3'b011: reads 8 bytes per beat 3'b100: reads 16 bytes per beat 3'b101~3'b111: reserved The total number of bytes that the DMAC reads into the MFIFO when it executes a DMALD instruction is the product of src_burst_len and src_burst_size.
0	RO	0x0	Programs the burst type that the DMAC performs when it reads the source data: 1'b0: Fixed-address burst. The DMAC signals ARBURST[0] LOW 1'b1: Incrementing-address burst. The DMAC signals ARBURST[0] HIGH

DMAC_LC0_0~DMAC_LC0_7

Address: Operational Base+0x40c
Operational Base+0x42C
Operational Base+0x44C
Operational Base+0x46C
Operational Base+0x48C
Operational Base+0x4AC
Operational Base+0x4CC
Operational Base+0x4EC

Loop Counter 0 Registers

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RO	0x0	Loop counter 0 iterations

DMAC_LC1_0~DMAC_LC1_7

Address: Operational Base+0x410
Operational Base+0x430
Operational Base+0x450
Operational Base+0x470
Operational Base+0x490
Operational Base+0x4B0
Operational Base+0x4D0

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Operational Base+0x4F0
Loop Counter 1 Registers

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RO	0x0	Loop counter 1 iterations

DMAC_DBGSTATUS
Address: Operational Base + offset (0x0d00)
Debug Status Register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1:0	RO	0x0	The debug encoding is as follows: 2'b00: execute the instruction that the DBGINST [1:0] Registers contain 2'b01: reserved 2'b10: reserved 2'b11: reserved

DMAC_DBGCMD
Address: Operational Base + offset (0x0d04)
Debug Command Register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1:0	WO	0x0	The debug encoding is as follows: 2'b00: execute the instruction that the DBGINST [1:0] Registers contain 2'b01: reserved 2'b10: reserved 2'b11: reserved

DMAC_DBGINST0
Address: Operational Base + offset (0x0d08)
Debug Instruction-0 Register

Bit	Attr	Reset Value	Description
31:24	WO	0x00	Instruction byte 1
23:16	WO	0x00	Instruction byte 0
15:11	RO	0x0	reserved
10:8	WO	0x0	DMA channel number: 3'b000: DMA channel 0 3'b001: DMA channel 1 3'b010: DMA channel 2 … 3'b111: DMA channel 7
7:1	RO	0x0	reserved
0	WO	0x0	The debug thread encoding is as follows: 1'b0: DMA manager thread 1'b1: DMA channel

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DMAC_DBGINST1
Address: Operational Base + offset (0x0d0c)
Debug Instruction-1 Register

Bit	Attr	Reset Value	Description
31:24	WO	0x00	Instruction byte 5
23:16	WO	0x00	Instruction byte 4
15:8	WO	0x00	Instruction byte 3
7:0	WO	0x00	Instruction byte 2

DMAC_CR0
Address: Operational Base + offset (0x0e00)
Configuration Register 0

Bit	Attr	Reset Value	Description
31:22	RO	0x0	reserved
21:17	RO	0x02	Number of interrupt outputs that the DMAC provides: 5'b00000: 1 interrupt output, irq[0] 5'b00001: 2 interrupt outputs, irq[1:0] 5'b00010: 3 interrupt outputs, irq[2:0] … b5'11111: 32 interrupt outputs, irq[31:0]
16:12	RO	0x07	Number of peripheral request interfaces that the DMAC provides: 5'b00000: 1 peripheral request interface 5'b00001: 2 peripheral request interfaces 5'b00010: 3 peripheral request interfaces … 5'b11111: 32 peripheral request interfaces
11:7	RO	0x0	reserved
6:4	RO	0x5	Number of DMA channels that the DMAC supports: 3'b000: 1 DMA channel 3'b001: 2 DMA channels 3'b010: 3 DMA channels … 3'b111: 8 DMA channels
3	RO	0x0	reserved
2	RO	0x0	Indicates the status of the boot_manager_ns signal when the DMAC exited from reset: 1'b0: boot_manager_ns was LOW 1'b1: boot_manager_ns was HIGH
1	RO	0x0	Indicates the status of the boot_from_pc signal when the DMAC exited from reset: 1'b0: boot_from_pc was LOW 1'b1: boot_from_pc was HIGH

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Bit	Attr	Reset Value	Description
0	RO	0x1	Supports peripheral requests: 1'b0: the DMAC does not provide a peripheral request interface 1'b1: the DMAC provides the number of peripheral request interfaces that the num_periph_req field specifies

DMAC_CR1
Address: Operational Base + offset (0x0e04)
Configuration Register 1

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RO	0x5	Number of i-cache lines: 4'b0000: 1 i-cache line 4'b0001: 2 i-cache lines 4'b0010: 3 i-cache lines … 4'b1111: 16 i-cache lines
3	RO	0x0	reserved
2:0	RO	0x7	The length of an i-cache line: 3'b000-3'b001: reserved 3'b010: 4 bytes 3'b011: 8 bytes 3'b100: 16 bytes 3'b101: 32 bytes 3'b110-3'b111: reserved

DMAC_CR2
Address: Operational Base + offset (0x0e08)
Configuration Register 2

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	Provides the value of boot_addr[31:0] when the DMAC exited from reset

DMAC_CR3
Address: Operational Base + offset (0x0e0c)
Configuration Register 3

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	Provides the security state of an event-interrupt resource: Bit [N]=1'b0: Assigns event<N> or irq[N] to the Secure state Bit [N]=1'b1: Assigns event<N> or irq[N] to the Non-secure state

DMAC_CR4
Address: Operational Base + offset (0x0e10)
Configuration Register 4

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000006	Provides the security state of the peripheral request interfaces: Bit [N]=1'b0: Assigns peripheral request interface N to the Secure state Bit [N]=1'b1: Assigns peripheral request interface N to the Non-secure state

DMAC_CRDn

Address: Operational Base + offset (0x0e14)

DMA Configuration Register

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RO	0x020	The number of lines that the data buffer contains: 10'b000000000: 1 line 10'b000000001: 2 lines … 10'b111111111: 1024 lines
19:16	RO	0x9	The depth of the read queue: 4'b0000: 1 line 4'b0001: 2 lines … 4'b1111: 16 lines
15	RO	0x0	reserved
14:12	RO	0x4	Read issuing capability that programs the number of outstanding read transactions: 3'b000: 1 3'b001: 2 … 3'b111: 8
11:8	RO	0x7	The depth of the write queue: 4'b0000: 1 line 4'b0001: 2 lines … 4'b1111: 16 lines
7	RO	0x0	reserved
6:4	RO	0x3	Write issuing capability that programs the number of outstanding write transactions: 3'b000: 1 3'b001: 2 … 3'b111: 8
3	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
2:0	RO	0x3	The data bus width of the AXI interface: 3'b000: reserved 3'b001: reserved 3'b010: 32-bit 3'b011: 64-bit 3'b100: 128-bit 3'b101-3'b111: reserved

DMAC_WD
Address: Operational Base + offset (0x0e80)
DMA Watchdog Register

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	Controls how the DMAC responds when it detects a lock-up condition: 1'b0: the DMAC aborts all of the contributing DMA channels and sets irq_abort HIGH 1'b1: the DMAC sets irq_abort HIGH

11.5 Timing Diagram

Following picture shows the relationship between dma_req and dma_ack.

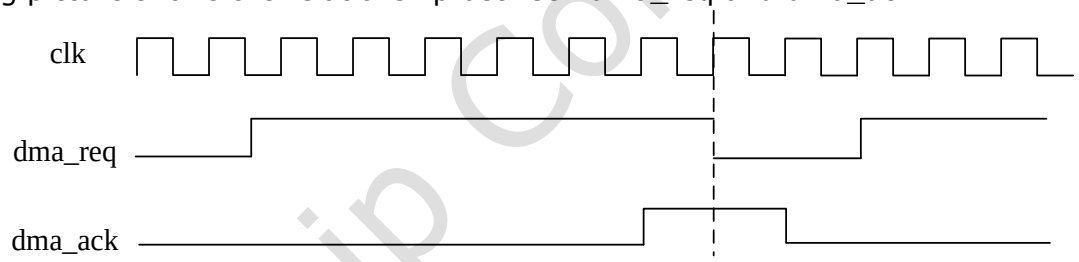


Fig. 11-3 DMAC request and acknowledge timing

11.6 Interface Description

DMAC has the following tie-off signals. It can be configured by GRF. (Please refer to the chapter to find how to configure)

Table 11-2 DMAC boot interface

Interface	Reset value	SGRF_SOC_CON0[15]=1
boot_addr	20'b0	{GRF_DMAC_CON2[3:0],GRF_DMAC_CON1[15:0]}
boot_from_pc	1'b1	GRF_DMAC_CON0[0]
boot_manager_ns	1'b1	1'b1
boot_irq_ns	16'h0	16'hffff
boot_periph_ns	16'hffff	16'hffff
drtype	2'h3	GRF_DMAC_CON2[5:4]

boot_addr
Configures the address location that contains the first instruction the DMAC executes, when it exits from reset.
boot_from_pc
Controls the location in which the DMAC executes its initial instruction, after it exits from reset:

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0 = DMAC waits for an instruction from either APB interface
1 = DMA manager thread executes the instruction that is located at the address that

boot_manager_ns

When the DMAC exits from reset, this signal controls the security state of the DMA manager thread:
0 = assigns DMA manager to the Secure state
1 = assigns DMA manager to the Non-secure state.

boot_irq_ns

Controls the security state of an event-interrupt resource, when the DMAC exits from reset:
boot_irq_ns[x] is LOW
The DMAC assigns event<x> or irq[x] to the Secure state.
boot_irq_ns[x] is HIGH
The DMAC assigns event<x> or irq[x] to the Non-secure state.

boot_periph_ns

Controls the security state of a peripheral request interface, when the DMAC exits from reset:
boot_periph_ns[x] is LOW
The DMAC assigns peripheral request interface x to the Secure state.
boot_periph_ns[x] is HIGH
The DMAC assigns peripheral request interface x to the Non-secure state.

11.7 Application Notes

11.7.1 Using the APB slave interfaces

DMAC can work under non-secure state only, and the secure APB interface is not used. So only the non-secure APB interface can be used to start or restart a DMA channel.
The necessary steps to start a DMA channel thread using the debug instruction registers as following:
1. Create a program for the DMA channel.
2. Store the program in a region of system memory.
3. Poll the DMAC_DBGSTATUS Register to ensure that debug is idle, that is, the dbgstatus bit is 0.
4. Write to the DMAC_DBGINST0 Register and enter the:

- Instruction byte 0 encoding for DMAGO.
- Instruction byte 1 encoding for DMAGO.
- Debug thread bit to 0. This selects the DMA manager thread.

5. Write to the DMAC_DBGINST1 Register with the DMAGO instruction byte [5:2] data, see Debug Instruction-1 Register 0. You must set these four bytes to the address of the first instruction in the program, which are written to system memory in step 2.
6. Writing zero to the DMAC_DBGCMD Register. The DMAC starts the DMA channel thread and sets the dbgstatus bit to 1.

11.7.2 Security usage

DMA manager thread is in the secure state

If the DNS bit is 0, the DMA manager thread operates in the secure state and it only performs secure instruction fetches. When a DMA manager thread in the secure state processes:

DMAGO

It uses the status of the ns bit, to set the security state of the DMA channel thread by writing to the CNS bit for that channel.

DMAWFE

It halts execution of the thread until the event occurs. When the event occurs, the DMAC continues execution of the thread, irrespective of the security state of the corresponding INS bit.

DMASEV

It sets the corresponding bit in the DMAC_EVENT_RIS Register, irrespective of the security state of the corresponding INS bit.

DMA manager thread is in the Non-secure state

If the DNS bit is 1, the DMA manager thread operates in the Non-secure state, and it only

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performs non-secure instruction fetches. When a DMA manager thread in the Non-secure state processes:

DMAGO

The DMAC uses the status of the ns bit, to control if it starts a DMA channel thread. If:

ns = 0

The DMAC does not start a DMA channel thread and instead it:

1. Executes a NOP.
2. Sets the DMAC_FSRD Register, see Fault Status DMA Manager
3. Sets the dmago_err bit in the DMAC_FTRD Register, see Fault Type DMA Manager Register.
4. Moves the DMA manager to the Faulting state.

ns = 1

The DMAC starts a DMA channel thread in the Non-secure state and programs the CNS bit to be non-secure.

DMAWFE

The DMAC uses the status of the corresponding INS bit, in the DMAC_CR3 Register, to control if it waits for the event. If:

INS = 0

The event is in the Secure state. The DMAC:

1. Executes a NOP.
2. Sets the DMAC_FSRD Register, see Fault Status DMA Manager Register.
3. Sets the mgr_evnt_err bit in the DMAC_FTRD Register, see Fault Type DMA Manager Register.
4. Moves the DMA manager to the Faulting state.

INS = 1

The event is in the Non-secure state. The DMAC halts execution of the thread and waits for the event to occur.

DMASEV

The DMAC uses the status of the corresponding INS bit, in the DMAC_CR3 Register, to control if it creates the event-interrupt. If:

INS = 0

The event-interrupt resource is in the secure state. The DMAC:

1. Executes a NOP.
2. Sets the DMAC_FSRD Register, see Fault Status DMA Manager Register.
3. Sets the mgr_evnt_err bit in the DMAC_FTRD Register, see Fault Type DMA Manager Register.
4. Moves the DMA manager to the Faulting state.

INS = 1

The event-interrupt resource is in the Non-secure state. The DMAC creates the event-interrupt.

DMA channel thread is in the secure state

When the CNS bit is 0, the DMA channel thread is programmed to operate in the Secure state and it only performs secure instruction fetches.

When a DMA channel thread in the secure state processes the following instructions:

DMAWFE

The DMAC halts execution of the thread until the event occurs. When the event occurs, the DMAC continues execution of the thread, irrespective of the security state of the corresponding INS bit, in the DMAC_CR3 Register.

DMASEV

The DMAC creates the event-interrupt, irrespective of the security state of the corresponding INS bit, in the DMAC_CR3 Register.

DMAWFP

The DMAC halts execution of the thread until the peripheral signals a DMA request. When this occurs, the DMAC continues execution of the thread, irrespective of the security state of the corresponding PNS bit, in the DMAC_CR4 Register.

DMALDP, DMASTP

The DMAC sends a message to the peripheral to communicate that data transfer is

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complete, irrespective of the security state of the corresponding PNS bit, in the DMAC_CR4 Register.

DMAFLUSHP

The DMAC clears the state of the peripheral and sends a message to the peripheral to resend its level status, irrespective of the security state of the corresponding PNS bit, in the DMAC_CR4 Register.

When a DMA channel thread is in the Secure state, it enables the DMAC to perform secure and non-secure AXI accesses

DMA channel thread is in the Non-secure state

When the CNS bit is 1, the DMA channel thread is programmed to operate in the Non-secure state and it only performs non-secure instruction fetches.

When a DMA channel thread in the Non-secure state processes the following instructions:

DMAWFE

The DMAC uses the status of the corresponding INS bit, in the DMAC_CR3 Register, to control if it waits for the event. If:

INS = 0

The event is in the Secure state. The DMAC:

1. Executes a NOP.
2. Sets the appropriate bit in the DMAC_FSRC Register that corresponds to the DMA channel number. See Fault Status DMA Channel Register.
3. Sets the ch_evnt_err bit in the DMAC_FTRn(n=0~7) Register, see Fault Type DMA Channel Registers.
4. Moves the DMA channel to the Faulting completing state.

INS = 1

The event is in the Non-secure state. The DMAC halts execution of the thread and waits for the event to occur.

DMASEV

The DMAC uses the status of the corresponding INS bit, in the DMAC_CR3 Register, to control if it creates the event. If:

INS = 0

The event-interrupt resource is in the Secure state. The DMAC:

1. Executes a NOP.
2. Sets the appropriate bit in the DMAC_FSRC Register that corresponds to the DMA channel number. See Fault Status DMA Channel Register.
3. Sets the ch_evnt_err bit in the DMAC_FTRn(n=0~7) Register, see Fault Type DMA Channel Registers.
4. Moves the DMA channel to the Faulting completing state.

INS = 1

The event-interrupt resource is in the Non-secure state. The DMAC creates the event-interrupt.

DMAWFP

The DMAC uses the status of the corresponding PNS bit, in the DMAC_CR4 Register, to control if it waits for the peripheral to signal a request. If:

PNS = 0

The peripheral is in the Secure state. The DMAC:

1. Executes a NOP.
2. Sets the appropriate bit in the DMAC_FSRC Register that corresponds to the DMA channel number. See Fault Status DMA Channel Register.
3. Sets the ch_periph_err bit in the DMAC_FTRn(n=0~7) Register, see Fault Type DMA Channel Registers.
4. Moves the DMA channel to the Faulting completing state.

PNS = 1

The peripheral is in the Non-secure state. The DMAC halts execution of the thread and waits for the peripheral to signal a request.

DMALDP, DMASTP

The DMAC uses the status of the corresponding PNS bit, in the DMAC_CR4 Register, to control if it sends an acknowledgement to the peripheral. If:

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PNS = 0
The peripheral is in the secure state. The DMAC:
1. Executes a NOP.
2. Sets the appropriate bit in the DMAC_FSRC Register that corresponds to the DMA channel number. See Fault Status DMA Channel Register.
3. Sets the ch_periph_err bit in the DMAC_FTRn(n=0~7) Register, see Fault Type DMA Channel Registers.
4. Moves the DMA channel to the Faulting completing state.
PNS = 1
The peripheral is in the Non-secure state. The DMAC sends a message to the peripheral to communicate when the data transfer is complete.

DMAFLUSHP

The DMAC uses the status of the corresponding PNS bit, in the DMAC_CR4 Register, to control if it sends a flush request to the peripheral. If:
PNS = 0
The peripheral is in the secure state. The DMAC:
1. Executes a NOP.
2. Sets the appropriate bit in the DMAC_FSRC Register that corresponds to the DMA channel number. See Fault Status DMA Channel Register.
3. Sets the ch_periph_err bit in the DMAC_FTRn(n=0~7) Register, see Fault Type DMA Channel Registers.
4. Moves the DMA channel to the Faulting completing state.
PNS = 1
The peripheral is in the Non-secure state. The DMAC clears the state of the peripheral and sends a message to the peripheral to resend its level status.
When a DMA channel thread is in the Non-secure state, and a DMAMOV CCR instruction attempts to program the channel to perform a secure AXI transaction, the DMAC:
1. Executes a DMANOP.
2. Sets the appropriate bit in the DMAC_FSRC Register that corresponds to the DMA channel number. See Fault Status DMA Channel Register.
3. Sets the ch_rdwr_err bit in the DMAC_FTRn(n=0~7) Register, see Fault Type DMA Channel Registers.
4. Moves the DMA channel thread to the Faulting completing state.

11.7.3 Programming restrictions

Fixed unaligned bursts

The DMAC does not support fixed unaligned bursts. If you program the following conditions, the DMAC treats this as a programming error:
Unaligned read

- src_inc field is 0 in the DMAC_CCRn(n=0~7) Register
- the SARn Register contains an address that is not aligned to the size of data that the src_burst_size field contain

Unaligned write

- dst_inc field is 0 in the DMAC_CCRn(n=0~7) Register
- the DARn Register contains an address that is not aligned to the size of data that the dst_burst_size field contains

Endian swap size restrictions

If you program the endian_swap_size field in the DMAC_CCRn(n=0~7) Register, to enable a DMA channel to perform an endian swap then you must set the corresponding DMAC_SARn(n=0~7) Register and the corresponding DMAC_DARn(n=0~7) Register to contain an address that is aligned to the value that the endian_swap_size field contains.

Updating DMA channel control registers during a DMA cycle restrictions

Prior to the DMAC executing a sequence of DMALD and DMAST instructions, the values you program in to the DMAC_CCRn(n=0~7) Register, DMAC_SARn(n=0~7) Register, and DMAC_DARn(n=0~7) Register control the data byte lane manipulation that the DMAC performs when it transfers the data from the source address to the destination address. You'd better not update these registers during a DMA cycle.

Resource sharing between DMA channels

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DMA channel programs share the MFIFO data storage resource. You must not start a set of concurrently running DMA channel programs with a resource requirement that exceeds the configured size of the MFIFO. If you exceed this limit then the DMAC might lock up and generate a Watchdog abort.

11.7.4 Unaligned transfers may be corrupted

For a configuration with more than one channel, if any of channels 1 to 7 is performing transfers between certain types of misaligned source and destination addresses, then the output data may be corrupted by the action of channel 0.

Data corruption might occur if all of the following are true:

1. Two beats of AXI read data are received for one of channels 1 to 7.
2. Source and destination address alignments mean that each read data beat is split across two lines in the data buffer (see Splitting data, below).
3. There is one idle cycle between the two read data beats.
4. Channel 0 performs an operation that updates channel control information during this idle cycle (see Updates to channel control information, below)

Splitting data

Depending upon the programmed values for the DMA transfer, one beat of read data from the AXI interface need to be split across two lines in the internal data buffer. This occurs when the read data beat contains data bytes which will be written to addresses that wrap around at the AXI interface data width, so that these bytes could not be transferred by a single AXI write data beat of the full interface width.

Most applications of DMAC do not split data in this way, so are NOT vulnerable to data corruption from this defect.

The following cases are NOT vulnerable to data corruption because they do not split data:

- Byte lane offset between source and destination addresses is 0 when source and destination addresses have the same byte lane alignment, the offset is 0 and a wrap operation that splits data cannot occur.
- Byte lane offset between source and destination addresses is a multiple of source size

Table 11-3 Source size in CCRn

Source size in DMAC_CCRn(n-0~7)	Allowed offset between DMAC_SARn and DMAC_DARn(n=0~7)
SS8	any offset allowed.
SS16	0,2,4,6,8,10,12,14
SS32	0,4,8,12
SS64	0,8

11.7.5 Interrupt shares between channel

As the DMAC does not record which channel (or list of channels) have asserted an interrupt. So it will depend on your program and whether any of the visible information for that program can be used to determine progress, and help identify the interrupt source.

There are 4 likely information sources that can be used to determine the progress made by a program:

- Program counter (PC)
- Source address
- Destination address
- Loop counters (LC)

For example, a program might emit an interrupt each time that it iterates around a loop. In this case, the interrupt service routine (ISR) would need to store the loop value of each channel when it is called, and then compare against the new value when it is next called. A change in value would indicate that the program has progressed.

The ISR must be carefully written to ensure that no interrupts are lost. The sequence of operations is as follows:

1. Disable interrupts
2. Immediately clear the interrupt in DMAC
3. Check the relevant registers for both channels to determine which must be serviced
4. Take appropriate action for the channels
5. Re-enable interrupts and exit ISR

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11.7.6 Instruction sets

Table 11-4 DMAC Instruction sets

Mnemonic	Instruction	Thread usage
DMAADDH	Add Halfword	C
DMAEND	End	M/C
DMAFLUSHP	Flush and notify Peripheral	C
DMAGO	Go	M
DMAKILL	Kill	C
DMALD	Load	C
DMALDP	Load Peripheral	C
DMALP	Loop	C
DMALPEND	Loop End	C
DMALPFE	Loop Forever	C
DMAMOV	Move	C
DMANOP	No operation	M/C
DMARMB	Read Memory Barrier	C
DMASEV	Send Event	M/C
DMAST	Store	C
DMASTP	Store and notify Peripheral	C
DMASTZ	Store Zero	C
DMAWFE	Wait For Event M	M/C
DMAWFP	Wait For Peripheral	C
DMAWMB	Write Memory Barrier	C
DMAADNH	Add Negative Halfword	C

Notes: Thread usage: C=DMA channel, M=DMA manager

11.7.7 Assembler directives

In this document, only DMMADNH instruction is took as an example to show the way the instruction assembled.

DMAADNH

Add Negative Halfword adds an immediate negative 16-bit value to the DMAC_SARn(n=0~7) Register or DMAC_DARn(n=0~7) Register, for the DMA channel thread. This enables the DMAC to support 2D DMA operations, or reading or writing an area of memory in a different order to naturally incrementing addresses. See Source Address Registers and Destination Address Registers.

The immediate unsigned 16-bit value is one-extended to 32 bits, to create a value that is the two's complement representation of a negative number between -65536 and -1, before the DMAC adds it to the address using 32-bit addition. The DMAC discards the carry bit so that addresses wrap from 0xFFFFFFFF to 0x00000000. The net effect is to subtract between 65536 and 1 from the current value in the Source or Destination Address Register.

Following table shows the instruction encoding.

Table 11-5 DMAC instruction encoding

Imm[15:8]	Imm[7:0]	0	1	0	1	1	1	ra	0

Assembler syntax

DMAADNH <address_register>, <16-bit immediate>

where:

<address_register>

Selects the address register to use. It must be either:

SAR

DMAC_SARn(n=0~7) Register and sets ra to 0.

DAR

DMAC_DARn(n=0~7) Register and sets ra to 1.

<16-bit immediate>

The immediate value to be added to the <address_register>.

You should specify the 16-bit immediate as the number that is to be represented in the instruction encoding. For example, DMAADNH DAR, 0xFFF0 causes the value 0xFFFFFFF0 to be added to the current value of the Destination Address Register, effectively subtracting 16

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from the DAR.
You can only use this instruction in a DMA channel thread.

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Chapter 12 GMAC Ethernet Interface

12.1 Overview

The GMAC Ethernet Controller provides a complete Ethernet interface from processor to a Reduced Media Independent Interface (RMII) and Reduced Gigabit Media Independent Interface (RGMII) compliant Ethernet PHY.
The GMAC includes a DMA controller. The DMA controller efficiently moves packet data from microprocessor's RAM, formats the data for an IEEE 802.3-2002 compliant packet and transmits the data to an Ethernet Physical Interface (PHY). It also efficiently moves packet data from RXFIFO to microprocessor's RAM.

12.1.1 Feature

- Supports 10/100/1000-Mbps data transfer rates with the RGMII interfaces
- Supports 10/100-Mbps data transfer rates with the RMII interfaces
- Supports both full-duplex and half-duplex operation
  - Supports CSMA/CD Protocol for half-duplex operation
  - Supports packet bursting and frame extension in 1000 Mbps half-duplex operation
  - Supports IEEE 802.3x flow control for full-duplex operation
  - Optional forwarding of received pause control frames to the user application in full-duplex operation
  - Back-pressure support for half-duplex operation
  - Automatic transmission of zero-quanta pause frame on de-assertion of flow control input in full-duplex operation
- Preamble and start-of-frame data (SFD) insertion in Transmit, and deletion in Receive paths
- Automatic CRC and pad generation controllable on a per-frame basis
- Options for Automatic Pad/CRC Stripping on receive frames
- Programmable frame length to support Standard Ethernet frames
- Programmable InterFrameGap (40-96 bit times in steps of 8)
- Supports a variety of flexible address filtering modes:
  - 64-bit Hash filter (optional) for multicast and uni-cast (DA) addresses
  - Option to pass all multicast addressed frames
  - Promiscuous mode support to pass all frames without any filtering for network monitoring
  - Passes all incoming packets (as per filter) with a status report
- Separate 32-bit status returned for transmission and reception packets
- Supports IEEE 802.1Q VLAN tag detection for reception frames
- MDIO Master interface for PHY device configuration and management
- Support detection of LAN wake-up frames and AMD Magic Packet frames
- Support checksum off-load for received IPv4 and TCP packets encapsulated by the Ethernet frame
- Support checking IPv4 header checksum and TCP, UDP, or ICMP checksum encapsulated in IPv4 or IPv6 datagrams
- Comprehensive status reporting for normal operation and transfers with errors
- Support per-frame Transmit/Receive complete interrupt control
- Supports 4-KB receive FIFO depths on reception.
- Supports 2-KB FIFO depth on transmission
- Automatic generation of PAUSE frame control or backpressure signal to the GMAC core based on Receive FIFO-fill (threshold configurable) level
- Handles automatic retransmission of Collision frames for transmission
- Discards frames on late collision, excessive collisions, excessive deferral and underrun conditions
- AXI interface to any CPU or memory
- Software can select the type of AXI burst (fixed and variable length burst) in the AXI Master interface
- Supports internal loopback on the RGMII/RMII for debugging

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- Debug status register that gives status of FSMs in Transmit and Receive data-paths and FIFO fill-levels.

12.2 Block Diagram

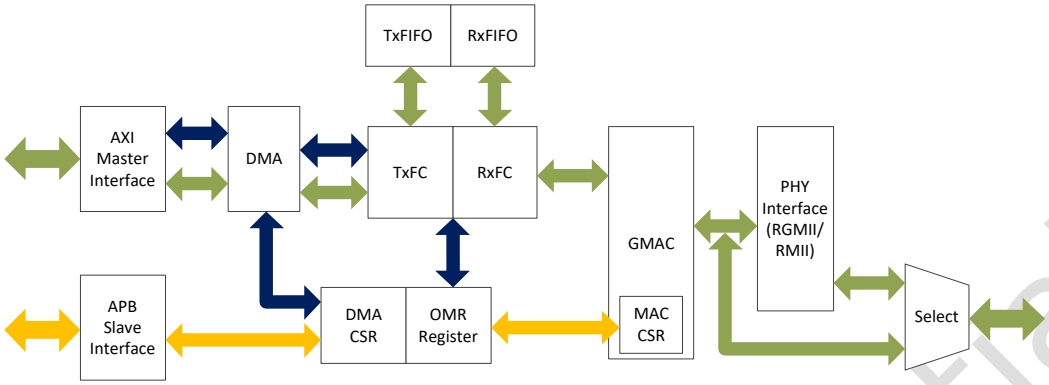


Fig. 12-1 GMAC Architecture

The GMAC is broken up into multiple separate functional units. These blocks are interconnected in the MAC module. The block diagram shows the general flow of data and control signals between these blocks.
The GMAC transfers data to system memory through the AXI master interface. The host CPU uses the APB Slave interface to access the GMAC subsystem's control and status registers (CSRs).
The GMAC supports the PHY interfaces of reduced GMII (RGMII) and reduced MII (RMII).
The Transmit FIFO (Tx FIFO) buffers data read from system memory by the DMA before transmission by the GMAC Core. Similarly, the Receive FIFO (Rx FIFO) stores the Ethernet frames received from the line until they are transferred to system memory by the DMA. These are asynchronous FIFOs, as they also transfer the data between the application clock and the GMAC line clocks.

12.3 Function Description

12.3.1 Frame Structure

Data frames transmitted shall have the frame format shown in Fig. 25-2.



Fig. 12-2 MAC Block Diagram

The preamble <preamble> begins a frame transmission. The bit value of the preamble field consists of 7 octets with the following bit values:
10101010 10101010 10101010 10101010 10101010 10101010 10101010
The SFD (start frame delimiter) <sfd> indicates the start of a frame and follows the preamble. The bit value is 10101011.
The data in a well formed frame shall consist of N octet's data.

12.3.2 RMII Interface timing diagram

The Reduced Media Independent Interface (RMII) specification reduces the pin count between Ethernet PHYs and Switch ASICs (only in 10/100 mode). According to the IEEE 802.3u standard, an MII contains 16 pins for data and control. In devices incorporating multiple MAC or PHY interfaces (such as switches), the number of pins adds significant cost with increase in port count. The RMII specification addresses this problem by reducing the pin count to 7 for each port - a 62.5% decrease in pin count.
The RMII module is instantiated between the GMAC and the PHY. This helps translation of the MAC's MII into the RMII. The RMII block has the following characteristics:

- Supports 10-Mbps and 100-Mbps operating rates. It does not support 1000-Mbps operation.
- Two clock references are sourced externally or CRU, providing independent, 2-bit wide transmit and receive paths.

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Transmit Bit Ordering

Each nibble from the MII must be transmitted on the RMII a di-bit at a time with the order of di-bit transmission shown in Fig.1-3. The lower order bits (D1 and D0) are transmitted first followed by higher order bits (D2 and D3).

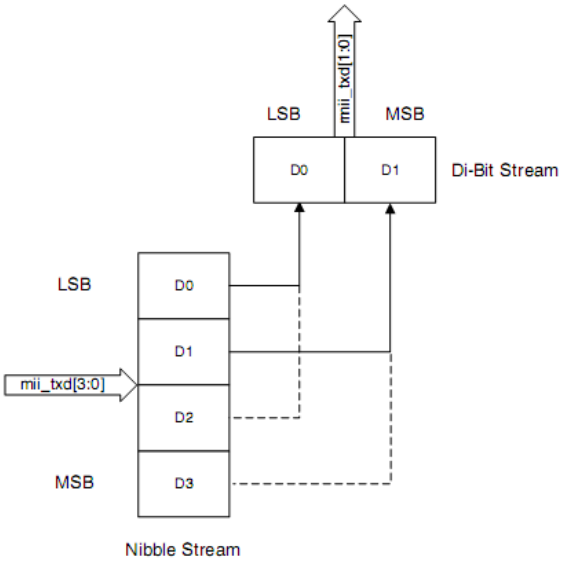


Fig. 12-3 RMII transmission bit ordering

RMII Transmit Timing Diagrams

Fig.1-4 through 1-7 show MII-to-RMII transaction timing. The clk_rmii_i (REF_CLK) frequency is 50MHz in RMII interface. In 10Mb/s mode, as the REF_CLK frequency is 10 times as the data rate, the value on rmii_txd_o[1:0] (TXD[1:0]) shall be valid such that TXD[1:0] may be sampled every 10th cycle, regard-less of the starting cycle within the group and yield the correct frame data.

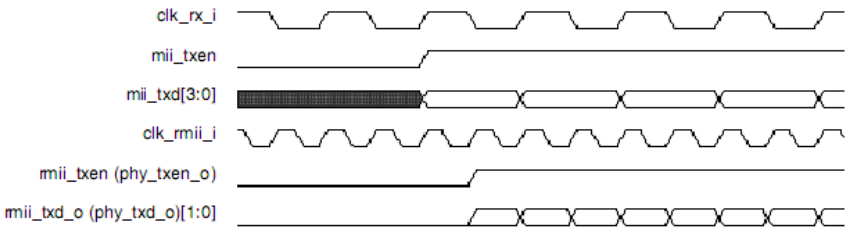


Fig. 12-4 Start of MII and RMII transmission in 100-Mbps mode

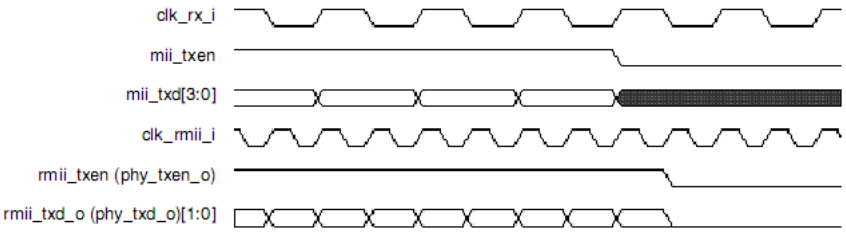


Fig. 12-5 End of MII and RMII Transmission in 100-Mbps Mode

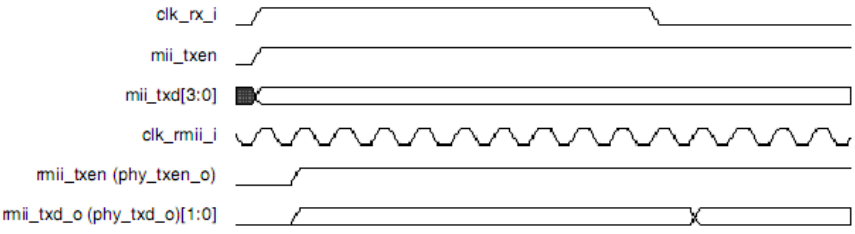


Fig. 12-6 Start of MII and RMII Transmission in 10-Mbps Mode

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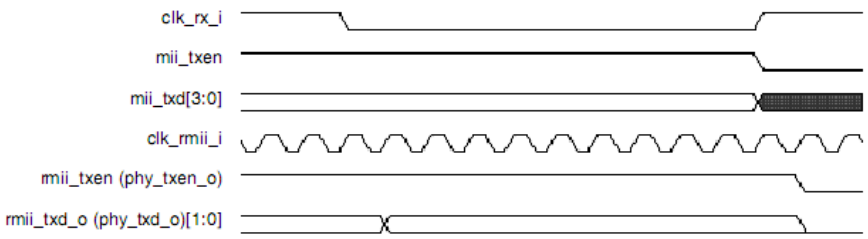


Fig. 12-7 End of MII and RMII Transmission in 10-Mbps Mode

Receive Bit Ordering

Each nibble is transmitted to the MII from the di-bit received from the RMII in the nibble transmission order shown in Fig.1-8. The lower order bits (D0 and D1) are received first, followed by the higher order bits (D2 and D3).

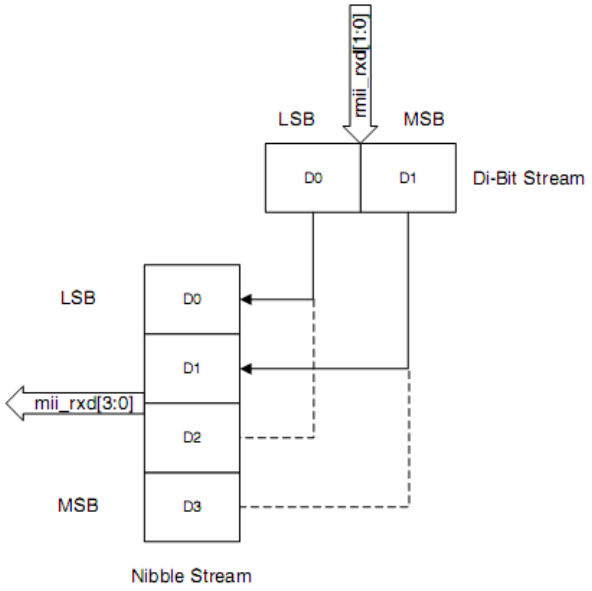


Fig. 12-8 RMII receive bit ordering

12.3.3 RGMII interface

The Reduced Gigabit Media Independent Interface (RGMII) specification reduces the pin count of the interconnection between the GMAC 10/100/1000 controller and the PHY for GMII and MII interfaces. To achieve this, the data path and control signals are reduced and multiplexed together with both the edges of the transmission and receive clocks. For gigabit operation the clocks operate at 125 MHz; for 10/100 operation, the clock rates are 2.5 MHz/25 MHz.

In the GMAC 10/100/1000 controller, the RGMII module is instantiated between the GMAC core's GMII and the PHY to translate the control and data signals between the GMII and RGMII protocols.

The RGMII block has the following characteristics:

- Supports 10-Mbps, 100-Mbps, and 1000-Mbps operation rates.
- For the RGMII block, no extra clock is required because both the edges of the incoming clocks are used.
- The RGMII block extracts the in-band (link speed, duplex mode and link status) status signals from the PHY and provides them to the GMAC core logic for link detection.

12.3.4 Management Interface

The MAC management interface provides a simple, two-wire, serial interface to connect the GMAC and a managed PHY, for the purposes of controlling the PHY and gathering status from the PHY. The management interface consists of a pair of signals that transport the management information across the MII bus: MDIO and MDC.

The GMAC initiates the management write/read operation. The clock gmii_mdc_o(MDC) is a divided clock from the application clock pclk_gmac. The divide factor depends on the clock

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range setting in the GMII address register. Clock range is set as follows:

Selection	pclk_gmac	MDC Clock
0000	60-100 MHz	pclk_gmac/42
0001	100-150 MHz	pclk_gmac/62
0010	20-35 MHz	pclk_gmac/16
0011	35-60 MHz	pclk_gmac/26
0100	150-250 MHz	pclk_gmac/102
0101	250-300 MHz	pclk_gmac/124
0110, 0111	Reserved	

The MDC is the derivative of the application clock pclk_gmac. The management operation is performed through the gmii_mdi_i, gmii_mdo_o and gmii_mdo_o_e signals. A three-state buffer is implemented in the PAD.
The frame structure on the MDIO line is shown below.

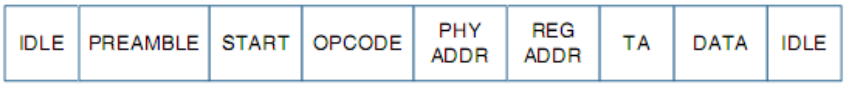


Fig. 12-9 MDIO frame structure

IDLE: The mdio line is three-state; there is no clock on gmii_mdc_o
PREAMBLE: 32 continuous bits of value 1
START: Start-of-frame is 2'b01
OPCODE: 2'b10 for read and 2'b01 for write
PHY ADDR: 5-bit address select for one of 32 PHYs
REG ADDR: Register address in the selected PHY
TA: Turnaround is 2'bZ0 for read and 2'b10 for Write
DATA: Any 16-bit value. In a write operation, the GMAC drives mdio; in a read operation, PHY drives it.

12.3.5 Power Management Block

Power management (PMT) supports the reception of network (remote) wake-up frames and Magic Packet frames. PMT does not perform the clock gate function, but generates interrupts for wake-up frames and Magic Packets received by the GMAC. The PMT block sits on the receiver path of the GMAC and is enabled with remote wake-up frame enable and Magic Packet enable. These enables are in the PMT control and status register and are programmed by the application.
When the power down mode is enabled in the PMT, then all received frames are dropped by the core and they are not forwarded to the application. The core comes out of the power down mode only when either a Magic Packet or a Remote Wake-up frame is received and the corresponding detection is enabled.

Remote Wake-Up Frame Detection

When the GMAC is in sleep mode and the remote wake-up bit is enabled in register GMAC_PMT_CTRL_STA (0x002C), normal operation is resumed after receiving a remote wake-up frame. The application writes all eight wake-up filter registers, by performing a sequential write to address (0028). The application enables remote wake-up by writing a 1 to bit 2 of the register GMAC_PMT_CTRL_STA.
PMT supports four programmable filters that allow support of different receive frame patterns. If the incoming frame passes the address filtering of Filter Command, and if Filter CRC-16 matches the incoming examined pattern, then the wake-up frame is received. Filter_offset (minimum value 12, which refers to the 13th byte of the frame) determines the offset from which the frame is to be examined. Filter Byte Mask determines which bytes of the frame must be examined. The thirty-first bit of Byte Mask must be set to zero.
The remote wake-up CRC block determines the CRC value that is compared with Filter CRC-16. The wake-up frame is checked only for length error, FCS error, dribble bit error, GMII error, collision, and to ensure that it is not a runt frame. Even if the wake-up frame is more than 512 bytes long, if the frame has a valid CRC value, it is considered valid. Wake-up frame detection is updated in the register GMAC_PMT_CTRL_STA for every remote Wake-up frame received. A PMT interrupt to the application triggers a read to the GMAC_PMT_CTRL_STA register to determine reception of a wake-up frame.

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Magic Packet Detection

The Magic Packet frame is based on a method that uses Advanced Micro Device's Magic Packet technology to power up the sleeping device on the network. The GMAC receives a specific packet of information, called a Magic Packet, addressed to the node on the network.

Only Magic Packets that are addressed to the device or a broadcast address will be checked to determine whether they meet the wake-up requirements. Magic Packets that pass the address filtering (unicast or broadcast) will be checked to determine whether they meet the remote Wake-on-LAN data format of 6 bytes of all ones followed by a GMAC Address appearing 16 times.

The application enables Magic Packet wake-up by writing a 1 to Bit 1 of the register GMAC_PMT_CTRL_STA. The PMT block constantly monitors each frame addressed to the node for a specific Magic Packet pattern. Each frame received is checked for a 48'hFF_FF_FF_FF_FF_FF pattern following the destination and source address field. The PMT block then checks the frame for 16 repetitions of the GMAC address without any breaks or interruptions. In case of a break in the 16 repetitions of the address, the 48'hFF_FF_FF_FF_FF_FF pattern is scanned for again in the incoming frame. The 16 repetitions can be anywhere in the frame, but must be preceded by the synchronization stream (48'hFF_FF_FF_FF_FF_FF). The device will also accept a multicast frame, as long as the 16 duplications of the GMAC address are detected.

If the MAC address of a node is 48'h00_11_22_33_44_55, then the GMAC scans for the data sequence:

Destination Address Source Address …… FF FF FF FF FF FF
00 11 22 33 44 55 00 11 22 33 44 55 00 11 22 33 44 55 00 11 22 33 44 55
00 11 22 33 44 55 00 11 22 33 44 55 00 11 22 33 44 55 00 11 22 33 44 55
00 11 22 33 44 55 00 11 22 33 44 55 00 11 22 33 44 55 00 11 22 33 44 55
00 11 22 33 44 55 00 11 22 33 44 55 00 11 22 33 44 55 00 11 22 33 44 55
…CRC

Magic Packet detection is updated in the PMT Control and Status register for Magic Packet received. A PMT interrupt to the Application triggers a read to the PMT CSR to determine whether a Magic Packet frame has been received.

12.3.6 MAC Management Counters

The counters in the MAC Management Counters (MMC) module can be viewed as an extension of the register address space of the CSR module. The MMC module maintains a set of registers for gathering statistics on the received and transmitted frames. These include a control register for controlling the behavior of the registers, two 32-bit registers containing interrupts generated (receive and transmit), and two 32-bit registers containing masks for the Interrupt register (receive and transmit). These registers are accessible from the Application through the MAC Control Interface (MCI). Non-32-bit accesses are allowed as long as the address is word-aligned.

The organization of these registers is shown in Register Description. The MMCs are accessed using transactions, in the same way the CSR address space is accessed. The Register Description in this chapter describe the various counters and list the address for each of the statistics counters. This address will be used for Read/Write accesses to the desired transmit/receive counter.

The MMC module gathers statistics on encapsulated IPv4, IPv6, TCP, UDP, or ICMP payloads in received Ethernet frames.

12.4 Register Description

12.4.1 Registers Summary

Name	Offset	Size	Reset Value	Description
GMAC_MAC_CONF	0x0000	W	0x00000000	MAC Configuration Register
GMAC_MAC_FRM_FILT	0x0004	W	0x00000000	MAC Frame Filter

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Name	Offset	Size	Reset Value	Description
GMAC_HASH_TAB_HI	0x0008	W	0x00000000	Hash Table High Register
GMAC_HASH_TAB_LO	0x000c	W	0x00000000	Hash Table Low Register
GMAC_GMII_ADDR	0x0010	W	0x00000000	GMII Address Register
GMAC_GMII_DATA	0x0014	W	0x00000000	GMII Data Register
GMAC_FLOW_CTRL	0x0018	W	0x00000000	Flow Control Register
GMAC_VLAN_TAG	0x001c	W	0x00000000	VLAN Tag Register
GMAC_DEBUG	0x0024	W	0x00000000	Debug register
GMAC_PMT_CTRL_STA	0x002c	W	0x00000000	PMT Control and Status Register
GMAC_INT_STATUS	0x0038	W	0x00000000	Interrupt Status Register
GMAC_INT_MASK	0x003c	W	0x00000000	Interrupt Mask Register
GMAC_MAC_ADDR0_HI	0x0040	W	0x0000ffff	MAC Address0 High Register
GMAC_MAC_ADDR0_LO	0x0044	W	0xffffffff	MAC Address0 Low Register
GMAC_AN_CTRL	0x00c0	W	0x00000000	AN Control Register
GMAC_AN_STATUS	0x00c4	W	0x00000008	AN Status Register
GMAC_AN_ADV	0x00c8	W	0x000001e0	Auto Negotiation Advertisement Register
GMAC_AN_LINK_PART_AB	0x00cc	W	0x00000000	Auto Negotiation Link Partner Ability Register
GMAC_AN_EXP	0x00d0	W	0x00000000	Auto Negotiation Expansion Register
GMAC_INTF_MODE_STA	0x00d8	W	0x00000000	RGMII Status Register
GMAC_MMC_CTRL	0x0100	W	0x00000000	MMC Control Register
GMAC_MMC_RX_INTR	0x0104	W	0x00000000	MMC Receive Interrupt Register
GMAC_MMC_TX_INTR	0x0108	W	0x00000000	MMC Transmit Interrupt Register
GMAC_MMC_RX_INT_MSK	0x010c	W	0x00000000	MMC Receive Interrupt Mask Register
GMAC_MMC_TX_INT_MSK	0x0110	W	0x00000000	MMC Transmit Interrupt Mask Register
GMAC_MMC_TXOCTETCNT_GB	0x0114	W	0x00000000	MMC TX OCTET Good and Bad Counter
GMAC_MMC_TXFRMCNT_GB	0x0118	W	0x00000000	MMC TX Frame Good and Bad Counter
GMAC_MMC_TXUNDFLWERR	0x0148	W	0x00000000	MMC TX Underflow Error
GMAC_MMC_TXCARERR	0x0160	W	0x00000000	MMC TX Carrier Error
GMAC_MMC_TXOCTETCNT_G	0x0164	W	0x00000000	MMC TX OCTET Good Counter
GMAC_MMC_TXFRMCNT_G	0x0168	W	0x00000000	MMC TX Frame Good Counter
GMAC_MMC_RXFRMCNT_GB	0x0180	W	0x00000000	MMC RX Frame Good and Bad Counter
GMAC_MMC_RXOCTETCNT_GB	0x0184	W	0x00000000	MMC RX OCTET Good and Bad Counter

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Name	Offset	Size	Reset Value	Description
GMAC_MMC_RXOCTETCNT_G	0x0188	W	0x00000000	MMC RX OCTET Good Counter
GMAC_MMC_RXMCFRMCNT_G	0x0190	W	0x00000000	MMC RX Multicast Frame Good Counter
GMAC_MMC_RXCRCERR	0x0194	W	0x00000000	MMC RX Carrier
GMAC_MMC_RXLENERR	0x01c8	W	0x00000000	MMC RX Length Error
GMAC_MMC_RXFIFOOVRFLW	0x01d4	W	0x00000000	MMC RX FIFO Overflow
GMAC_MMC_IPC_INT_MSK	0x0200	W	0x00000000	MMC Receive Checksum Offload Interrupt Mask Register
GMAC_MMC_IPC_INTR	0x0208	W	0x00000000	MMC Receive Checksum Offload Interrupt Register
GMAC_MMC_RXIPV4GFRM	0x0210	W	0x00000000	MMC RX IPV4 Good Frame
GMAC_MMC_RXIPV4HDERRFRM	0x0214	W	0x00000000	MMC RX IPV4 Head Error Frame
GMAC_MMC_RXIPV6GFRM	0x0224	W	0x00000000	MMC RX IPV6 Good Frame
GMAC_MMC_RXIPV6HDERRFRM	0x0228	W	0x00000000	MMC RX IPV6 Head Error Frame
GMAC_MMC_RXUDPERRFRM	0x0234	W	0x00000000	MMC RX UDP Error Frame
GMAC_MMC_RXTCPERRFRM	0x023c	W	0x00000000	MMC RX TCP Error Frame
GMAC_MMC_RXICMPERRFRM	0x0244	W	0x00000000	MMC RX ICMP Error Frame
GMAC_MMC_RXIPV4HDERROCT	0x0254	W	0x00000000	MMC RX OCTET IPV4 Head Error
GMAC_MMC_RXIPV6HDERROCT	0x0268	W	0x00000000	MMC RX OCTET IPV6 Head Error
GMAC_MMC_RXUDPERROCT	0x0274	W	0x00000000	MMC RX OCTET UDP Error
GMAC_MMC_RXTCPERROCT	0x027c	W	0x00000000	MMC RX OCTET TCP Error
GMAC_MMC_RXICMPERROCT	0x0284	W	0x00000000	MMC RX OCTET ICMP Error
GMAC_BUS_MODE	0x1000	W	0x00020101	Bus Mode Register
GMAC_TX_POLL_DEMAND	0x1004	W	0x00000000	Transmit Poll Demand Register
GMAC_RX_POLL_DEMAND	0x1008	W	0x00000000	Receive Poll Demand Register
GMAC_RX_DESC_LIST_ADDR	0x100c	W	0x00000000	Receive Descriptor List Address Register
GMAC_TX_DESC_LIST_ADDR	0x1010	W	0x00000000	Transmit Descriptor List Address Register
GMAC_STATUS	0x1014	W	0x00000000	Status Register
GMAC_OP_MODE	0x1018	W	0x00000000	Operation Mode Register
GMAC_INT_ENA	0x101c	W	0x00000000	Interrupt Enable Register

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Name	Offset	Size	Reset Value	Description
GMAC_OVERFLOW_CNT	0x1020	W	0x00000000	Missed Frame and Buffer Overflow Counter Register
GMAC_REC_INT_WDT_TIMER	0x1024	W	0x00000000	Receive Interrupt Watchdog Timer Register
GMAC_AXI_BUS_MODE	0x1028	W	0x00110001	AXI Bus Mode Register
GMAC_AXI_STATUS	0x102c	W	0x00000000	AXI Status Register
GMAC_CUR_HOST_TX_DESC	0x1048	W	0x00000000	Current Host Transmit Descriptor Register
GMAC_CUR_HOST_RX_DESC	0x104c	W	0x00000000	Current Host Receive Descriptor Register
GMAC_CUR_HOST_TX_BUF_ADDR	0x1050	W	0x00000000	Current Host Transmit Buffer Address Register
GMAC_CUR_HOST_RX_BUF_ADDR	0x1054	W	0x00000000	Current Host Receive Buffer Address Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

12.4.2 Detail Register Description

GMAC_MAC_CONF

Address: Operational Base + offset (0x0000)

MAC Configuration Register

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24	RW	0x0	TC Transmit Configuration in RGMII When set, this bit enables the transmission of duplex mode, link speed, and link up/down information to the PHY in the RGMII ports. When this bit is reset, no such information is driven to the PHY.
23	RW	0x0	WD Watchdog Disable When this bit is set, the GMAC disables the watchdog timer on the receiver, and can receive frames of up to 16,384 bytes. When this bit is reset, the GMAC allows no more than 2,048 bytes (10,240 if JE is set high) of the frame being received and cuts off any bytes received after that.
22	RW	0x0	JD Jabber Disable When this bit is set, the GMAC disables the jabber timer on the transmitter, and can transfer frames of up to 16,384 bytes. When this bit is reset, the GMAC cuts off the transmitter if the application sends out more than 2,048 bytes of data (10,240 if JE is set high) during transmission.

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Bit	Attr	Reset Value	Description
21	RW	0x0	BE Frame Burst Enable When this bit is set, the GMAC allows frame bursting during transmission in GMII Half-Duplex mode.
20	RO	0x0	reserved
19:17	RW	0x0	IFG Inter-Frame Gap These bits control the minimum IFG between frames during transmission. 3'b000: 96 bit times 3'b001: 88 bit times 3'b010: 80 bit times ... 3'b111: 40 bit times
16	RW	0x0	DCRS Disable Carrier Sense During Transmission When set high, this bit makes the MAC transmitter ignore the (G)MII CRS signal during frame transmission in Half-Duplex mode. This request results in no errors generated due to Loss of Carrier or No Carrier during such transmission. When this bit is low, the MAC transmitter generates such errors due to Carrier Sense and will even abort the transmissions.
15	RW	0x0	PS Port Select Selects between GMII and MII: 1'b0: GMII (1000 Mbps) 1'b1: MII (10/100 Mbps)
14	RW	0x0	FES Speed Indicates the speed in Fast Ethernet (MII) mode: 1'b0: 10 Mbps 1'b1: 100 Mbps
13	RW	0x0	DO Disable Receive Own When this bit is set, the GMAC disables the reception of frames when the gmii_txen_o is asserted in Half-Duplex mode. When this bit is reset, the GMAC receives all packets that are given by the PHY while transmitting.
12	RW	0x0	LM Loopback Mode When this bit is set, the GMAC operates in loopback mode at GMII/MII. The (G)MII Receive clock input (clk_rx_i) is required for the loopback to work properly, as the Transmit clock is not looped-back internally.

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Bit	Attr	Reset Value	Description
11	RW	0x0	DM Duplex Mode When this bit is set, the GMAC operates in a Full-Duplex mode where it can transmit and receive simultaneously. This bit is RO with default value of 1'b1 in Full-Duplex-only configuration.
10	RW	0x0	IPC Checksum Offload When this bit is set, the GMAC calculates the 16-bit one's complement of the one's complement sum of all received Ethernet frame payloads. It also checks whether the IPv4 Header checksum (assumed to be bytes 25-26 or 29-30 (VLAN-tagged) of the received Ethernet frame) is correct for the received frame and gives the status in the receive status word. The GMAC core also appends the 16-bit checksum calculated for the IP header datagram payload (bytes after the IPv4 header) and appends it to the Ethernet frame transferred to the application (when Type 2 COE is deselected). When this bit is reset, this function is disabled. When Type 2 COE is selected, this bit, when set, enables IPv4 checksum checking for received frame payloads TCP/UDP/ICMP headers. When this bit is reset, the COE function in the receiver is disabled and the corresponding PCE and IP HCE status bits are always cleared.
9	RW	0x0	DR Disable Retry When this bit is set, the GMAC will attempt only 1 transmission. When a collision occurs on the GMII/MII, the GMAC will ignore the current frame transmission and report a Frame Abort with excessive collision error in the transmit frame status. When this bit is reset, the GMAC will attempt retries based on the settings of BL.
8	RW	0x0	LUD Link Up/Down Indicates whether the link is up or down during the transmission of configuration in RGMII interface: 1'b0: Link Down 1'b1: Link Up
7	RW	0x0	ACS Automatic Pad/CRC Stripping When this bit is set, the GMAC strips the Pad/FCS field on incoming frames only if the length's field value is less than or equal to 1,500 bytes. All received frames with length field greater than or equal to 1,501 bytes are passed to the application without stripping the Pad/FCS field. When this bit is reset, the GMAC will pass all incoming frames to the Host unmodified.

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Bit	Attr	Reset Value	Description
6:5	RW	0x0	BL Back-Off Limit The Back-Off limit determines the random integer number (r) of slot time delays (4,096 bit times for 1000 Mbps and 512 bit times for 10/100 Mbps) the GMAC waits before rescheduling a transmission attempt during retries after a collision. This bit is applicable only to Half-Duplex mode and is reserved (RO) in Full-Duplex-only configuration. 2'b00: k = min (n, 10) 2'b01: k = min (n, 8) 2'b10: k = min (n, 4) 2'b11: k = min (n, 1), Where n = retransmission attempt. The random integer r takes the value in the range 0 = r < 2^k
4	RW	0x0	DC Deferral Check When this bit is set, the deferral check function is enabled in the GMAC. The GMAC will issue a Frame Abort status, along with the excessive deferral error bit set in the transmit frame status when the transmission state machine is deferred for more than 24,288 bit times in 10/100-Mbps mode. If the Core is configured for 1000 Mbps operation, the threshold for deferral is 155,680 bits times. Deferral begins when the transmitter is ready to transmit, but is prevented because of an active CRS (carrier sense) signal on the GMII/MII. Defer time is not cumulative. If the transmitter defers for 10,000 bit times, then transmits, collides, backs off, and then has to defer again after completion of back-off, the deferral timer resets to 0 and restarts. When this bit is reset, the deferral check function is disabled and the GMAC defers until the CRS signal goes inactive.
3	RW	0x0	TE Transmitter Enable When this bit is set, the transmission state machine of the GMAC is enabled for transmission on the GMII/MII. When this bit is reset, the GMAC transmit state machine is disabled after the completion of the transmission of the current frame, and will not transmit any further frames.
2	RW	0x0	RE Receiver Enable When this bit is set, the receiver state machine of the GMAC is enabled for receiving frames from the GMII/MII. When this bit is reset, the GMAC receive state machine is disabled after the completion of the reception of the current frame, and will not receive any further frames from the GMII/MII.
1:0	RO	0x0	reserved

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GMAC_MAC_FRM_FILT
Address: Operational Base + offset (0x0004)
MAC Frame Filter

Bit	Attr	Reset Value	Description
31	RW	0x0	RA Receive All When this bit is set, the GMAC Receiver module passes to the Application all frames received irrespective of whether they pass the address filter. The result of the SA/DA filtering is updated (pass or fail) in the corresponding bits in the Receive Status Word. When this bit is reset, the Receiver module passes to the Application only those frames that pass the SA/DA address filter.
30:11	RO	0x0	reserved
10	RW	0x0	HPF Hash or Perfect Filter When set, this bit configures the address filter to pass a frame if it matches either the perfect filtering or the hash filtering as set by HMC or HUC bits. When low and if the HUC/HMC bit is set, the frame is passed only if it matches the Hash filter.
9	RW	0x0	SAF Source Address Filter Enable The GMAC core compares the SA field of the received frames with the values programmed in the enabled SA registers. If the comparison matches, then the SAMatch bit of RxStatus Word is set high. When this bit is set high and the SA filter fails, the GMAC drops the frame. When this bit is reset, then the GMAC Core forwards the received frame to the application and with the updated SA Match bit of the RxStatus depending on the SA address comparison.
8	RW	0x0	SAIF SA Inverse Filtering When this bit is set, the Address Check block operates in inverse filtering mode for the SA address comparison. The frames whose SA matches the SA registers will be marked as failing the SA Address filter. When this bit is reset, frames whose SA does not match the SA registers will be marked as failing the SA Address filter.

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Bit	Attr	Reset Value	Description
7:6	RW	0x0	PCF Pass Control Frames These bits control the forwarding of all control frames (including unicast and multicast PAUSE frames). Note that the processing of PAUSE control frames depends only on RFE of Register GMAC_FLOW_CTRL[2]. 2'b00: GMAC filters all control frames from reaching the application. 2'b01: GMAC forwards all control frames except PAUSE control frames to application even if they fail the Address filter. 2'b10: GMAC forwards all control frames to application even if they fail the Address Filter. 2'b11: GMAC forwards control frames that pass the Address Filter.
5	RW	0x0	DBF Disable Broadcast Frames When this bit is set, the AFM module filters all incoming broadcast frames. When this bit is reset, the AFM module passes all received broadcast frames.
4	RW	0x0	PM Pass All Multicast When set, this bit indicates that all received frames with a multicast destination address (first bit in the destination address field is '1') are passed. When reset, filtering of multicast frame depends on HMC bit.
3	RW	0x0	DAIF DA Inverse Filtering When this bit is set, the Address Check block operates in inverse filtering mode for the DA address comparison for both unicast and multicast frames. When reset, normal filtering of frames is performed.
2	RW	0x0	HMC Hash Multicast When set, MAC performs destination address filtering of received multicast frames according to the hash table. When reset, the MAC performs a perfect destination address filtering for multicast frames, that is, it compares the DA field with the values programmed in DA registers.
1	RW	0x0	HUC Hash Unicast When set, MAC performs destination address filtering of unicast frames according to the hash table. When reset, the MAC performs a perfect destination address filtering for unicast frames, that is, it compares the DA field with the values programmed in DA registers.

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Bit	Attr	Reset Value	Description
0	RW	0x0	PR Promiscuous Mode When this bit is set, the Address Filter module passes all incoming frames regardless of its destination or source address. The SA/DA Filter Fails status bits of the Receive Status Word will always be cleared when PR is set.

GMAC_HASH_TAB_HI
Address: Operational Base + offset (0x0008)
Hash Table High Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	HTH Hash Table High This field contains the upper 32 bits of Hash table

GMAC_HASH_TAB_LO
Address: Operational Base + offset (0x000c)
Hash Table Low Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	HTL Hash Table Low This field contains the lower 32 bits of Hash table

GMAC_GMII_ADDR
Address: Operational Base + offset (0x0010)
GMII Address Register

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:11	RW	0x00	PA Physical Layer Address This field tells which of the 32 possible PHY devices are being accessed
10:6	RW	0x00	GR GMII Register These bits select the desired GMII register in the selected PHY device

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Bit	Attr	Reset Value	Description
5:2	RW	0x0	CR APB Clock Range The APB Clock Range selection determines the frequency of the MDC clock as per the pclk_gmac frequency used in your design. The suggested range of pclk_gmac frequency applicable for each value below (when Bit[5] = 0) ensures that the MDC clock is approximately between the frequency range 1.0 MHz - 2.5 MHz. **Selection** **pclk_gmac** **MDC Clock** 0000 60-100 MHz pclk_gmac/42 0001 100-150 MHz pclk_gmac/62 0010 20-35 MHz pclk_gmac/16 0011 35-60 MHz pclk_gmac/26 0100 150-250 MHz pclk_gmac/102 0101 250-300 MHz pclk_gmac/124 0110, 0111 Reserved When bit 5 is set, you can achieve MDC clock of frequency higher than the IEEE 802.3 specified frequency limit of 2.5 MHz and program a clock divider of lower value. For example, when pclk_gmac is of frequency 100 MHz and you program these bits as "1010", then the resultant MDC clock will be of 12.5 MHz which is outside the limit of IEEE 802.3 specified range. Please program the values given below only if the interfacing chips supports faster MDC clocks. **Selection** **MDC Clock** 1000 pclk_gmac/4 1001 pclk_gmac/6 1010 pclk_gmac/8 1011 pclk_gmac/10 1100 pclk_gmac/12 1101 pclk_gmac/14 1110 pclk_gmac/16 1111 pclk_gmac/18
1	RW	0x0	GW GMII Write When set, this bit tells the PHY that this will be a Write operation using register GMAC_GMII_DATA. If this bit is not set, this will be a Read operation, placing the data in register GMAC_GMII_DATA.

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Bit	Attr	Reset Value	Description
0	W1C	0x0	GB GMII Busy This bit should read a logic 0 before writing to Register GMII_ADDR and Register GMII_DATA. This bit must also be set to 0 during a Write to Register GMII_ADDR. During a PHY register access, this bit will be set to 1'b1 by the Application to indicate that a Read or Write access is in progress. Register GMII_DATA (GMII Data) should be kept valid until this bit is cleared by the GMAC during a PHY Write operation. The Register GMII_DATA is invalid until this bit is cleared by the GMAC during a PHY Read operation. The Register GMII_ADDR (GMII Address) should not be written to until this bit is cleared.

GMAC_GMII_DATA
Address: Operational Base + offset (0x0014)
GMII Data Register

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0000	GD GMII Data This contains the 16-bit data value read from the PHY after a Management Read operation or the 16-bit data value to be written to the PHY before a Management Write operation.

GMAC_FLOW_CTRL
Address: Operational Base + offset (0x0018)
Flow Control Register

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	PT Pause Time This field holds the value to be used in the Pause Time field in the transmit control frame. If the Pause Time bits is configured to be double-synchronized to the (G)MII clock domain, then consecutive writes to this register should be performed only after at least 4 clock cycles in the destination clock domain.
15:8	RO	0x0	reserved
7	RW	0x0	DZPQ Disable Zero-Quanta Pause When set, this bit disables the automatic generation of Zero-Quanta Pause Control frames on the de-assertion of the flow-control signal from the FIFO layer (MTL or external sideband flow control signal sbd_flowctrl_i/mti_flowctrl_i). When this bit is reset, normal operation with automatic Zero-Quanta Pause Control frame generation is enabled.
6	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
5:4	RW	0x0	PLT Pause Low Threshold This field configures the threshold of the PAUSE timer at which the input flow control signal mti_flowctrl_i (or sbd_flowctrl_i) is checked for automatic retransmission of PAUSE Frame. The threshold values should be always less than the Pause Time configured in Bits[31:16]. For example, if PT = 100H (256 slot-times), and PLT = 01, then a second PAUSE frame is automatically transmitted if the mti_flowctrl_i signal is asserted at 228 (256-28) slot-times after the first PAUSE frame is transmitted. **Selection Threshold** 00 Pause time minus 4 slot times 01 Pause time minus 28 slot times 10 Pause time minus 144 slot times 11 Pause time minus 256 slot times Slot time is defined as time taken to transmit 512 bits (64 bytes) on the GMII/MII interface.
3	RW	0x0	UP Unicast Pause Frame Detect When this bit is set, the GMAC will detect the Pause frames with the station's unicast address specified in MAC Address0 High Register and MAC Address0 Low Register, in addition to the detecting Pause frames with the unique multicast address. When this bit is reset, the GMAC will detect only a Pause frame with the unique multicast address specified in the 802.3x standard.
2	RW	0x0	RFE Receive Flow Control Enable When this bit is set, the GMAC will decode the received Pause frame and disable its transmitter for a specified (Pause Time) time. When this bit is reset, the decode function of the Pause frame is disabled.
1	RW	0x0	TFE Transmit Flow Control Enable In Full-Duplex mode, when this bit is set, the GMAC enables the flow control operation to transmit Pause frames. When this bit is reset, the flow control operation in the GMAC is disabled, and the GMAC will not transmit any Pause frames. In Half-Duplex mode, when this bit is set, the GMAC enables the back-pressure operation. When this bit is reset, the backpressure feature is disabled.

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Bit	Attr	Reset Value	Description
0	RW	0x0	FCB_BPA Flow Control Busy/Backpressure Activate This bit initiates a Pause Control frame in Full-Duplex mode and activates the backpressure function in Half-Duplex mode if TFE bit is set. In Full-Duplex mode, this bit should be read as 1'b0 before writing to the register GMAC_FLOW_CTRL. To initiate a pause control frame, the application must set this bit to 1'b1. During a transfer of the control frame, this bit will continue to be set to signify that a frame transmission is in progress. After the completion of Pause control frame transmission, the GMAC will reset this bit to 1'b0. The register GMAC_FLOW_CTRL should not be written to until this bit is cleared. In Half-Duplex mode, when this bit is set (and TFE is set), then backpressure is asserted by the GMAC Core. During backpressure, when the GMAC receives a new frame, the transmitter starts sending a JAM pattern resulting in a collision. This control register bit is logically OR'ed with the mti_flowctrl_i input signal for the backpressure function.

GMAC_VLAN_TAG
Address: Operational Base + offset (0x001c)
VLAN Tag Register

Bit	Attr	Reset Value	Description
31:17	RO	0x0	reserved
16	RW	0x0	ETV Enable 12-Bit VLAN Tag Comparison When this bit is set, a 12-bit VLAN identifier, rather than the complete 16-bit VLAN tag, is used for comparison and filtering. Bits[11:0] of the VLAN tag are compared with the corresponding field in the received VLAN-tagged frame. When this bit is reset, all 16 bits of the received VLAN frame's fifteenth and sixteenth bytes are used for comparison.
15:0	RW	0x0000	VL VLAN Tag Identifier for Receive Frames This contains the 802.1Q VLAN tag to identify VLAN frames, and is compared to the fifteenth and sixteenth bytes of the frames being received for VLAN frames. Bits[15:13] are the User Priority, Bit[12] is the Canonical Format Indicator (CFI) and bits[11:0] are the VLAN tag's VLAN Identifier (VID) field. When the ETV bit is set, only the VID (Bits[11:0]) is used for comparison. If VL (VL[11:0] if ETV is set) is all zeros, the GMAC does not check the fifteenth and sixteenth bytes for VLAN tag comparison, and declares all frames with a Type field value of 0x8100 to be VLAN frames.

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GMAC_DEBUG
Address: Operational Base + offset (0x0024)
Debug register

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25	RW	0x0	TFIFO3 When high, it indicates that the MTL TxStatus FIFO is full and hence the MTL will not be accepting any more frames for transmission.
24	RW	0x0	TFIFO2 When high, it indicates that the MTL TxFIFO is not empty and has some data left for transmission.
23	RO	0x0	reserved
22	RW	0x0	TFIFO1 When high, it indicates that the MTL TxFIFO Write Controller is active and transferring data to the TxFIFO.
21:20	RW	0x0	TFIFOSTA This indicates the state of the TxFIFO read Controller: 2'b00: IDLE state 2'b01: READ state (transferring data to MAC transmitter) 2'b10: Waiting for TxStatus from MAC transmitter 2'b11: Writing the received TxStatus or flushing the TxFIFO
19	RW	0x0	PAUSE When high, it indicates that the MAC transmitter is in PAUSE condition (in full-duplex only) and hence will not schedule any frame for transmission
18:17	RW	0x0	TSAT This indicates the state of the MAC Transmit Frame Controller module: 2'b00: IDLE 2'b01: Waiting for Status of previous frame or IFG/backoff period to be over 2'b10: Generating and transmitting a PAUSE control frame (in full duplex mode) 2'b11: Transferring input frame for transmission
16	RW	0x0	TACT When high, it indicates that the MAC GMII/MII transmit protocol engine is actively transmitting data and not in IDLE state.
15:10	RO	0x0	reserved
9:8	RW	0x0	RFIFO This gives the status of the RxFIFO Fill-level: 2'b00: RxFIFO Empty 2'b01: RxFIFO fill-level below flow-control de-activate threshold 2'b10: RxFIFO fill-level above flow-control activate threshold 2'b11: RxFIFO Full
7	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
6:5	RW	0x0	RFIFORD It gives the state of the RxFIFO read Controller: 2'b00: IDLE state 2'b01: Reading frame data 2'b10: Reading frame status (or time-stamp) 2'b11: Flushing the frame data and Status
4	RW	0x0	RFIFOWR When high, it indicates that the MTL RxFIFO Write Controller is active and transferring a received frame to the FIFO.
3	RO	0x0	reserved
2:1	RW	0x0	ACT When high, it indicates the active state of the small FIFO Read and Write controllers respectively of the MAC receive Frame Controller module
0	RW	0x0	RDB When high, it indicates that the MAC GMII/MII receive protocol engine is actively receiving data and not in IDLE state.

GMAC_PMT_CTRL_STA

Address: Operational Base + offset (0x002c)

PMT Control and Status Register

Bit	Attr	Reset Value	Description
31	W1C	0x0	WFFRPR Wake-Up Frame Filter Register Pointer Reset When set, resets the Remote Wake-up Frame Filter register pointer to 3'b000. It is automatically cleared after 1 clock cycle.
30:10	RO	0x0	reserved
9	RW	0x0	GU Global Unicast When set, enables any unicast packet filtered by the GMAC (DAF) address recognition to be a wake-up frame.
8:7	RO	0x0	reserved
6	RC	0x0	WFR Wake-Up Frame Received When set, this bit indicates the power management event was generated due to reception of a wake-up frame. This bit is cleared by a read into this register.
5	RC	0x0	MPR Magic Packet Received When set, this bit indicates the power management event was generated by the reception of a Magic Packet. This bit is cleared by a read into this register.
4:3	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
2	RW	0x0	WFE Wake-Up Frame Enable When set, enables generation of a power management event due to wake-up frame reception.
1	RW	0x0	MPE Magic Packet Enable When set, enables generation of a power management event due to Magic Packet reception.
0	R/WSC	0x0	PD Power Down When set, all received frames will be dropped. This bit is cleared automatically when a magic packet or Wake-Up frame is received, and Power-Down mode is disabled. Frames received after this bit is cleared are forwarded to the application. This bit must only be set when either the Magic Packet Enable or Wake-Up Frame Enable bit is set high.

GMAC_INT_STATUS
Address: Operational Base + offset (0x0038)
Interrupt Status Register

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7	RO	0x0	MRCOIS MMC Receive Checksum Offload Interrupt Status This bit is set high whenever an interrupt is generated in the MMC Receive Checksum Offload Interrupt Register. This bit is cleared when all the bits in this interrupt register are cleared.
6	RO	0x0	MTIS MMC Transmit Interrupt Status This bit is set high whenever an interrupt is generated in the MMC Transmit Interrupt Register. This bit is cleared when all the bits in this interrupt register are cleared. This bit is only valid when the optional MMC module is selected during configuration.
5	RO	0x0	MRIS MMC Receive Interrupt Status This bit is set high whenever an interrupt is generated in the MMC Receive Interrupt Register. This bit is cleared when all the bits in this interrupt register are cleared. This bit is only valid when the optional MMC module is selected during configuration.
4	RO	0x0	MIS MMC Interrupt Status This bit is set high whenever any of bits 7:5 is set high and cleared only when all of these bits are low. This bit is valid only when the optional MMC module is selected during configuration.

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Bit	Attr	Reset Value	Description
3	RO	0x0	PIS PMT Interrupt Status This bit is set whenever a Magic packet or Wake-on-LAN frame is received in Power-Down mode). This bit is cleared when both bits[6:5] are cleared due to a read operation to the register GMAC_PMT_CTRL_STA.
2:1	RO	0x0	reserved
0	RO	0x0	RIS RGMII Interrupt Status This bit is set due to any change in value of the Link Status of RGMII interface. This bit is cleared when the user makes a read operation the RGMII Status register.

GMAC_INT_MASK
Address: Operational Base + offset (0x003c)
Interrupt Mask Register

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3	RW	0x0	PIM PMT Interrupt Mask This bit when set, will disable the assertion of the interrupt signal due to the setting of PMT Interrupt Status bit in Register GMAC_INT_STATUS.
2:1	RO	0x0	reserved
0	RW	0x0	RIM RGMII Interrupt Mask This bit when set, will disable the assertion of the interrupt signal due to the setting of RGMII Interrupt Status bit in Register GMAC_INT_STATUS.

GMAC_MAC_ADDR0_HI
Address: Operational Base + offset (0x0040)
MAC Address0 High Register

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0xffff	A47_A32 MAC Address0 [47:32] This field contains the upper 16 bits (47:32) of the 6-byte first MAC address. This is used by the MAC for filtering for received frames and for inserting the MAC address in the Transmit Flow Control (PAUSE) Frames.

GMAC_MAC_ADDR0_LO
Address: Operational Base + offset (0x0044)
MAC Address0 Low Register

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Bit	Attr	Reset Value	Description
31:0	RW	0xffffffff	A31_A0 MAC Address0 [31:0] This field contains the lower 32 bits of the 6-byte first MAC address. This is used by the MAC for filtering for received frames and for inserting the MAC address in the Transmit Flow Control (PAUSE) Frames.

GMAC_AN_CTRL
Address: Operational Base + offset (0x00c0)
AN Control Register

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12	RW	0x0	ANE Auto-Negotiation Enable When set, will enable the GMAC to perform auto-negotiation with the link partner. Clearing this bit will disable auto-negotiation.
11:10	RO	0x0	reserved
9	R/W SC	0x0	RAN Restart Auto-Negotiation When set, will cause auto-negotiation to restart if the ANE is set. This bit is self-clearing after auto-negotiation starts. This bit should be cleared for normal operation.
8:0	RO	0x0	reserved

GMAC_AN_STATUS
Address: Operational Base + offset (0x00c4)
AN Status Register

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5	RO	0x0	ANC Auto-Negotiation Complete When set, this bit indicates that the auto-negotiation process is completed. This bit is cleared when auto-negotiation is reinitiated.
4	RO	0x0	reserved
3	RO	0x1	ANA Auto-Negotiation Ability This bit is always high, because the GMAC supports auto-negotiation.
2	R/W SC	0x0	LS Link Status When set, this bit indicates that the link is up. When cleared, this bit indicates that the link is down.
1:0	RO	0x0	reserved

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GMAC_AN_ADV
Address: Operational Base + offset (0x00c8)
Auto Negotiation Advertisement Register

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15	RO	0x0	NP Next Page Support This bit is tied to low, because the GMAC does not support the next page.
14	RO	0x0	reserved
13:12	RW	0x0	RFE Remote Fault Encoding These 2 bits provide a remote fault encoding, indicating to a link partner that a fault or error condition has occurred.
11:9	RO	0x0	reserved
8:7	RW	0x3	PSE Pause Encoding These 2 bits provide an encoding for the PAUSE bits, indicating that the GMAC is capable of configuring the PAUSE function as defined in IEEE 802.3x.
6	RW	0x1	HD Half-Duplex This bit, when set high, indicates that the GMAC supports Half-Duplex. This bit is tied to low (and RO) when the GMAC is configured for Full-Duplex-only operation.
5	RW	0x1	FD Full-Duplex This bit, when set high, indicates that the GMAC supports Full-Duplex.
4:0	RO	0x0	reserved

GMAC_AN_LINK_PART_AB
Address: Operational Base + offset (0x00cc)
Auto Negotiation Link Partner Ability Register

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15	RO	0x0	NP Next Page Support When set, this bit indicates that more next page information is available. When cleared, this bit indicates that next page exchange is not desired.

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Bit	Attr	Reset Value	Description
14	RO	0x0	ACK Acknowledge When set, this bit is used by the auto-negotiation function to indicate that the link partner has successfully received the GMAC's base page. When cleared, it indicates that a successful receipt of the base page has not been achieved.
13:12	RO	0x0	RFE Remote Fault Encoding These 2 bits provide a remote fault encoding, indicating a fault or error condition of the link partner.
11:9	RO	0x0	reserved
8:7	RO	0x0	PSE Pause Encoding These 2 bits provide an encoding for the PAUSE bits, indicating that the link partner's capability of configuring the PAUSE function as defined in IEEE 802.3x.
6	RO	0x0	HD Half-Duplex When set, this bit indicates that the link partner has the ability to operate in Half-Duplex mode. When cleared, the link partner does not have the ability to operate in Half-Duplex mode.
5	RO	0x0	FD Full-Duplex When set, this bit indicates that the link partner has the ability to operate in Full-Duplex mode. When cleared, the link partner does not have the ability to operate in Full-Duplex mode.
4:0	RO	0x0	reserved

GMAC_AN_EXP
Address: Operational Base + offset (0x00d0)
Auto Negotiation Expansion Register

Bit	Attr	Reset Value	Description
31:3	RO	0x0	reserved
2	RO	0x0	NPA Next Page Ability This bit is tied to low, because the GMAC does not support next page function.
1	RO	0x0	NPR New Page Received When set, this bit indicates that a new page has been received by the GMAC. This bit will be cleared when read.
0	RO	0x0	reserved

GMAC_INTF_MODE_STA
Address: Operational Base + offset (0x00d8)

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RGMII Status Register

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3	RO	0x0	LST Link Status Indicates whether the link is up (1'b1) or down (1'b0)
2:1	RO	0x0	LSD Link Speed Indicates the current speed of the link: 2'b00: 2.5 MHz 2'b01: 25 MHz 2'b10: 125 MHz
0	RW	0x0	LM Link Mode Indicates the current mode of operation of the link: 1'b0: Half-Duplex mode 1'b1: Full-Duplex mode

GMAC_MMC_CTRL

Address: Operational Base + offset (0x0100)

MMC Control Register

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5	RW	0x0	FHP Full-Half preset When low and bit4 is set, all MMC counters get preset to almost-half value. All octet counters get preset to 0x7FFF_F800 (half - 2K Bytes) and all frame-counters gets preset to 0x7FFF_FFF0 (half - 16) When high and bit4 is set, all MMC counters get preset to almost-full value. All octet counters get preset to 0xFFFF_F800 (full - 2K Bytes) and all frame-counters gets preset to 0xFFFF_FFF0 (full - 16)
4	R/W SC	0x0	CP Counters Preset When set, all counters will be initialized or preset to almost full or almost half as per Bit5 above. This bit will be cleared automatically after 1 clock cycle. This bit along with bit5 is useful for debugging and testing the assertion of interrupts due to MMC counter becoming half-full or full.

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Bit	Attr	Reset Value	Description
3	RW	0x0	MCF MMC Counter Freeze When set, this bit freezes all the MMC counters to their current value. (None of the MMC counters are updated due to any transmitted or received frame until this bit is reset to 0. If any MMC counter is read with the Reset on Read bit set, then that counter is also cleared in this mode.)
2	RW	0x0	ROR Reset on Read When set, the MMC counters will be reset to zero after Read (self-clearing after reset). The counters are cleared when the least significant byte lane (bits[7:0]) is read.
1	RW	0x0	CSR Counter Stop Rollover When set, counter after reaching maximum value will not roll over to zero
0	R/WSC	0x0	CR Counters Reset When set, all counters will be reset. This bit will be cleared automatically after 1 clock cycle

GMAC_MMC_RX_INTR
Address: Operational Base + offset (0x0104)
MMC Receive Interrupt Register

Bit	Attr	Reset Value	Description
31:22	RO	0x0	reserved
21	RW	0x0	INT21 The bit is set when the rxfifooverflow counter reaches half the maximum value, and also when it reaches the maximum value.
20:19	RO	0x0	reserved
18	RC	0x0	INT18 The bit is set when the rxlengtherror counter reaches half the maximum value, and also when it reaches the maximum value.
17:6	RO	0x0	reserved
5	RW	0x0	INT5 The bit is set when the rxcrcerror counter reaches half the maximum value, and also when it reaches the maximum value.
4	RC	0x0	INT4 The bit is set when the rxmulticastframes_g counter reaches half the maximum value, and also when it reaches the maximum value.
3	RO	0x0	reserved
2	RC	0x0	INT2 The bit is set when the rxoctetcount_g counter reaches half the maximum value, and also when it reaches the maximum value.

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Bit	Attr	Reset Value	Description
1	RC	0x0	INT1 The bit is set when the rxoctetcount_gb counter reaches half the maximum value, and also when it reaches the maximum value.
0	RC	0x0	INT0 The bit is set when the rxframecount_gb counter reaches half the maximum value, and also when it reaches the maximum value.

GMAC_MMC_TX_INTR
Address: Operational Base + offset (0x0108)
MMC Transmit Interrupt Register

Bit	Attr	Reset Value	Description
31:22	RO	0x0	reserved
21	RC	0x0	INT21 The bit is set when the txframecount_g counter reaches half the maximum value, and also when it reaches the maximum value.
20	RC	0x0	INT20 The bit is set when the txoctetcount_g counter reaches half the maximum value, and also when it reaches the maximum value.
19	RC	0x0	INT19 The bit is set when the txcarriererror counter reaches half the maximum value, and also when it reaches the maximum value.
18:14	RO	0x0	reserved
13	RC	0x0	INT13 The bit is set when the txunderflowerror counter reaches half the maximum value, and also when it reaches the maximum value.
12:2	RO	0x0	reserved
1	RC	0x0	INT1 The bit is set when the txframecount_gb counter reaches half the maximum value, and also when it reaches the maximum value.
0	RC	0x0	INT0 The bit is set when the txoctetcount_gb counter reaches half the maximum value, and also when it reaches the maximum value.

GMAC_MMC_RX_INT_MSK
Address: Operational Base + offset (0x010c)
MMC Receive Interrupt Mask Register

Bit	Attr	Reset Value	Description
31:22	RO	0x0	reserved
21	RW	0x0	INT21 Setting this bit masks the interrupt when the rxfifooverflow counter reaches half the maximum value, and also when it reaches the maximum value.
20:19	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
18	RW	0x0	INT18 Setting this bit masks the interrupt when the rxlengtherror counter reaches half the maximum value, and also when it reaches the maximum value.
17:6	RO	0x0	reserved
5	RW	0x0	INT5 Setting this bit masks the interrupt when the rxcrcerror counter reaches half the maximum value, and also when it reaches the maximum value.
4	RW	0x0	INT4 Setting this bit masks the interrupt when the rxmulticastframes_g counter reaches half the maximum value, and also when it reaches the maximum value.
3	RO	0x0	reserved
2	RW	0x0	INT2 Setting this bit masks the interrupt when the rxoctetcount_g counter reaches half the maximum value, and also when it reaches the maximum value.
1	RW	0x0	INT1 Setting this bit masks the interrupt when the rxoctetcount_gb counter reaches half the maximum value, and also when it reaches the maximum value.
0	RW	0x0	INT0 Setting this bit masks the interrupt when the rxframecount_gb counter reaches half the maximum value, and also when it reaches the maximum value.

GMAC_MMC_TX_INT_MSK
Address: Operational Base + offset (0x0110)
MMC Transmit Interrupt Mask Register

Bit	Attr	Reset Value	Description
31:22	RO	0x0	reserved
21	RW	0x0	INT21 Setting this bit masks the interrupt when the txframecount_g counter reaches half the maximum value, and also when it reaches the maximum value.
20	RW	0x0	INT20 Setting this bit masks the interrupt when the txoctetcount_g counter reaches half the maximum value, and also when it reaches the maximum value.
19	RW	0x0	INT19 Setting this bit masks the interrupt when the txcarriererror counter reaches half the maximum value, and also when it reaches the maximum value.
18:14	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
13	RW	0x0	INT13 Setting this bit masks the interrupt when the txunderflowerror counter reaches half the maximum value, and also when it reaches the maximum value.
12:2	RO	0x0	reserved
1	RW	0x0	INT1 Setting this bit masks the interrupt when the txframecount_gb counter reaches half the maximum value, and also when it reaches the maximum value.
0	RW	0x0	INT0 Setting this bit masks the interrupt when the txoctetcount_gb counter reaches half the maximum value, and also when it reaches the maximum value.

GMAC_MMC_TXOCTETCNT_GB
Address: Operational Base + offset (0x0114)
MMC TX OCTET Good and Bad Counter

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	txoctetcount_gb Number of bytes transmitted, exclusive of preamble and retried bytes, in good and bad frames.

GMAC_MMC_TXFRMCNT_GB
Address: Operational Base + offset (0x0118)
MMC TX Frame Good and Bad Counter

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	txframecount_gb Number of good and bad frames transmitted, exclusive of retried frames.

GMAC_MMC_TXUNDFLWERR
Address: Operational Base + offset (0x0148)
MMC TX Underflow Error

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	txunderflowerror Number of frames aborted due to frame underflow error.

GMAC_MMC_TXCARERR
Address: Operational Base + offset (0x0160)
MMC TX Carrier Error

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	txcarriererror Number of frames aborted due to carrier sense error (no carrier or loss of carrier).

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GMAC_MMC_TXOCTETCNT_G
Address: Operational Base + offset (0x0164)
MMC TX OCTET Good Counter

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	txoctetcount_g Number of bytes transmitted, exclusive of preamble, in good frames only.

GMAC_MMC_TXFRMCNT_G
Address: Operational Base + offset (0x0168)
MMC TX Frame Good Counter

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	txframecount_g Number of good frames transmitted.

GMAC_MMC_RXFRMCNT_GB
Address: Operational Base + offset (0x0180)
MMC RX Frame Good and Bad Counter

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rxframecount_gb Number of good and bad frames received.

GMAC_MMC_RXOCTETCNT_GB
Address: Operational Base + offset (0x0184)
MMC RX OCTET Good and Bad Counter

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rxoctetcount_gb Number of bytes received, exclusive of preamble, in good and bad frames.

GMAC_MMC_RXOCTETCNT_G
Address: Operational Base + offset (0x0188)
MMC RX OCTET Good Counter

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rxoctetcount_g Number of bytes received, exclusive of preamble, only in good frames.

GMAC_MMC_RXMCFRMCNT_G
Address: Operational Base + offset (0x0190)
MMC RX Mulitcast Frame Good Counter

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rxmulticastframes_g Number of good multicast frames received.

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GMAC_MMC_RXCRCERR
Address: Operational Base + offset (0x0194)
MMC RX Carrier

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rxcrcerror Number of frames received with CRC error.

GMAC_MMC_RXLENERR
Address: Operational Base + offset (0x01c8)
MMC RX Length Error

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rxlengtherror Number of frames received with length error (Length type field ≠frame size), for all frames with valid length field.

GMAC_MMC_RXFIFOOVRFLW
Address: Operational Base + offset (0x01d4)
MMC RX FIFO Overflow

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rxfifooverflow Number of missed received frames due to FIFO overflow.

GMAC_MMC_IPC_INT_MSK
Address: Operational Base + offset (0x0200)
MMC Receive Checksum Offload Interrupt Mask Register

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29	RW	0x0	INT29 Setting this bit masks the interrupt when the rxicmp_err_octets counter reaches half the maximum value, and also when it reaches the maximum value.
28	RO	0x0	reserved
27	RW	0x0	INT27 Setting this bit masks the interrupt when the rxtcp_err_octets counter reaches half the maximum value, and also when it reaches the maximum value.
26	RO	0x0	reserved
25	RW	0x0	INT25 Setting this bit masks the interrupt when the rxudp_err_octets counter reaches half the maximum value, and also when it reaches the maximum value.
24:23	RO	0x0	reserved
22	RW	0x0	INT22 Setting this bit masks the interrupt when the rxipv6_hdrerr_octets counter reaches half the maximum value, and also when it reaches the maximum value.

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Bit	Attr	Reset Value	Description
21:18	RO	0x0	reserved
17	RW	0x0	INT17 Setting this bit masks the interrupt when the rxipv4_hdrerr_octets counter reaches half the maximum value, and also when it reaches the maximum value.
16:14	RO	0x0	reserved
13	RW	0x0	INT13 Setting this bit masks the interrupt when the rxicmp_err_frms counter reaches half the maximum value, and also when it reaches the maximum value.
12	RO	0x0	reserved
11	RW	0x0	INT11 Setting this bit masks the interrupt when the rxtcp_err_frms counter reaches half the maximum value, and also when it reaches the maximum value.
10	RO	0x0	reserved
9	RW	0x0	INT9 Setting this bit masks the interrupt when the rxudp_err_frms counter reaches half the maximum value, and also when it reaches the maximum value.
8:7	RO	0x0	reserved
6	RW	0x0	INT6 Setting this bit masks the interrupt when the rxipv6_hdrerr_frms counter reaches half the maximum value, and also when it reaches the maximum value.
5	RW	0x0	INT5 Setting this bit masks the interrupt when the rxipv6_gd_frms counter reaches half the maximum value, and also when it reaches the maximum value.
4:2	RO	0x0	reserved
1	RW	0x0	INT1 Setting this bit masks the interrupt when the rxipv4_hdrerr_frms counter reaches half the maximum value, and also when it reaches the maximum value.
0	RW	0x0	INT0 Setting this bit masks the interrupt when the rxipv4_gd_frms counter reaches half the maximum value, and also when it reaches the maximum value.

GMAC_MMC_IPC_INTR
Address: Operational Base + offset (0x0208)
MMC Receive Checksum Offload Interrupt Register

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
29	RC	0x0	INT29 The bit is set when the rxicmp_err_octets counter reaches half the maximum value, and also when it reaches the maximum value.
28	RO	0x0	reserved
27	RC	0x0	INT27 The bit is set when the rxtcp_err_octets counter reaches half the maximum value, and also when it reaches the maximum value.
26	RO	0x0	reserved
25	RC	0x0	INT25 The bit is set when the rxudp_err_octets counter reaches half the maximum value, and also when it reaches the maximum value.
24:23	RO	0x0	reserved
22	RC	0x0	INT22 The bit is set when the rxipv6_hdrerr_octets counter reaches half the maximum value, and also when it reaches the maximum value.
21:18	RO	0x0	reserved
17	RC	0x0	INT17 The bit is set when the rxipv4_hdrerr_octets counter reaches half the maximum value, and also when it reaches the maximum value.
16:14	RO	0x0	reserved
13	RC	0x0	INT13 The bit is set when the rxicmp_err_frms counter reaches half the maximum value, and also when it reaches the maximum value.
12	RO	0x0	reserved
11	RC	0x0	INT11 The bit is set when the rxtcp_err_frms counter reaches half the maximum value, and also when it reaches the maximum value.
10	RO	0x0	reserved
9	RC	0x0	INT9 The bit is set when the rxudp_err_frms counter reaches half the maximum value, and also when it reaches the maximum value.
8:7	RO	0x0	reserved
6	RC	0x0	INT6 The bit is set when the rxipv6_hdrerr_frms counter reaches half the maximum value, and also when it reaches the maximum value.
5	RC	0x0	INT5 The bit is set when the rxipv6_gd_frms counter reaches half the maximum value, and also when it reaches the maximum value.
4:2	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
1	RC	0x0	INT1 The bit is set when the rxipv4_hdrerr_frms counter reaches half the maximum value, and also when it reaches the maximum value.
0	RC	0x0	INT0 The bit is set when the rxipv4_gd_frms counter reaches half the maximum value, and also when it reaches the maximum value.

GMAC_MMC_RXIPV4GFRM
Address: Operational Base + offset (0x0210)
MMC RX IPV4 Good Frame

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rxipv4_gd_frms Number of good IPv4 datagrams received with the TCP, UDP, or ICMP payload

GMAC_MMC_RXIPV4HDERRFRM
Address: Operational Base + offset (0x0214)
MMC RX IPV4 Head Error Frame

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rxipv4_hdrerr_frms Number of IPv4 datagrams received with header (checksum, length, or version mismatch) errors

GMAC_MMC_RXIPV6GFRM
Address: Operational Base + offset (0x0224)
MMC RX IPV6 Good Frame

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rxipv6_gd_frms Number of good IPv6 datagrams received with TCP, UDP, or ICMP payloads.

GMAC_MMC_RXIPV6HDERRFRM
Address: Operational Base + offset (0x0228)
MMC RX IPV6 Head Error Frame

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rxipv6_hdrerr_frms Number of IPv6 datagrams received with header errors (length or version mismatch).

GMAC_MMC_RXUDPERRFRM
Address: Operational Base + offset (0x0234)
MMC RX UDP Error Frame

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rxudp_err_frms Number of good IP datagrams whose UDP payload has a checksum error.

GMAC_MMC_RXTCPERRFRM
Address: Operational Base + offset (0x023c)
MMC RX TCP Error Frame

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rxtcp_err_frms Number of good IP datagrams whose TCP payload has a checksum error.

GMAC_MMC_RXICMPERRFRM
Address: Operational Base + offset (0x0244)
MMC RX ICMP Error Frame

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rxicmp_err_frms Number of good IP datagrams whose ICMP payload has a checksum error.

GMAC_MMC_RXIPV4HDERROCT
Address: Operational Base + offset (0x0254)
MMC RX OCTET IPV4 Head Error

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rxipv4_hdrerr_octets Number of bytes received in IPv4 datagrams with header errors (checksum, length, version mismatch). The value in the Length field of IPv4 header is used to update this counter.

GMAC_MMC_RXIPV6HDERROCT
Address: Operational Base + offset (0x0268)
MMC RX OCTET IPV6 Head Error

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rxipv6_hdrerr_octets Number of bytes received in IPv6 datagrams with header errors (length, version mismatch). The value in the IPv6 header's Length field is used to update this counter.

GMAC_MMC_RXUDPERROCT
Address: Operational Base + offset (0x0274)
MMC RX OCTET UDP Error

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rxudp_err_octets Number of bytes received in a UDP segment that had checksum errors.

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GMAC_MMC_RXTCPERROCT
Address: Operational Base + offset (0x027c)
MMC RX OCTET TCP Error

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rxtcp_err_octets Number of bytes received in a TCP segment with checksum errors.

GMAC_MMC_RXICMPERROCT
Address: Operational Base + offset (0x0284)
MMC RX OCTET ICMP Error

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rxicmp_err_octets Number of bytes received in an ICMP segment with checksum errors.

GMAC_BUS_MODE
Address: Operational Base + offset (0x1000)
Bus Mode Register

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25	RW	0x0	AAL Address-Aligned Beats When this bit is set high and the FB bit equals 1, the AXI interface generates all bursts aligned to the start address LS bits. If the FB bit equals 0, the first burst (accessing the data buffer's start address) is not aligned, but subsequent bursts are aligned to the address.
24	RW	0x0	PBL_Mode 8xPBL Mode When set high, this bit multiplies the PBL value programmed (bits [22:17] and bits [13:8]) eight times. Thus the DMA will transfer data in to a maximum of 8, 16, 32, 64, 128, and 256 beats depending on the PBL value.
23	RW	0x0	USP Use Separate PBL When set high, it configures the RxDMA to use the value configured in bits [22:17] as PBL while the PBL value in bits [13:8] is applicable to TxDMA operations only. When reset to low, the PBL value in bits [13:8] is applicable for both DMA engines.

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Bit	Attr	Reset Value	Description
22:17	RW	0x01	RPBL RxDMA PBL These bits indicate the maximum number of beats to be transferred in one RxDMA transaction. This will be the maximum value that is used in a single block Read/Write. The RxDMA will always attempt to burst as specified in RPBL each time it starts a Burst transfer on the host bus. RPBL can be programmed with permissible values of 1, 2, 4, 8, 16, and 32. Any other value will result in undefined behavior. These bits are valid and applicable only when USP is set high.
16	RW	0x0	FB Fixed Burst This bit controls whether the AXI Master interface performs fixed burst transfers or not. When set, the AHB will use only SINGLE, INCR4, INCR8 or INCR16 during start of normal burst transfers. When reset, the AXI will use SINGLE and INCR burst transfer operations.
15:14	RO	0x0	reserved
13:8	RW	0x01	PBL Programmable Burst Length These bits indicate the maximum number of beats to be transferred in one DMA transaction. This will be the maximum value that is used in a single block Read/Write. The DMA will always attempt to burst as specified in PBL each time it starts a Burst transfer on the host bus. PBL can be programmed with permissible values of 1, 2, 4, 8, 16, and 32. Any other value will result in undefined behavior. When USP is set high, this PBL value is applicable for TxDMA transactions only. The PBL values have the following limitations. The maximum number of beats (PBL) possible is limited by the size of the Tx FIFO and Rx FIFO in the MTL layer and the data bus width on the DMA. The FIFO has a constraint that the maximum beat supported is half the depth of the FIFO, except when specified (as given below). For different data bus widths and FIFO sizes, the valid PBL range (including x8 mode) is provided in the following table. If the PBL is common for both transmit and receive DMA, the minimum Rx FIFO and Tx FIFO depths must be considered. Do not program out-of-range PBL values, because the system may not behave properly. For TxFIFO, valid PBL range in full duplex mode and duplex mode is 128 or less. For RxFIFO, valid PBL range in full duplex mode is all.
7	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
6:2	RW	0x00	DSL Descriptor Skip Length This bit specifies the number of dword to skip between two unchained descriptors. The address skipping starts from the end of current descriptor to the start of next descriptor. When DSL value equals zero, then the descriptor table is taken as contiguous by the DMA, in Ring mode.
1	RO	0x0	reserved
0	R/WSC	0x1	SWR Software Reset When this bit is set, the MAC DMA Controller resets all GMAC Subsystem internal registers and logic. It is cleared automatically after the reset operation has completed in all of the core clock domains. Read a 0 value in this bit before re-programming any register of the core. Note: The reset operation is completed only when all the resets in all the active clock domains are de-asserted. Hence it is essential that all the PHY inputs clocks (applicable for the selected PHY interface) are present for software reset completion.

GMAC_TX_POLL_DEMAND
Address: Operational Base + offset (0x1004)
Transmit Poll Demand Register

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	TPD Transmit Poll Demand When these bits are written with any value, the DMA reads the current descriptor pointed to by Register GMAC_CUR_HOST_TX_DESC. If that descriptor is not available (owned by Host), transmission returns to the Suspend state and DMA Register GMAC_STATUS[2] is asserted. If the descriptor is available, transmission resumes.

GMAC_RX_POLL_DEMAND
Address: Operational Base + offset (0x1008)
Receive Poll Demand Register

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RPD Receive Poll Demand When these bits are written with any value, the DMA reads the current descriptor pointed to by Register GMAC_CUR_HOST_RX_DESC. If that descriptor is not available (owned by Host), reception returns to the Suspended state and Register GMAC_STATUS[7] is not asserted. If the descriptor is available, the Receive DMA returns to active state.

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GMAC_RX_DESC_LIST_ADDR
Address: Operational Base + offset (0x100c)
Receive Descriptor List Address Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	SRL Start of Receive List This field contains the base address of the First Descriptor in the Receive Descriptor list. The LSB bits [1/2/3:0] for 32/64/128-bit bus width) will be ignored and taken as all-zero by the DMA internally. Hence these LSB bits are Read Only.

GMAC_TX_DESC_LIST_ADDR
Address: Operational Base + offset (0x1010)
Transmit Descriptor List Address Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	STL Start of Transmit List This field contains the base address of the First Descriptor in the Transmit Descriptor list. The LSB bits [1/2/3:0] for 32/64/128-bit bus width) will be ignored and taken as all-zero by the DMA internally. Hence these LSB bits are Read Only.

GMAC_STATUS
Address: Operational Base + offset (0x1014)
Status Register

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28	RO	0x0	GPI GMAC PMT Interrupt This bit indicates an interrupt event in the GMAC core's PMT module. The software must read the corresponding registers in the GMAC core to get the exact cause of interrupt and clear its source to reset this bit to 1'b0. The interrupt signal from the GMAC subsystem (sbd_intr_o) is high when this bit is high.
27	RO	0x0	GMI GMAC MMC Interrupt This bit reflects an interrupt event in the MMC module of the GMAC core. The software must read the corresponding registers in the GMAC core to get the exact cause of interrupt and clear the source of interrupt to make this bit as 1'b0. The interrupt signal from the GMAC subsystem (sbd_intr_o) is high when this bit is high.

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Bit	Attr	Reset Value	Description
26	RO	0x0	GLI GMAC Line interface Interrupt This bit reflects an interrupt event in the GMAC Core's PCS or RGMII interface block. The software must read the corresponding registers in the GMAC core to get the exact cause of interrupt and clear the source of interrupt to make this bit as 1'b0. The interrupt signal from the GMAC subsystem (sbd_intr_o) is high when this bit is high.
25:23	RO	0x0	EB Error Bits These bits indicate the type of error that caused a Bus Error (e.g., error response on the AXI interface). Valid only with Fatal Bus Error bit (Register GMAC_STATUS[13]) set. This field does not generate an interrupt. Bit 23: 1'b1 Error during data transfer by TxDMA 1'b0 Error during data transfer by RxDMA Bit 24: 1'b1 Error during read transfer 1'b0 Error during write transfer Bit 25: 1'b1 Error during descriptor access 1'b0 Error during data buffer access
22:20	RO	0x0	TS Transmit Process State These bits indicate the Transmit DMA FSM state. This field does not generate an interrupt. 3'b000: Stopped; Reset or Stop Transmit Command issued. 3'b001: Running; Fetching Transmit Transfer Descriptor. 3'b010: Running; Waiting for status. 3'b011: Running; Reading Data from host memory buffer and queuing it to transmit buffer (Tx FIFO). 3'b100: TIME_STAMP write state. 3'b101: Reserved for future use. 3'b110: Suspended; Transmit Descriptor Unavailable or Transmit Buffer Underflow. 3'b111: Running; Closing Transmit Descriptor.

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Bit	Attr	Reset Value	Description
19:17	RO	0x0	RS Receive Process State These bits indicate the Receive DMA FSM state. This field does not generate an interrupt. 3'b000: Stopped: Reset or Stop Receive Command issued. 3'b001: Running: Fetching Receive Transfer Descriptor. 3'b010: Reserved for future use. 3'b011: Running: Waiting for receive packet. 3'b100: Suspended: Receive Descriptor Unavailable. 3'b101: Running: Closing Receive Descriptor. 3'b110: TIME_STAMP write state. 3'b111: Running: Transferring the receive packet data from receive buffer to host memory.
16	W1C	0x0	NIS Normal Interrupt Summary Normal Interrupt Summary bit value is the logical OR of the following when the corresponding interrupt bits are enabled in Register OP_MODE: Register GMAC_STATUS[0]: Transmit Interrupt Register GMAC_STATUS[2]: Transmit Buffer Unavailable Register GMAC_STATUS[6]: Receive Interrupt Register GMAC_STATUS[14]: Early Receive Interrupt Only unmasked bits affect the Normal Interrupt Summary bit. This is a sticky bit and must be cleared (by writing a 1 to this bit) each time a corresponding bit that causes NIS to be set is cleared.
15	W1C	0x0	AIS Abnormal Interrupt Summary Abnormal Interrupt Summary bit value is the logical OR of the following when the corresponding interrupt bits are enabled in Register OP_MODE: Register GMAC_STATUS[1]: Transmit Process Stopped Register GMAC_STATUS[3]: Transmit Jabber Timeout Register GMAC_STATUS[4]: Receive FIFO Overflow Register GMAC_STATUS[5]: Transmit Underflow Register GMAC_STATUS[7]: Receive Buffer Unavailable Register GMAC_STATUS[8]: Receive Process Stopped Register GMAC_STATUS[9]: Receive Watchdog Timeout Register GMAC_STATUS[10]: Early Transmit Interrupt Register GMAC_STATUS[13]: Fatal Bus Error Only unmasked bits affect the Abnormal Interrupt Summary bit. This is a sticky bit and must be cleared each time a corresponding bit that causes AIS to be set is cleared.

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Bit	Attr	Reset Value	Description
14	W1C	0x0	ERI Early Receive Interrupt This bit indicates that the DMA had filled the first data buffer of the packet. Receive Interrupt Register GMAC_STATUS[6] automatically clears this bit.
13	W1C	0x0	FBI Fatal Bus Error Interrupt This bit indicates that a bus error occurred, as detailed in [25:23]. When this bit is set, the corresponding DMA engine disables all its bus accesses.
12:11	RO	0x0	reserved
10	W1C	0x0	ETI Early Transmit Interrupt This bit indicates that the frame to be transmitted was fully transferred to the MTL Transmit FIFO.
9	W1C	0x0	RWT Receive Watchdog Timeout This bit is asserted when a frame with a length greater than 2,048 bytes is received.
8	W1C	0x0	RPS Receive Process Stopped This bit is asserted when the Receive Process enters the Stopped state.
7	W1C	0x0	RU Receive Buffer Unavailable This bit indicates that the Next Descriptor in the Receive List is owned by the host and cannot be acquired by the DMA. Receive Process is suspended. To resume processing Receive descriptors, the host should change the ownership of the descriptor and issue a Receive Poll Demand command. If no Receive Poll Demand is issued, Receive Process resumes when the next recognized incoming frame is received. Register GMAC_STATUS[7] is set only when the previous Receive Descriptor was owned by the DMA.
6	W1C	0x0	RI Receive Interrupt This bit indicates the completion of frame reception. Specific frame status information has been posted in the descriptor. Reception remains in the Running state.
5	W1C	0x0	UNF Transmit Underflow This bit indicates that the Transmit Buffer had an Underflow during frame transmission. Transmission is suspended and an Underflow Error TDES0[1] is set.

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Bit	Attr	Reset Value	Description
4	W1C	0x0	OVF Receive Overflow This bit indicates that the Receive Buffer had an Overflow during frame reception. If the partial frame is transferred to application, the overflow status is set in RDES0[11].
3	W1C	0x0	TJT Transmit Jabber Timeout This bit indicates that the Transmit Jabber Timer expired, meaning that the transmitter had been excessively active. The transmission process is aborted and placed in the Stopped state. This causes the Transmit Jabber Timeout TDES0[14] flag to assert.
2	W1C	0x0	TU Transmit Buffer Unavailable This bit indicates that the Next Descriptor in the Transmit List is owned by the host and cannot be acquired by the DMA. Transmission is suspended. Bits[22:20] explain the Transmit Process state transitions. To resume processing transmit descriptors, the host should change the ownership of the bit of the descriptor and then issue a Transmit Poll Demand command.
1	W1C	0x0	TPS Transmit Process Stopped This bit is set when the transmission is stopped.
0	W1C	0x0	TI Transmit Interrupt This bit indicates that frame transmission is finished and TDES1[31] is set in the First Descriptor.

GMAC_OP_MODE
Address: Operational Base + offset (0x1018)
Operation Mode Register

Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved
26	RW	0x0	DT Disable Dropping of TCP/IP Checksum Error Frames When this bit is set, the core does not drop frames that only have errors detected by the Receive Checksum Offload engine. Such frames do not have any errors (including FCS error) in the Ethernet frame received by the MAC but have errors in the encapsulated payload only. When this bit is reset, all error frames are dropped if the FEF bit is reset.

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Bit	Attr	Reset Value	Description
25	RW	0x0	RSF Receive Store and Forward When this bit is set, the MTL only reads a frame from the Rx FIFO after the complete frame has been written to it, ignoring RTC bits. When this bit is reset, the Rx FIFO operates in Cut-Through mode, subject to the threshold specified by the RTC bits.
24	RW	0x0	DFF Disable Flushing of Received Frames When this bit is set, the RxDMA does not flush any frames due to the unavailability of receive descriptors/buffers as it does normally when this bit is reset.
23:22	RO	0x0	reserved
21	RW	0x0	TSF Transmit Store and Forward When this bit is set, transmission starts when a full frame resides in the MTL Transmit FIFO. When this bit is set, the TTC values specified in Register GMAC_OP_MODE[16:14] are ignored. This bit should be changed only when transmission is stopped.
20	W1C	0x0	FTF Flush Transmit FIFO When this bit is set, the transmit FIFO controller logic is reset to its default values and thus all data in the Tx FIFO is lost/flushed. This bit is cleared internally when the flushing operation is completed fully. The Operation Mode register should not be written to until this bit is cleared. The data which is already accepted by the MAC transmitter will not be flushed. It will be scheduled for transmission and will result in underflow and runt frame transmission. Note: The flush operation completes only after emptying the TxFIFO of its contents and all the pending Transmit Status of the transmitted frames are accepted by the host. In order to complete this flush operation, the PHY transmit clock (clk_tx_i) is required to be active.
19:17	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
16:14	RW	0x0	TTC Transmit Threshold Control These three bits control the threshold level of the MTL Transmit FIFO. Transmission starts when the frame size within the MTL Transmit FIFO is larger than the threshold. In addition, full frames with a length less than the threshold are also transmitted. These bits are used only when the TSF bit (Bit 21) is reset. 3'b000: 64 3'b001: 128 3'b010: 192 3'b011: 256 3'b100: 40 3'b101: 32 3'b110: 24 3'b111: 16
13	RW	0x0	ST Start/Stop Transmission Command When this bit is set, transmission is placed in the Running state, and the DMA checks the Transmit List at the current position for a frame to be transmitted. Descriptor acquisition is attempted either from the current position in the list, which is the Transmit List Base Address set by Register GMAC_TX_DESC_LIST_ADDR, or from the position retained when transmission was stopped previously. If the current descriptor is not owned by the DMA, transmission enters the Suspended state and Transmit Buffer Unavailable (Register GMAC_STATUS[2]) is set. The Start Transmission command is effective only when transmission is stopped. If the command is issued before setting DMA Register TX_DESC_LIST_ADDR, then the DMA behavior is unpredictable. When this bit is reset, the transmission process is placed in the Stopped state after completing the transmission of the current frame. The Next Descriptor position in the Transmit List is saved, and becomes the current position when transmission is restarted. The stop transmission command is effective only the transmission of the current frame is complete or when the transmission is in the Suspended state.
12:11	RW	0x0	RFD Threshold for deactivating flow control (in both HD and FD) These bits control the threshold (Fill-level of Rx FIFO) at which the flow-control is de-asserted after activation. 2'b00: Full minus 1 KB 2'b01: Full minus 2 KB 2'b10: Full minus 3 KB 2'b11: Full minus 4 KB Note that the de-assertion is effective only after flow control is asserted.

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Bit	Attr	Reset Value	Description
10:9	RW	0x0	RFA Threshold for activating flow control (in both HD and FD) These bits control the threshold (Fill level of Rx FIFO) at which flow control is activated. 2'b00: Full minus 1 KB 2'b01: Full minus 2 KB 2'b10: Full minus 3 KB 2'b11: Full minus 4 KB Note that the above only applies to Rx FIFOs of 4 KB or more when the EFC bit is set high.
8	RW	0x0	EFC Enable HW flow control When this bit is set, the flow control signal operation based on fill-level of Rx FIFO is enabled. When reset, the flow control operation is disabled.
7	RW	0x0	FEF Forward Error Frames When this bit is reset, the Rx FIFO drops frames with error status (CRC error, collision error, GMII_ER, giant frame, watchdog timeout, overflow). However, if the frame's start byte (write) pointer is already transferred to the read controller side (in Threshold mode), then the frames are not dropped. When FEF is set, all frames except runt error frames are forwarded to the DMA. But when RxFIFO overflows when a partial frame is written, then such frames are dropped even when FEF is set.
6	RW	0x0	FUF Forward Undersized Good Frames When set, the Rx FIFO will forward Undersized frames (frames with no Error and length less than 64 bytes) including pad-bytes and CRC). When reset, the Rx FIFO will drop all frames of less than 64 bytes, unless it is already transferred due to lower value of Receive Threshold (e.g., RTC = 01).
5	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
4:3	RW	0x0	RTC Receive Threshold Control These two bits control the threshold level of the MTL Receive FIFO. Transfer (request) to DMA starts when the frame size within the MTL Receive FIFO is larger than the threshold. In addition, full frames with a length less than the threshold are transferred automatically. Note that value of 11 is not applicable if the configured Receive FIFO size is 128 bytes. These bits are valid only when the RSF bit is zero, and are ignored when the RSF bit is set to 1. 2'b00: 64 2'b01: 32 2'b10: 96 2'b11: 128
2	RW	0x0	OSF Operate on Second Frame When this bit is set, this bit instructs the DMA to process a second frame of Transmit data even before status for first frame is obtained.
1	RW	0x0	SR Start/Stop Receive When this bit is set, the Receive process is placed in the Running state. The DMA attempts to acquire the descriptor from the Receive list and processes incoming frames. Descriptor acquisition is attempted from the current position in the list, which is the address set by register GMAC_RX_DESC_LIST_ADDR or the position retained when the Receive process was previously stopped. If no descriptor is owned by the DMA, reception is suspended and Receive Buffer Unavailable (Register GMAC_STATUS[7]) is set. The Start Receive command is effective only when reception has stopped. If the command was issued before setting register GMAC_RX_DESC_LIST_ADDR, DMA behavior is unpredictable. When this bit is cleared, RxDMA operation is stopped after the transfer of the current frame. The next descriptor position in the Receive list is saved and becomes the current position after the Receive process is restarted. The Stop Receive command is effective only when the Receive process is in either the Running (waiting for receive packet) or in the Suspended state.
0	RO	0x0	reserved

GMAC_INT_ENA
Address: Operational Base + offset (0x101c)
Interrupt Enable Register

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Bit	Attr	Reset Value	Description
31:17	RO	0x0	reserved
16	RW	0x0	NIE Normal Interrupt Summary Enable When this bit is set, a normal interrupt is enabled. When this bit is reset, a normal interrupt is disabled. This bit enables the following bits: Register GMAC_STATUS[0]: Transmit Interrupt Register GMAC_STATUS[2]: Transmit Buffer Unavailable Register GMAC_STATUS[6]: Receive Interrupt Register GMAC_STATUS[14]: Early Receive Interrupt
15	RW	0x0	AIE Abnormal Interrupt Summary Enable When this bit is set, an Abnormal Interrupt is enabled. When this bit is reset, an Abnormal Interrupt is disabled. This bit enables the following bits Register GMAC_STATUS[1]: Transmit Process Stopped Register GMAC_STATUS[3]: Transmit Jabber Timeout Register GMAC_STATUS[4]: Receive Overflow Register GMAC_STATUS[5]: Transmit Underflow Register GMAC_STATUS[7]: Receive Buffer Unavailable Register GMAC_STATUS[8]: Receive Process Stopped Register GMAC_STATUS[9]: Receive Watchdog Timeout Register GMAC_STATUS[10]: Early Transmit Interrupt Register GMAC_STATUS[13]: Fatal Bus Error
14	RW	0x0	ERE Early Receive Interrupt Enable When this bit is set with Normal Interrupt Summary Enable (BIT 16), Early Receive Interrupt is enabled. When this bit is reset, Early Receive Interrupt is disabled.
13	RW	0x0	FBE Fatal Bus Error Enable When this bit is set with Abnormal Interrupt Summary Enable (BIT 15), the Fatal Bus Error Interrupt is enabled. When this bit is reset, Fatal Bus Error Enable Interrupt is disabled.
12:11	RO	0x0	reserved
10	RW	0x0	ETE Early Transmit Interrupt Enable When this bit is set with an Abnormal Interrupt Summary Enable (BIT 15), Early Transmit Interrupt is enabled. When this bit is reset, Early Transmit Interrupt is disabled.

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Bit	Attr	Reset Value	Description
9	RW	0x0	RWE Receive Watchdog Timeout Enable When this bit is set with Abnormal Interrupt Summary Enable (BIT 15), the Receive Watchdog Timeout Interrupt is enabled. When this bit is reset, Receive Watchdog Timeout Interrupt is disabled.
8	RW	0x0	RSE Receive Stopped Enable When this bit is set with Abnormal Interrupt Summary Enable (BIT 15), Receive Stopped Interrupt is enabled. When this bit is reset, Receive Stopped Interrupt is disabled.
7	RW	0x0	RUE Receive Buffer Unavailable Enable When this bit is set with Abnormal Interrupt Summary Enable (BIT 15), Receive Buffer Unavailable Interrupt is enabled. When this bit is reset, the Receive Buffer Unavailable Interrupt is disabled
6	RW	0x0	RIE Receive Interrupt Enable When this bit is set with Normal Interrupt Summary Enable (BIT 16), Receive Interrupt is enabled. When this bit is reset, Receive Interrupt is disabled.
5	RW	0x0	UNE Underflow Interrupt Enable When this bit is set with Abnormal Interrupt Summary Enable (BIT 15), Transmit Underflow Interrupt is enabled. When this bit is reset, Underflow Interrupt is disabled.
4	RW	0x0	OVE Overflow Interrupt Enable When this bit is set with Abnormal Interrupt Summary Enable (BIT 15), Receive Overflow Interrupt is enabled. When this bit is reset, Overflow Interrupt is disabled
3	RW	0x0	TJE Transmit Jabber Timeout Enable When this bit is set with Abnormal Interrupt Summary Enable (BIT 15), Transmit Jabber Timeout Interrupt is enabled. When this bit is reset, Transmit Jabber Timeout Interrupt is disabled.
2	RW	0x0	TUE Transmit Buffer Unavailable Enable When this bit is set with Normal Interrupt Summary Enable (BIT 16), Transmit Buffer Unavailable Interrupt is enabled. When this bit is reset, Transmit Buffer Unavailable Interrupt is disabled.

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Bit	Attr	Reset Value	Description
1	RW	0x0	TSE Transmit Stopped Enable When this bit is set with Abnormal Interrupt Summary Enable (BIT 15), Transmission Stopped Interrupt is enabled. When this bit is reset, Transmission Stopped Interrupt is disabled.
0	RW	0x0	TIE Transmit Interrupt Enable When this bit is set with Normal Interrupt Summary Enable (BIT 16), Transmit Interrupt is enabled. When this bit is reset, Transmit Interrupt is disabled.

GMAC_OVERFLOW_CNT
Address: Operational Base + offset (0x1020)
Missed Frame and Buffer Overflow Counter Register

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28	RC	0x0	FIFO_overflow_bit Overflow bit for FIFO Overflow Counter
27:17	RC	0x000	Frame_miss_number Indicates the number of frames missed by the application This counter is incremented each time the MTL asserts the sideband signal mtl_rxoverflow_o. The counter is cleared when this register is read with mci_be_i[2] at 1'b1.
16	RC	0x0	Miss_frame_overflow_bit Overflow bit for Missed Frame Counter
15:0	RC	0x0000	Frame_miss_number_2 Indicates the number of frames missed by the controller due to the Host Receive Buffer being unavailable. This counter is incremented each time the DMA discards an incoming frame. The counter is cleared when this register is read with mci_be_i[0] at 1'b1.

GMAC_REC_INT_WDT_TIMER
Address: Operational Base + offset (0x1024)
Receive Interrupt Watchdog Timer Register

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	RIWT RI Watchdog Timer count Indicates the number of system clock cycles multiplied by 256 for which the watchdog timer is set. The watchdog timer gets triggered with the programmed value after the RxDMA completes the transfer of a frame for which the RI status bit is not set due to the setting in the corresponding descriptor RDES1[31]. When the watch-dog timer runs out, the RI bit is set and the timer is stopped. The watchdog timer is reset when RI bit is set high due to automatic setting of RI as per RDES1[31] of any received frame.

GMAC_AXI_BUS_MODE
Address: Operational Base + offset (0x1028)
AXI Bus Mode Register

Bit	Attr	Reset Value	Description
31	RW	0x0	EN_LPI Enable LPI (Low Power Interface) When set to 1, enable the LPI (Low Power Interface) supported by the GMAC and accepts the LPI request from the AXI System Clock controller. When set to 0, disables the Low Power Mode and always denies the LPI request from the AXI System Clock controller.
30	RW	0x0	UNLCK_ON_MGK_RWK Unlock on Magic Packet or Remote Wake Up When set to 1, enables it to request coming out of Low Power mode only when Magic Packet or Remote Wake Up Packet is received. When set to 0, enables it requests to come out of Low Power mode when any frame is received.
29:22	RO	0x0	reserved
21:20	RW	0x1	WR_OSR_LMT AXI Maximum Write Out Standing Request Limit This value limits the maximum outstanding request on the AXI write interface. Maximum outstanding requests = WR_OSR_LMT+1
19:18	RO	0x0	reserved
17:16	RW	0x1	RD_OSR_LMT AXI Maximum Read Out Standing Request Limit This value limits the maximum outstanding request on the AXI read interface. Maximum outstanding requests = RD_OSR_LMT+1
15:13	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
12	RO	0x0	AXI_AAL Address-Aligned Beats This bit is read-only bit and reflects the AAL bit (register GMAC_BUS_MODE[25]). When this bit set to 1, it performs address-aligned burst transfers on both read and write channels.
11:4	RO	0x0	reserved
3	RW	0x0	BLEN16 AXI Burst Length 16 When this bit is set to 1, or when UNDEF is set to 1, it is allowed to select a burst length of 16.
2	RW	0x0	BLEN8 AXI Burst Length 8 When this bit is set to 1, or when UNDEF is set to 1, it is allowed to select a burst length of 8.
1	RW	0x0	BLEN4 AXI Burst Length 4 When this bit is set to 1, or when UNDEF is set to 1, it is allowed to select a burst length of 4.
0	RO	0x1	UNDEF AXI Undefined Burst Length This bit is read-only bit and indicates the complement (invert) value of FB bit in register GMAC_BUS_MODE[16]. When this bit is set to 1, it is allowed to perform any burst length equal to or below the maximum allowed burst length as programmed in bits[7:1]; When this bit is set to 0, it is allowed to perform only fixed burst lengths as indicated by BLEN256/128/64/32/16/8/4, or a burst length of 1.

GMAC_AXI_STATUS
Address: Operational Base + offset (0x102c)
AXI Status Register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RO	0x0	RD_CH_STA When high, it indicates that AXI Master's read channel is active and transferring data.
0	RO	0x0	WR_CH_STA When high, it indicates that AXI Master's write channel is active and transferring data.

GMAC_CUR_HOST_TX_DESC
Address: Operational Base + offset (0x1048)
Current Host Transmit Descriptor Register

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	HTDAP Host Transmit Descriptor Address Pointer Cleared on Reset. Pointer updated by DMA during operation.

GMAC_CUR_HOST_RX_DESC
Address: Operational Base + offset (0x104c)
Current Host Receive Descriptor Register

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	HRDAP Host Receive Descriptor Address Pointer Cleared on Reset. Pointer updated by DMA during operation.

GMAC_CUR_HOST_TX_Buf_ADDR
Address: Operational Base + offset (0x1050)
Current Host Transmit Buffer Address Register

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	HTBAP Host Transmit Buffer Address Pointer Cleared on Reset. Pointer updated by DMA during operation.

GMAC_CUR_HOST_RX_BUF_ADDR
Address: Operational Base + offset (0x1054)
Current Host Receive Buffer Adderss Register

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	HRBAP Host Receive Buffer Address Pointer Cleared on Reset. Pointer updated by DMA during operation.

12.5 Interface Description

Table 12-1 RMII Interface Description

Module pin	Direction	Pad name	IOMUX setting
RGMII/RMII interface			
mac_clk	I/O	IO_LCD0d12_EBCsdce4_GMACclk_GPIO2b6	GRF_GPIO2B_IOMUX[13:12]=2'b11
mac_txen	O	IO_LCD0d11_EBCsdce3_GMACtxen_GPIO2b5	GRF_GPIO2B_IOMUX[11:10]=2'b11
mac_txd1	O	IO_LCD0d16_EBCgdsp_GMACtxd1_GPIO2c2	GRF_GPIO2C_IOMUX[5:4]=2'b11
mac_txd0	O	IO_LCD0d17_EBCgdpwr0_GMACtxd0_GPIO2c3	GRF_GPIO2C_IOMUX[7:6]=2'b11
mac_rxdv	I	IO_LCD0dclk_EBCsdclk_GMACrxdv_GPIO2b0	GRF_GPIO2B_IOMUX[1:0]=2'b11
mac_rxer	I	IO_LCD0d13_EBCsdce5_GMACrxer_GPIO2b7	GRF_GPIO2B_IOMUX[15:14]=2'b11
mac_rxd1	I	IO_LCD0d14_EBCvcom_GMACrxd1_GPIO2c0	GRF_GPIO2C_IOMUX[1:0]=2'b11
mac_rxd0	I	IO_LCD0d15_EBCgdoe_GMACrxd0_GPIO2c1	GRF_GPIO2C_IOMUX[3:2]=2'b11
Management interface			

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Module pin	Direction	Pad name	IOMUX setting
mac_mdio	I/O	IO_LCD0d10_EBCsdce2_GMACmdio_GPIO2b4	GRF_GPIO2B_IOMUX[9:8]=2'b11
mac_mdc	O	IO_LCD0d23_EBCgdpwr2_GMACmdc_GPIO2d1	GRF_GPIO2D_IOMUX[3:2]=2'b11

Table 12-2 RGMII Interface Description

Module pin	Direction	Pad name	IOMUX setting
RGMII/RMII interface			
mac_clk	I/O	IO_LCD0d12_EBCsdce4_GMACclk_GPIO2b6	GRF_GPIO2B_IOMUX[13:12]=2'b11
mac_txclk	O	IO_LCD0hsync_EBCsdle_GMACtxclk_GPIO2b1	GRF_GPIO2B_IOMUX[3:2]=2'b11
mac_txen	O	IO_LCD0d11_EBCsdce3_GMACtxen_GPIO2b5	GRF_GPIO2B_IOMUX[11:10]=2'b11
mac_txd3	O	IO_LCD0d21_EBCborder1_GPSmag_GMACtxd3_GPIO2c7	GRF_GPIO2C_IOMUX2[14:12]=3'b100
mac_txd2	O	IO_LCD0d20_EBCborder0_GPSsign_GMACtxd2_GPIO2c6	GRF_GPIO2C_IOMUX2[10:8]=3'b100
mac_txd1	O	IO_LCD0d16_EBCgdsp_GMACtxd1_GPIO2c2	GRF_GPIO2C_IOMUX[5:4]=2'b11
mac_txd0	O	IO_LCD0d17_EBCgdpwr0_GMACtxd0_GPIO2c3	GRF_GPIO2C_IOMUX[7:6]=2'b11
mac_rxclk	I	IO_LCD0den_EBCgdclk_GMACrxclk_GPIO2b3	GRF_GPIO2B_IOMUX[7:6]=2'b11
mac_rxdv	I	IO_LCD0dclk_EBCsdclk_GMACrxdv_GPIO2b0	GRF_GPIO2B_IOMUX[1:0]=2'b11
mac_rxd3	I	IO_LCD0d18_EBCgdrl_I2C2sda_GMACrxd3_GPIO2c4	GRF_GPIO2C_IOMUX2[2:0]=3'b100
mac_rxd2	I	IO_LCD0d19_EBCsdshr_I2C2scl_GMACrxd2_GPIO2c5	GRF_GPIO2C_IOMUX2[6:4]=3'b100
mac_rxd1	I	IO_LCD0d14_EBCvcom_GMACrxd1_GPIO2c0	GRF_GPIO2C_IOMUX[1:0]=2'b11
mac_rxd0	I	IO_LCD0d15_EBCgdoe_GMACrxd0_GPIO2c1	GRF_GPIO2C_IOMUX[3:2]=2'b11
mac_crs	I	IO_LCD0vsync_EBCsdoe_GMACcrs_GPIO2b2	GRF_GPIO2B_IOMUX[5:4]=2'b11
mac_col	I	IO_LCD0d22_EBCgdpwr1_GPSclk_GMACcol_GPIO2d0	GRF_GPIO2D_IOMUX[14:12]=3'b100
Management interface			
mac_mdio	I/O	IO_LCD0d10_EBCsdce2_GMACmdio_GPIO2b4	GRF_GPIO2B_IOMUX[9:8]=2'b11
mac_mdc	O	IO_LCD0d23_EBCgdpwr2_GMACmdc_GPIO2d1	GRF_GPIO2D_IOMUX[3:2]=2'b11

Notes: I=input, O=output, I/O=input/output, bidirectional

12.6 Application Notes

12.6.1 Descriptors

The DMA in GMAC can communicate with Host driver through descriptor lists and data buffers. The DMA transfers data frames received by the core to the Receive Buffer in the Host memory, and Transmit data frames from the Transmit Buffer in the Host memory. Descriptors that reside in the Host memory act as pointers to these buffers.
There are two descriptor lists; one for reception, and one for transmission. The base address of each list is written into DMA Registers RX_DESC_LIST_ADDR and TX_DESC_LIST_ADDR, respectively. A descriptor list is forward linked (either implicitly or explicitly). The last descriptor may point back to the first entry to create a ring structure. Explicit chaining of descriptors is accomplished by setting the second address chained in both Receive and Transmit descriptors (RDES1[24] and TDES1[24]). The descriptor lists resides in the Host physical memory address space. Each descriptor can point to a maximum of two buffers. This enables two buffers to be used, physically addressed, rather than contiguous buffers in memory.

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A data buffer resides in the Host physical memory space, and consists of an entire frame or part of a frame, but cannot exceed a single frame. Buffers contain only data, buffer status is maintained in the descriptor. Data chaining refers to frames that span multiple data buffers. However, a single descriptor cannot span multiple frames. The DMA will skip to the next frame buffer when end-of-frame is detected. Data chaining can be enabled or disabled The descriptor ring and chain structure is shown in following figure.

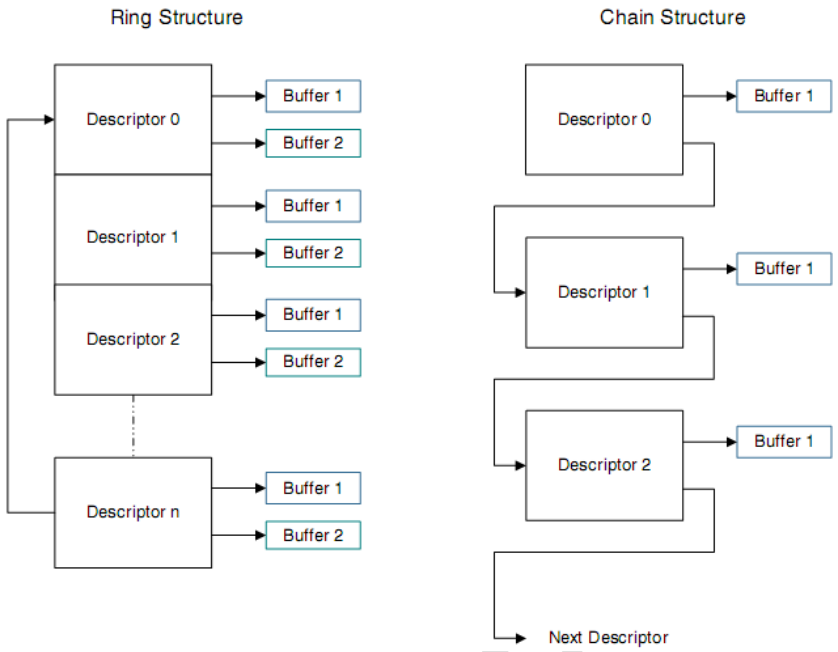


Fig. 12-10 Descriptor Ring and Chain Structure

Each descriptor contains two buffers, two byte-count buffers, and two address pointers, which enable the adapter port to be compatible with various types of memory management schemes. The descriptor addresses must be aligned to the bus width used (Word/Dword/Lword for 32/64/128-bit buses).

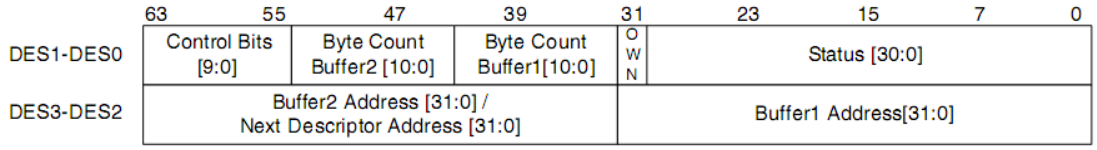


Fig. 12-11 Rx/Tx Descriptors definition

12.6.2 Receive Descriptor

The GMAC Subsystem requires at least two descriptors when receiving a frame. The Receive state machine of the DMA always attempts to acquire an extra descriptor in anticipation of an incoming frame. (The size of the incoming frame is unknown). Before the RxDMA closes a descriptor, it will attempt to acquire the next descriptor even if no frames are received.

In a single descriptor (receive) system, the subsystem will generate a descriptor error if the receive buffer is unable to accommodate the incoming frame and the next descriptor is not owned by the DMA. Thus, the Host is forced to increase either its descriptor pool or the buffer size. Otherwise, the subsystem starts dropping all incoming frames.

Receive Descriptor 0 (RDES0)

RDES0 contains the received frame status, the frame length, and the descriptor ownership information.

Table 12-3 Receive Descriptor 0

Bit	Description
31	OWN: Own Bit

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Bit	Description
	When set, this bit indicates that the descriptor is owned by the DMA of the GMAC Subsystem. When this bit is reset, this bit indicates that the descriptor is owned by the Host. The DMA clears this bit either when it completes the frame reception or when the buffers that are associated with this descriptor are full.
30	AFM: Destination Address Filter Fail When set, this bit indicates a frame that failed in the DA Filter in the GMAC Core.
29:16	FL: Frame Length These bits indicate the byte length of the received frame that was transferred to host memory (including CRC). This field is valid when Last Descriptor (RDES0[8]) is set and either the Descriptor Error (RDES0[14]) or Overflow Error bits are reset. The frame length also includes the two bytes appended to the Ethernet frame when IP checksum calculation (Type 1) is enabled and the received frame is not a MAC control frame. This field is valid when Last Descriptor (RDES0[8]) is set. When the Last Descriptor and Error Summary bits are not set, this field indicates the accumulated number of bytes that have been transferred for the current frame.
15	ES: Error Summary Indicates the logical OR of the following bits: • RDES0[0]: Payload Checksum Error • RDES0[1]: CRC Error • RDES0[3]: Receive Error • RDES0[4]: Watchdog Timeout • RDES0[6]: Late Collision • RDES0[7]: IPC Checksum • RDES0[11]: Overflow Error • RDES0[14]: Descriptor Error This field is valid only when the Last Descriptor (RDES0[8]) is set.
14	DE: Descriptor Error When set, this bit indicates a frame truncation caused by a frame that does not fit within the current descriptor buffers, and that the DMA does not own the Next Descriptor. The frame is truncated. This field is valid only when the Last Descriptor (RDES0[8]) is set
13	SAF: Source Address Filter Fail When set, this bit indicates that the SA field of frame failed the SA Filter in the GMAC Core.
12	LE: Length Error When set, this bit indicates that the actual length of the frame received and that the Length/ Type field does not match. This bit is valid only when the Frame Type (RDES0[5]) bit is reset. Length error status is not valid when CRC error is present.
11	OE: Overflow Error When set, this bit indicates that the received frame was damaged due to buffer overflow.
10	VLAN: VLAN Tag When set, this bit indicates that the frame pointed to by this descriptor is a VLAN frame tagged by the GMAC Core.
9	FS: First Descriptor When set, this bit indicates that this descriptor contains the first buffer of the frame. If the size of the first buffer is 0, the second buffer contains the beginning of the frame. If the size of the second buffer is also 0, the next Descriptor contains the beginning of the frame.
8	LS: Last Descriptor When set, this bit indicates that the buffers pointed to by this descriptor are the last buffers of the frame.
7	IPC Checksum Error/Giant Frame

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Bit	Description
	When IP Checksum Engine is enabled, this bit, when set, indicates that the 16-bit IPv4 Header checksum calculated by the core did not match the received checksum bytes. The Error Summary bit[15] is NOT set when this bit is set in this mode.
6	LC: Late Collision When set, this bit indicates that a late collision has occurred while receiving the frame in Half-Duplex mode.
5	FT: Frame Type When set, this bit indicates that the Receive Frame is an Ethernet-type frame (the LT field is greater than or equal to 16'h0600). When this bit is reset, it indicates that the received frame is an IEEE802.3 frame. This bit is not valid for Runt frames less than 14 bytes.
4	RWT: Receive Watchdog Timeout When set, this bit indicates that the Receive Watchdog Timer has expired while receiving the current frame and the current frame is truncated after the Watchdog Timeout.
3	RE: Receive Error When set, this bit indicates that the gmii_rxer_i signal is asserted while gmii_rxdv_i is asserted during frame reception. This error also includes carrier extension error in GMII and Half-duplex mode. Error can be of less/no extension, or error (rxd $\neq$ 0f) during extension.
2	DE: Dribble Bit Error When set, this bit indicates that the received frame has a non-integer multiple of bytes (odd nibbles). This bit is valid only in MII Mode.
1	CE: CRC Error When set, this bit indicates that a Cyclic Redundancy Check (CRC) Error occurred on the received frame. This field is valid only when the Last Descriptor (RDES0[8]) is set.
0	Rx MAC Address/Payload Checksum Error When set, this bit indicates that the Rx MAC Address registers value (1 to 15) matched the frame's DA field. When reset, this bit indicates that the Rx MAC Address Register 0 value matched the DA field. If Full Checksum Offload Engine is enabled, this bit, when set, indicates the TCP, UDP, or ICMP checksum the core calculated does not match the received encapsulated TCP, UDP, or ICMP segment's Checksum field. This bit is also set when the received number of payload bytes does not match the value indicated in the Length field of the encapsulated IPv4 or IPv6 datagram in the received Ethernet frame.

Receive Descriptor 1 (RDES1)

RDES1 contains the buffer sizes and other bits that control the descriptor chain/ring.

Table 12-4 Receive Descriptor 1

Bit	Description
31	Disable Interrupt on Completion When set, this bit will prevent the setting of the RI (CSR5[6]) bit of the GMAC_STATUS Register for the received frame that ends in the buffer pointed to by this descriptor. This, in turn, will disable the assertion of the interrupt to Host due to RI for that frame.
30:26	Reserved.
25	RER: Receive End of Ring When set, this bit indicates that the descriptor list reached its final descriptor. The DMA returns to the base address of the list, creating a Descriptor Ring.
24	RCH: Second Address Chained When set, this bit indicates that the second address in the descriptor is the Next Descriptor address rather than the second buffer address. When RDES1[24] is

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Bit	Description
	set, RBS2 (RDES1[21-11]) is a "don't care" value. RDES1[25] takes precedence over RDES1[24].
23:22	Reserved.
21:11	RBS2: Receive Buffer 2 Size These bits indicate the second data buffer size in bytes. The buffer size must be a multiple of 8 depending upon the bus widths (64), even if the value of RDES3 (buffer2 address pointer) is not aligned to bus width. In the case where the buffer size is not a multiple of 8, the resulting behavior is undefined. This field is not valid if RDES1[24] is set.
10:0	RBS1: Receive Buffer 1 Size Indicates the first data buffer size in bytes. The buffer size must be a multiple of 8 depending upon the bus widths (64), even if the value of RDES2 (buffer1 address pointer) is not aligned. In the case where the buffer size is not a multiple of 8, the resulting behavior is undefined. If this field is 0, the DMA ignores this buffer and uses Buffer 2 or next descriptor depending on the value of RCH (Bit 24).

Receive Descriptor 2 (RDES2)

RDES2 contains the address pointer to the first data buffer in the descriptor.

Table 12-5 Receive Descriptor 2

Bit	Description
31:0	Buffer 1 Address Pointer These bits indicate the physical address of Buffer 1. There are no limitations on the buffer address alignment except for the following condition: The DMA uses the configured value for its address generation when the RDES2 value is used to store the start of frame. Note that the DMA performs a write operation with the RDES2[2:0] bits as 0 during the transfer of the start of frame but the frame data is shifted as per the actual Buffer address pointer. The DMA ignores RDES2[2:0] (corresponding to bus width of 64) if the address pointer is to a buffer where the middle or last part of the frame is stored.

Receive Descriptor 3 (RDES3)

RDES3 contains the address pointer either to the second data buffer in the descriptor or to the next descriptor.

Table 12-6 Receive Descriptor 3

Bit	Description
31:0	Buffer 2 Address Pointer (Next Descriptor Address) These bits indicate the physical address of Buffer 2 when a descriptor ring structure is used. If the Second Address Chained (RDES1[24]) bit is set, this address contains the pointer to the physical memory where the Next Descriptor is present. If RDES1[24] is set, the buffer (Next Descriptor) address pointer must be bus width-aligned (RDES3[2:0] = 0, corresponding to a bus width of 64. LSBs are ignored internally.) However, when RDES1[24] is reset, there are no limitations on the RDES3 value, except for the following condition: The DMA uses the configured value for its buffer address generation when the RDES3 value is used to store the start of frame. The DMA ignores RDES3[2:0] (corresponding to a bus width of 64) if the address pointer is to a buffer where the middle or last part of the frame is stored.

12.6.3 Transmit Descriptor

The descriptor addresses must be aligned to the bus width used (64). Each descriptor is provided with two buffers, two byte-count buffers, and two address pointers, which enable

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the adapter port to be compatible with various types of memory-management schemes.

Transmit Descriptor 0 (TDES0)

TDES0 contains the transmitted frame status and the descriptor ownership information.

Table 12-7 Transmit Descriptor 0

Bit	Description
31	OWN: Own Bit When set, this bit indicates that the descriptor is owned by the DMA. When this bit is reset, this bit indicates that the descriptor is owned by the Host. The DMA clears this bit either when it completes the frame transmission or when the buffers allocated in the descriptor are empty. The ownership bit of the First Descriptor of the frame should be set after all subsequent descriptors belonging to the same frame have been set. This avoids a possible race condition between fetching a descriptor and the driver setting an ownership bit.
30:17	Reserved.
16	IHE: IP Header Error When set, this bit indicates that the Checksum Offload engine detected an IP header error and consequently did not modify the transmitted frame for any checksum insertion.
15	ES: Error Summary Indicates the logical OR of the following bits: • TDES0[14]: Jabber Timeout • TDES0[13]: Frame Flush • TDES0[11]: Loss of Carrier • TDES0[10]: No Carrier • TDES0[9]: Late Collision • TDES0[8]: Excessive Collision • TDES0[2]: Excessive Deferral • TDES0[1]: Underflow Error
14	JT: Jabber Timeout When set, this bit indicates the GMAC transmitter has experienced a jabber time-out.
13	FF: Frame Flushed When set, this bit indicates that the DMA/MTL flushed the frame due to a SW flush command given by the CPU.
12	PCE: Payload Checksum Error This bit, when set, indicates that the Checksum Offload engine had a failure and did not insert any checksum into the encapsulated TCP, UDP, or ICMP payload. This failure can be either due to insufficient bytes, as indicated by the IP Header's Payload Length field, or the MTL starting to forward the frame to the MAC transmitter in Store-and-Forward mode without the checksum having been calculated yet. This second error condition only occurs when the Transmit FIFO depth is less than the length of the Ethernet frame being transmitted: to avoid deadlock, the MTL starts forwarding the frame when the FIFO is full, even in Store-and-Forward mode.
11	LC: Loss of Carrier When set, this bit indicates that Loss of Carrier occurred during frame transmission. This is valid only for the frames transmitted without collision and when the GMAC operates in Half-Duplex Mode.
10	NC: No Carrier When set, this bit indicates that the carrier sense signal form the PHY was not asserted during transmission.
9	LC: Late Collision When set, this bit indicates that frame transmission was aborted due to a collision occurring after the collision window (64 byte times including Preamble in RMII Mode and 512 byte times including Preamble and Carrier Extension in

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Bit	Description
	RGMII Mode). Not valid if Underflow Error is set.
8	EC: Excessive Collision When set, this bit indicates that the transmission was aborted after 16 successive collisions while attempting to transmit the current frame. If the DR (Disable Retry) bit in the GMAC Configuration Register is set, this bit is set after the first collision and the transmission of the frame is aborted.
7	VF: VLAN Frame When set, this bit indicates that the transmitted frame was a VLAN-type frame.
6:3	CC: Collision Count This 4-bit counter value indicates the number of collisions occurring before the frame was transmitted. The count is not valid when the Excessive Collisions bit (TDES0[8]) is set.
2	ED: Excessive Deferral When set, this bit indicates that the transmission has ended because of excessive deferral of over 24,288 bit times (155,680 bits times in 1000-Mbps mode) if the Deferral Check (DC) bit is set high in the GMAC Control Register.
1	UF: Underflow Error When set, this bit indicates that the GMAC aborted the frame because data arrived late from the Host memory. Underflow Error indicates that the DMA encountered an empty Transmit Buffer while transmitting the frame. The transmission process enters the suspended state and sets both Transmit Underflow (Register GMAC_STATUS[5]) and Transmit Interrupt (Register GMAC_STATUS [0]).
0	DB: Deferred Bit When set, this bit indicates that the GMAC defers before transmission because of the presence of carrier. This bit is valid only in Half-Duplex mode.

Transmit Descriptor 1 (TDES1)

TDES1 contains the buffer sizes and other bits which control the descriptor chain/ring and the frame being transferred.

Table 12-8 Transmit Descriptor 1

Bit	Description
31	IC: Interrupt on Completion When set, this bit sets Transmit Interrupt (Register 5[0]) after the present frame has been transmitted.
30	LS: Last Segment When set, this bit indicates that the buffer contains the last segment of the frame.
29	FS: First Segment When set, this bit indicates that the buffer contains the first segment of a frame.
28:27	CIC: Checksum Insertion Control These bits control the insertion of checksums in Ethernet frames that encapsulate TCP, UDP, or ICMP over IPv4 or IPv6 as described below. • 2'b00: Do nothing. Checksum Engine is bypassed • 2'b01: Insert IPv4 header checksum. Use this value to insert IPv4 header checksum when the frame encapsulates an IPv4 datagram. • 2'b10: Insert TCP/UDP/ICMP checksum. The checksum is calculated over the TCP, UDP, or ICMP segment only and the TCP, UDP, or ICMP pseudo-header checksum is assumed to be present in the corresponding input frame's Checksum field. An IPv4 header checksum is also inserted if the encapsulated datagram conforms to IPv4. • 2'b11: Insert a TCP/UDP/ICMP checksum that is fully calculated in this engine. In other words, the TCP, UDP, or ICMP pseudo-header is included in the checksum calculation, and the input frame's corresponding Checksum field has an all-zero

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Bit	Description
	value. An IPv4 Header checksum is also inserted if the encapsulated datagram conforms to IPv4. The Checksum engine detects whether the TCP, UDP, or ICMP segment is encapsulated in IPv4 or IPv6 and processes its data accordingly.
26	DC: Disable CRC When set, the GMAC does not append the Cyclic Redundancy Check (CRC) to the end of the transmitted frame. This is valid only when the first segment (TDES1[29]).
25	TER: Transmit End of Ring When set, this bit indicates that the descriptor list reached its final descriptor. The returns to the base address of the list, creating a descriptor ring.
24	TCH: Second Address Chained When set, this bit indicates that the second address in the descriptor is the Next Descriptor address rather than the second buffer address. When TDES1[24] is set, TBS2 (TDES1[21–11]) are "don't care" values. TDES1[25] takes precedence over TDES1[24].
23	DP: Disable Padding When set, the GMAC does not automatically add padding to a frame shorter than 64 bytes. When this bit is reset, the DMA automatically adds padding and CRC to a frame shorter than 64 bytes and the CRC field is added despite the state of the DC (TDES1[26]) bit. This is valid only when the first segment (TDES1[29]) is set.
22	Reserved.
21:11	TBS2: Transmit Buffer 2 Size These bits indicate the Second Data Buffer in bytes. This field is not valid if TDES1[24] is set.
10:0	TBS1: Transmit Buffer 1 Size These bits indicate the First Data Buffer byte size. If this field is 0, the DMA ignores this buffer and uses Buffer 2 or next descriptor depending on the value of TCH (Bit 24).

Transmit Descriptor 2 (TDES2)

TDES2 contains the address pointer to the first buffer of the descriptor.

Table 12-9 Transmit Descriptor 2

Bit	Description
31:0	Buffer 1 Address Pointer These bits indicate the physical address of Buffer 1. There is no limitation on the buffer address alignment.

Transmit Descriptor 3 (TDES3)

TDES3 contains the address pointer either to the second buffer of the descriptor or the next descriptor.

Table 12-10 Transmit Descriptor 3

Bit	Description
31:0	Buffer 2 Address Pointer (Next Descriptor Address) Indicates the physical address of Buffer 2 when a descriptor ring structure is used. If the Second Address Chained (TDES1[24]) bit is set, this address contains the pointer to the physical memory where the Next Descriptor is present. The buffer address pointer must be aligned to the bus width only when TDES1[24] is set. (LSBs are ignored internally.)

12.6.4 Programming Guide

DMA Initialization – Descriptors

The following operations must be performed to initialize the DMA.

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1. Provide a software reset. This will reset all of the GMAC internal registers and logic. (GMAC_OP_MODE[0]).
2. Wait for the completion of the reset process (poll GMAC_OP_MODE[0], which is only cleared after the reset operation is completed).
3. Program the following fields to initialize the Bus Mode Register by setting values in register GMAC_BUS_MODE
   a. Mixed Burst and AAL
   b. Fixed burst or undefined burst
   c. Burst length values and burst mode values.
   d. Descriptor Length (only valid if Ring Mode is used)
   e. Tx and Rx DMA Arbitration scheme
4. Program the AXI Interface options in the register GMAC_BUS_MODE
   a. If fixed burst-length is enabled, then select the maximum burst-length possible on the AXI bus (Bits[7:1])
5. A proper descriptor chain for transmit and receive must be created. It should also ensure that the receive descriptors are owned by DMA (bit 31 of descriptor should be set). When OSF mode is used, at least two descriptors are required.
6. Software should create three or more different transmit or receive descriptors in the chain before reusing any of the descriptors.
7. Initialize receive and transmit descriptor list address with the base address of transmit and receive descriptor (register GMAC_RX_DESC_LIST_ADDR and GMAC_TX_DESC_LIST_ADDR).
8. Program the following fields to initialize the mode of operation by setting values in register GMAC_OP_MODE
   a. Receive and Transmit Store And Forward
   b. Receive and Transmit Threshold Control (RTC and TTC)
   c. Hardware Flow Control enable
   d. Flow Control Activation and De-activation thresholds for MTL Receive and Transmit FIFO (RFA and RFD)
   e. Error Frame and undersized good frame forwarding enable
   f. OSF Mode
9. Clear the interrupt requests, by writing to those bits of the status register (interrupt bits only) which are set. For example, by writing 1 into bit 16 - normal interrupt summary will clear this bit (register GMAC_STATUS).
10. Enable the interrupts by programming the interrupt enable register GMAC_INT_ENA.
11. Start the Receive and Transmit DMA by setting SR (bit 1) and ST (bit 13) of the control register GMAC_OP_MODE.

MAC Initialization

The following MAC Initialization operations can be performed after the DMA initialization sequence. If the MAC Initialization is done before the DMA is set-up, then enable the MAC receiver (last step below) only after the DMA is active. Otherwise, received frames will fill the RxFIFO and overflow.
1. Program the register GMAC_GMII_ADDR for controlling the management cycles for external PHY, for example, Physical Layer Address PA (bits 15-11). Also set bit 0 (GMII Busy) for writing into PHY and reading from PHY.
2. Read the 16-bit data of (GMAC_GMII_DATA) from the PHY for link up, speed of operation, and mode of operation, by specifying the appropriate address value in register GMAC_GMII_ADDR (bits 15-11).
3. Provide the MAC address registers (GMAC_MAC_ADDR0_HI and GMAC_MAC_ADDR0_LO).
4. If Hash filtering is enabled in your configuration, program the Hash filter register (GMAC_HASH_TAB_HI and GMAC_HASH_TAB_LO).
5. Program the following fields to set the appropriate filters for the incoming frames in register GMAC_MAC_FRM_FILT
   a. Receive All
   b. Promiscuous mode

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c. Hash or Perfect Filter
d. Unicast, Multicast, broad cast and control frames filter settings etc.
6. Program the following fields for proper flow control in register GMAC_FLOW_CTRL.
a. Pause time and other pause frame control bits
b. Receive and Transmit Flow control bits
c. Flow Control Busy/Backpressure Activate
7. Program the Interrupt Mask register bits, as required, and if applicable, for your configuration.
8. Program the appropriate fields in register GMAC_MAC_CONF for example, Inter-frame gap while transmission, jabber disable, etc. Based on the Auto-negotiation you can set the Duplex mode (bit 11), port select (bit 15), etc.
9. Set the bits Transmit enable (TE bit-3) and Receive Enable (RE bit-2) in register GMAC_MAC_CONF.

Normal Receive and Transmit Operation
For normal operation, the following steps can be followed.
- For normal transmit and receive interrupts, read the interrupt status. Then poll the descriptors, reading the status of the descriptor owned by the Host (either transmit or receive).
- On completion of the above step, set appropriate values for the descriptors, ensuring that transmit and receive descriptors are owned by the DMA to resume the transmission and reception of data.
- If the descriptors were not owned by the DMA (or no descriptor is available), the DMA will go into SUSPEND state. The transmission or reception can be resumed by freeing the descriptors and issuing a poll demand by writing 0 into the Tx/Rx poll demand register (GMAC_TX_POLL_DEMAND and GMAC_RX_POLL_DEMAND).
- The values of the current host transmitter or receiver descriptor address pointer can be read for the debug process (GMAC_CUR_HOST_TX_DESC and GMAC_CUR_HOST_RX_DESC).
- The values of the current host transmit buffer address pointer and receive buffer address pointer can be read for the debug process (GMAC_CUR_HOST_TX_Buf_ADDR and GMAC_CUR_HOST_RX_BUF_ADDR).

Stop and Start Operation
When the transmission is required to be paused for some time then the following steps can be followed.
1. Disable the Transmit DMA (if applicable), by clearing ST (bit 13) of the control register GMAC_OP_MODE.
2. Wait for any previous frame transmissions to complete. This can be checked by reading the appropriate bits of MAC Debug register.
3. Disable the MAC transmitter and MAC receiver by clearing the bits Transmit enable (TE bit-3) and Receive Enable (RE bit-2) in register GMAC_MAC_CONF.
4. Disable the Receive DMA (if applicable), after making sure the data in the RX FIFO is transferred to the system memory (by reading the register GMAC_DEBUG).
5. Make sure both the TX FIFO and RX FIFO are empty.
6. To re-start the operation, start the DMAs first, before enabling the MAC Transmitter and Receiver.

12.6.5 Clock Architecture

In RMII mode, reference clock and TX/RX clock can be from CRU or external OSC as following figure.
The mux select rmii_speed is GRF_MAC_CON1[11].

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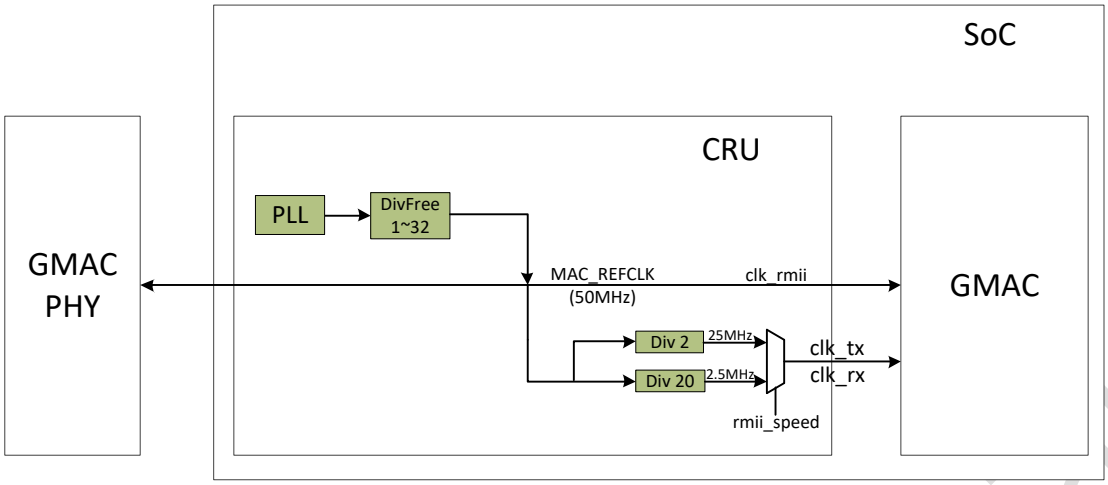


Fig. 12-12 RMII clock architecture when clock source from CRU

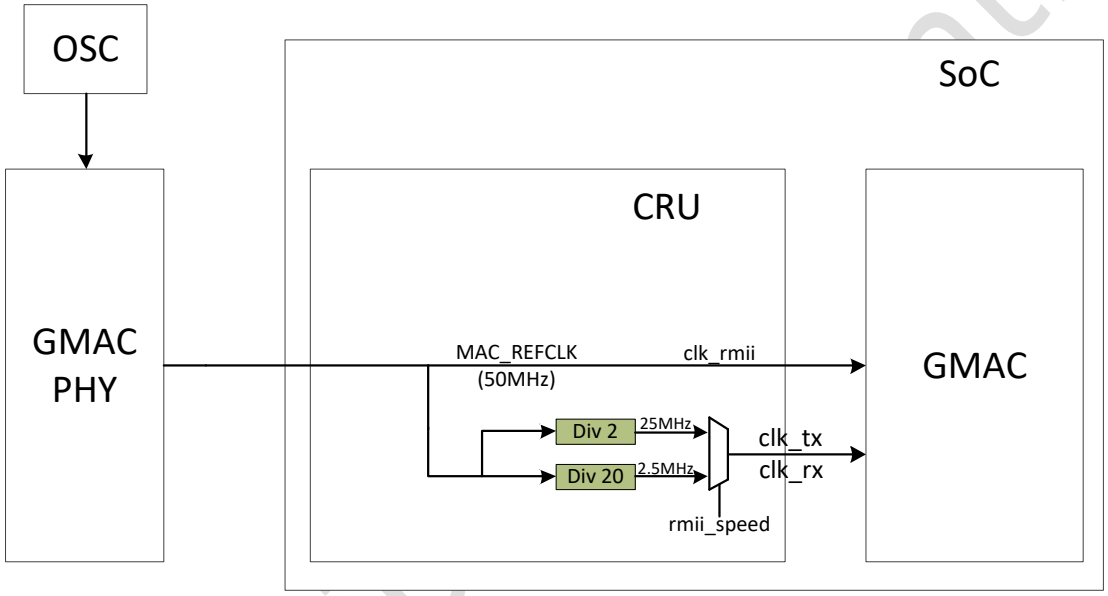


Fig. 12-13 RMII clock architecture when clock source from external OSC

In RGMII mode, clock architecture only supports that TX clock source is from CRU as following figure.

In order to dynamically adjust the timing between TX/RX clocks with data, deleyline is integrated in TX and RX clock path. Register GRF_MAC_CON0[15:14] can enable the deleylines, and GRF_MAC_CON0[13:0] is used to determine the delay length. There are 100 deley elements in each delayline.

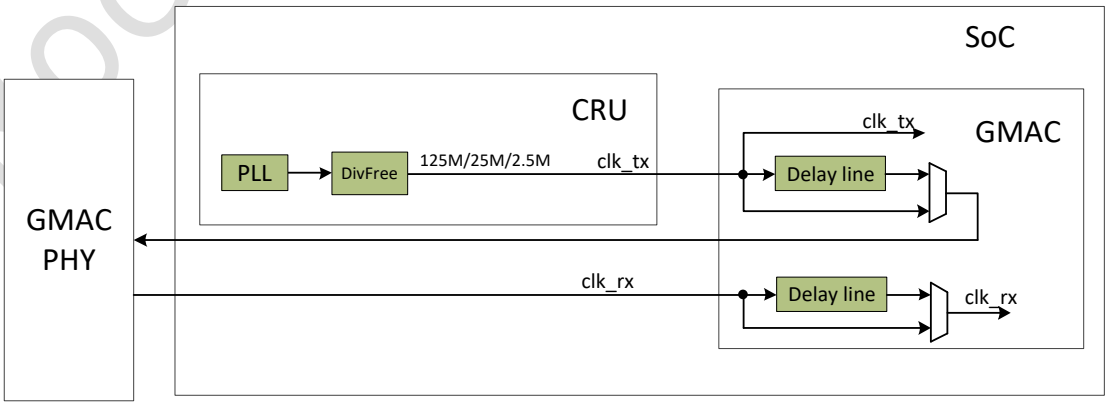


Fig. 12-14 RGMII clock architecture when clock source from CRU

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12.6.6 Remote Wake-Up Frame Filter Register

The register wkupfmfilter_reg, address (028H), loads the Wake-up Frame Filter register. To load values in a Wake-up Frame Filter register, the entire register (wkupfmfilter_reg) must be written. The wkupfmfilter_reg register is loaded by sequentially loading the eight register values in address (028) for wkupfmfilter_reg0, wkupfmfilter_reg1, ..., wkupfmfilter_reg7, respectively. Wkupfmfilter_reg is read in the same way.
The internal counter to access the appropriate wkupfmfilter_reg is incremented when lane3 (or lane 0 in big-endian) is accessed by the CPU. This should be kept in mind if you are accessing these registers in byte or half-word mode.

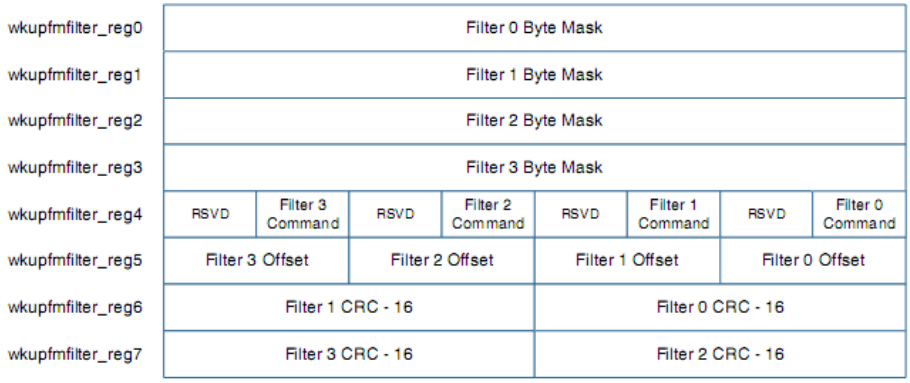


Fig. 12-15 Wake-Up Frame Filter Register

Filter i Byte Mask
This register defines which bytes of the frame are examined by filter i (0, 1, 2, and 3) in order to determine whether or not the frame is a wake-up frame. The MSB (thirty-first bit) must be zero. Bit j [30:0] is the Byte Mask. If bit j (byte number) of the Byte Mask is set, then Filter i Offset + j of the incoming frame is processed by the CRC block; otherwise Filter i Offset + j is ignored.
Filter i Command
This 4-bit command controls the filter i operation. Bit 3 specifies the address type, defining the pattern's destination address type. When the bit is set, the pattern applies to only multicast frames; when the bit is reset, the pattern applies only to unicast frame. Bit 2 and Bit 1 are reserved. Bit 0 is the enable for filter i; if Bit 0 is not set, filter i is disabled.
Filter i Offset
This register defines the offset (within the frame) from which the frames are examined by filter i. This 8-bit pattern-offset is the offset for the filter i first byte to examined. The minimum allowed is 12, which refers to the 13th byte of the frame (offset value 0 refers to the first byte of the frame).
Filter i CRC-16
This register contains the CRC_16 value calculated from the pattern, as well as the byte mask programmed to the wake-up filter register block.

12.6.7 System Consideration During Power-Down

GMAC neither gates nor stops clocks when Power-Down mode is enabled. Power saving by clock gating must be done outside the core by the CRU. The receive data path must be clocked with clk_rx_i during Power-Down mode, because it is involved in magic packet/wake-on-LAN frame detection. However, the transmit path and the APB path clocks can be gated off during Power-Down mode.
The PMT interrupt is asserted when a valid wake-up frame is received. This interrupt is generated in the clk_rx domain.
The recommended power-down and wake-up sequence is as follows.
1. Disable the Transmit DMA (if applicable) and wait for any previous frame transmissions to complete. These transmissions can be detected when Transmit Interrupt (TI - Register GMAC_STATUS[0]) is received.
2. Disable the MAC transmitter and MAC receiver by clearing the appropriate bits in the

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MAC Configuration register.
3. Wait until the Receive DMA empties all the frames from the Rx FIFO (a software timer may be required).
4. Enable Power-Down mode by appropriately configuring the PMT registers.
5. Enable the MAC Receiver and enter Power-Down mode.
6. Gate the APB and transmit clock inputs to the core (and other relevant clocks in the system) to reduce power and enter Sleep mode.
7. On receiving a valid wake-up frame, the GMAC asserts the PMT interrupt signal and exits Power-Down mode.
8. On receiving the interrupt, the system must enable the APB and transmit clock inputs to the core.
9. Read the register GMAC_PMT_CTRL_STA to clear the interrupt, then enable the other modules in the system and resume normal operation.

12.6.8 GRF Register Summary

GRF Register	Register Description
GRF_MAC_CON1[8:6]	PHY interface select 3'b001: RGMII 3'b100: RMII All others: Reserved
GRF_MAC_CON1[9]	GMAC transmit flow control When set high, instructs the GMAC to transmit PAUSE Control frames in Full-duplex mode. In Half-duplex mode, the GMAC enables the Back-pressure function until this signal is made low again
GRF_MAC_CON1[10]	GMAC speed 1'b1: 100-Mbps 1'b0: 10-Mbps
GRF_MAC_CON1[11]	RMII clock selection 1'b1: 25MHz 1'b0: 2.5MHz
GRF_MAC_CON1[13:12]	RGMII clock selection 2'b00: 125MHz 2'b11: 25MHz 2'b10: 2.5MHz
GRF_MAC_CON1[14]	RMII mode selection 1'b1: RMII mode 1’b0: Reserved
GRF_MAC_CON0[6:0]	RGMII TX clock delayline value
GRF_MAC_CON0[13:7]	RGMII RX clock delayline value
GRF_MAC_CON0[14]	RGMII TX clock delayline enable 1'b1: enable 1'b0: disable
GRF_MAC_CON0[15]	RGMII RX clock delayline enable 1'b1: enable 1'b0: disable

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Chapter 13 Debug

13.1 Overview

The chip uses the DAPLITE Technology to support real-time debug.

13.1.1 Features

- Invasive debug with core halted
- SW-DP

13.1.2 Debug components address map

The following table shows the debug components address in memory map:

Module	Base Address
DAP_ROM	0x20020000

13.2 Block Diagram

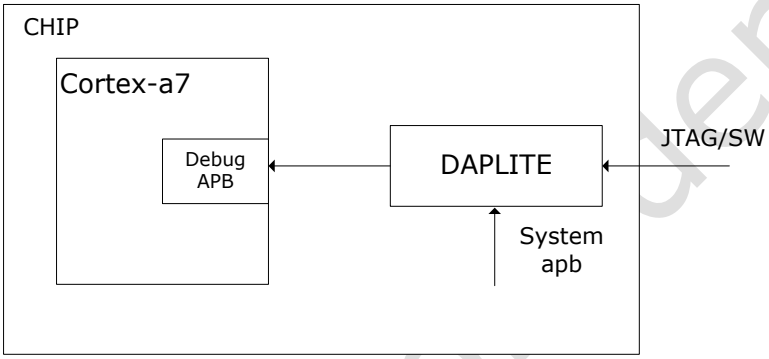


Fig. 13-1 Debug system structure

13.3 Function description

13.3.1 DAP

The DAP has following components:

- Serial Wire JTAG Debug Port(SWJ-DP)
- APB Access Port(APB-AP)
- ROM table

The debug port is the host tools interface to access the DAP-Lit. This interface controls any access ports provided within the DAP-Lite. The DAP-Lite supports a combined debug port which includes both JTAG and Serial Wire Debug(SWD), with a mechanism that supports switching between them.
The APB-AP acts as a bridge between SWJ-DP and APB bus which translate the Debug request to APB bus.
The DAP provides an internal ROM table connected to the master Debug APB port of the APB-Mux. The Debug ROM table is loaded at address 0x00000000 and 0x80000000 of this bus and is accessible from both APB-AP and the system APB input. Bit [31] of the address bus is not connected to the ROM Table, ensuring that both views read the same value. The ROM table stores the locations of the components on the Debug APB.

13.4 Register description

13.4.1 DAP APB-AP register summary

Name	Offset	Size	Reset Value	Description
DAP_CSW	0x0000	W	0x00000002	Control/Status Word, CSW
DAP_TAR	0x0004	W	0x00000000	Transfer Address, TAR

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Name	Offset	Size	Reset Value	Description
Reserved	0x0008	W	NA	Reserved
DAP_DRW	0x000c	W	NA	Data Read/Write, DRW
DAP_BD0	0x0010	W	NA	Bank Data 0, BD0
DAP_BD1	0x0014	W	NA	Bank Data 1, BD1
DAP_BD2	0x0018	W	NA	Bank Data 2, BD2
DAP_BD3	0x001c	W	NA	Bank Data 3, BD3
DAP_ROM_ADDR	0x00f8	W	NA	Debug ROM Address, ROM
DAP_IDR	0x00fc	W	0x14770002	Identification Register, IDR

13.4.2 DAP APB-AP Detailed Register Description

DAP_CSW
Address: APBAP_BASE + offset(0x000)
Control/Status Word

Bit	Attr	Reset Value	Description
31	RW	0x0	Software access enable. Drives DBGSWENABLE to enable or disable software access to the Debug APB bus in the APB multiplexor. 1'b1 = Enable software access 1'b0 = Disable software access. Reset value = 1'b0. On exit from reset, defaults to b1 to enable software access.
31:12	RW	0x0	Reserved
11:8	R	0x0	Specifies the mode of operation. 4'b0000 = Normal download/upload model 4'b0001-4'b1111 = Reserved Reset value = 4'b0000.
7	R	0x0	Transfer in progress. This field indicates if a transfer is currently in progress on the APB master port.
6	R	0x0	Transfer in progress. This field indicates if a transfer is currently in progress on the APB master port. Indicates the status of the DEVICEEN input. • If APB-AP is connected to the Debug APB, that is, a bus connected only to debug and trace components, it must be permanently enabled by tying DEVICEEN HIGH. This ensures that trace components can still be programmed when DBGEN is LOW. In practice, it is expected that the APB-AP is almost always used in this way. • If APB-AP is connected to a system APB dedicated to the non-secure world, DEVICEEN must be connected to DBGEN. • If APB-AP is connected to a system APB dedicated to the secure world, DEVICEEN must be connected to SPIDEN.

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Bit	Attr	Reset Value	Description
5:4	RW	0x0	Auto address increment and packing mode on Read or Write data access. Does not increment if the transaction completes with an error response or the transaction is aborted. Auto address incrementing is not performed on access to banked data registers0x10-0x1C.The status of these bits is ignored in these cases. 2'b11 = Reserved 2'b10 = Reserved 2'b01 = Increment 2'b00 = Auto increment OFF. Increment occurs in word steps. Reset value = 2'b00.
3	R	0x0	Reserved
2:0	R	0x2	Size of the access to perform. Fixed at 3'b010 = 32 bits. Reset value = 3'b010.

DAP_TAR
Address: APBAP_BASE + offset(0x004)
Transfer Address

Bit	Attr	Reset Value	Description
31:2	RW	0x0	Address[31:2] of the current transfer PADDR[31:2]=TAR[31:2] for accesses from Data Read/Write Register at 0x0C. PADDR[31:2]=TAR[31:4]+DAPADDR[3:2] for accesses from Banked Data Registers at 0x10-0x1C and 0x0C.
1:0	R	0x0	Reserved

DAP_DRW
Address: APBAP_BASE + offset(0x00c)
Data Read/Write

Bit	Attr	Reset Value	Description
31:0	RW	0x0	Write mode: Data value to write for the current transfer. Read mode: Data value read from the current transfer.

DAP_BD0-DAP_BD3
Address: APBAP_BASE + offset(0x010) - APBAP_BASE + offset(0x01c)
Bank Data 0-3

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Bit	Attr	Reset Value	Description
31:0	RW	0x0	If DAPADDR[7:4] = 0x0001, so accessing APB-AP registers in the range 0x10-0x1C, then the derived PADDR[31:0] is: • Write mode: Data value to write for the current transfer to external address TAR[31:4]+ DAPADDR[3:2] + 2'b00. • Read mode: Data value read from the current transfer from external address TAR[31:4]+ DAPADDR[3:2] + 2'b00. Auto address incrementing is not performed on DAP accesses to BD0-BD3. Reset value = 0x00000000

DAP_ROM_ADDR
Address: 0xf8
ROM address

Bit	Attr	Reset Value	Description
31:12	R	0x800000	Base address of the ROM Table The ROM provides a look-up table of all CoreSight Debug APB components. Read only. Set to 0xFFFFF if no ROM is present. In the initial CoreSight release this must be set to 0x80000.
11:0	R	0x000	Set to 0x000 if ROM is present. Set to 0xFFF if ROM table is not present. In the initial CoreSight release this must be set to 0x000.

DAP_IDR
Address: APBAP_BASE + offset(0x0fc)

Bit	Attr	Reset Value	Description
31:28	R	0x1	Revision. Reset value is 0x1 for APB-AP.
27:24	R	0x4	JEDEC bank. 0x4 indicates ARM Limited.
23:17	R	0x3b	JEDEC code. 0x3B indicates ARM Limited.
16	R	0x1	Memory AP. 0x1 indicates a standard register map is used.
15:8	R	0x00	Reserved
7:0	R	0x02	Identity value. Reset value is 0x02 for APB-AP.

13.4.3 DAP-ROM register summary

Name	Offset	Size	Reset Value	Description
DAP_ROMENTRY0	0x0000	W	0x00001003	CTI4 entry register
DAP_ROMENTRY1	0x0004	W	0x00002003	TPIU entry register
DAP_ROMENTRY2	0x0008	W	0x00003003	Trace Funnel register
DAP_ROMENTRY3	0x000c	W	0x00004003	Cortex-A9 ROM entry register
DAP_ROM_PERIPHID4	0x0fd0	W	0x00000004	Peripheral ID4
DAP_ROM_PERIPHID5	0x0fd4	W	0x00000000	Peripheral ID5
DAP_ROM_PERIPHID6	0x0fd8	W	0x00000000	Peripheral ID6
DAP_ROM_PERIPHID7	0x0fdc	W	0x00000000	Peripheral ID7
DAP_ROM_PERIPHID0	0x0fe0	W	0x000000c4	Peripheral ID0
DAP_ROM_PERIPHID1	0x0fe4	W	0x000000b4	Peripheral ID1

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Name	Offset	Size	Reset Value	Description
DAP_ROM_PERIPHID2	0x0fe8	W	0x0000006b	Peripheral ID2
DAP_ROM_PERIPHID3	0x0fec	W	0x00000020	Peripheral ID3
DAP_ROM_COMPONID0	0x0ff0	W	0x0000000d	Component ID0
DAP_ROM_COMPONID1	0x0ff4	W	0x00000010	Component ID1
DAP_ROM_COMPONID2	0x0ff8	W	0x00000005	Component ID2
DAP_ROM_COMPONID3	0x0ffc	W	0x000000b1	Component ID3

13.4.4 DAP-ROM Detailed Register Description

DAP_ROMENTRY0
Address: DAPROM_BASE + offset(0x0000)
TPIU entry register

Bit	Attr	Reset Value	Description
31:0	R	0x00001003	TPIU entry register

DAP_ROMENTRY1
Address: DAPROM_BASE + offset(0x0004)
Cortex-A9 Debug entry register

Bit	Attr	Reset Value	Description
31:0	R	0x00002003	CPU Debug entry register

DAP_ROMENTRY2
Address: DAPROM_BASE + offset(0x0008)
Cortex-A9 ETM entry register

Bit	Attr	Reset Value	Description
31:0	R	0x00003003	CPU ETM entry register

DAP_ROMENTRY3
Address: DAPROM_BASE + offset(0x000c)
Cortex-A9 CTI entry register

Bit	Attr	Reset Value	Description
31:0	R	0x00004003	Cortex-A9 CTI entry register

DAP_ROM_PERIPHID4
Address: DAPROM_BASE + offset(0x0fd0)
Peripheral ID4

Bit	Attr	Reset Value	Description
31:0	R	0x00000004	Peripheral ID4

DAP_ROM_PERIPHID5
Address: DAPROM_BASE + offset(0x0fd4)
Peripheral ID5

Bit	Attr	Reset Value	Description
31:0	R	0x00000000	Peripheral ID5

DAP_ROM_PERIPHID6
Address: DAPROM_BASE + offset(0x0fd8)
Peripheral ID6

Bit	Attr	Reset Value	Description
31:0	R	0x00000000	Peripheral ID6

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DAP_ROM_PERIPHID7
Address: DAPROM_BASE + offset(0x0fdc)
Peripheral ID7

Bit	Attr	Reset Value	Description
31:0	R	0x00000000	Peripheral ID7

DAP_ROM_PERIPHID0
Address: DAPROM_BASE + offset(0x0fe0)
Peripheral ID0

Bit	Attr	Reset Value	Description
31:0	R	0x000000c4	Peripheral ID0

DAP_ROM_PERIPHID1
Address: DAPROM_BASE + offset(0x0fe4)
Peripheral ID1

Bit	Attr	Reset Value	Description
31:0	R	0x000000b4	Peripheral ID1

DAP_ROM_PERIPHID2
Address: DAPROM_BASE + offset(0x0fe8)
Peripheral ID2

Bit	Attr	Reset Value	Description
31:0	R	0x0000006b	Peripheral ID2

DAP_ROM_PERIPHID3
Address: DAPROM_BASE + offset(0x0fec)
Peripheral ID3

Bit	Attr	Reset Value	Description
31:0	R	0x00000020	Peripheral ID3

DAP_ROM_COMPONID0
Address: DAPROM_BASE + offset(0x0ff0)
Component ID0

Bit	Attr	Reset Value	Description
31:0	R	0x0000000d	Component ID0

DAP_ROM_COMPONID1
Address: DAPROM_BASE + offset(0x0ff4)
Component ID1

Bit	Attr	Reset Value	Description
31:0	R	0x00000010	Component ID1

DAP_ROM_COMPONID2
Address: DAPROM_BASE + offset(0x0ff8)
Component ID2

Bit	Attr	Reset Value	Description
31:0	R	0x00000005	Component ID2

DAP_ROM_COMPONID3
Address: DAPROM_BASE + offset(0x0ffc)
Component ID3

Bit	Attr	Reset Value	Description
31:0	R	0x000000b1	Component ID3

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*Notes: Attr: **RW**– Read/writable, **RO**– read only, **WO**– write only, **RWTC-**Readable and write "1" to clear the asserted bit from "1" to "0".*

13.5 Interface description

13.5.1 DAP SWJ-DP interface

The following figure is the DAP SWJ-DP interface, the SWJ-DP is a combined JTAG-DP and SW-DP that enable you connect either a Serial Wire Debug(SWJ) to JTAG probe to a target.

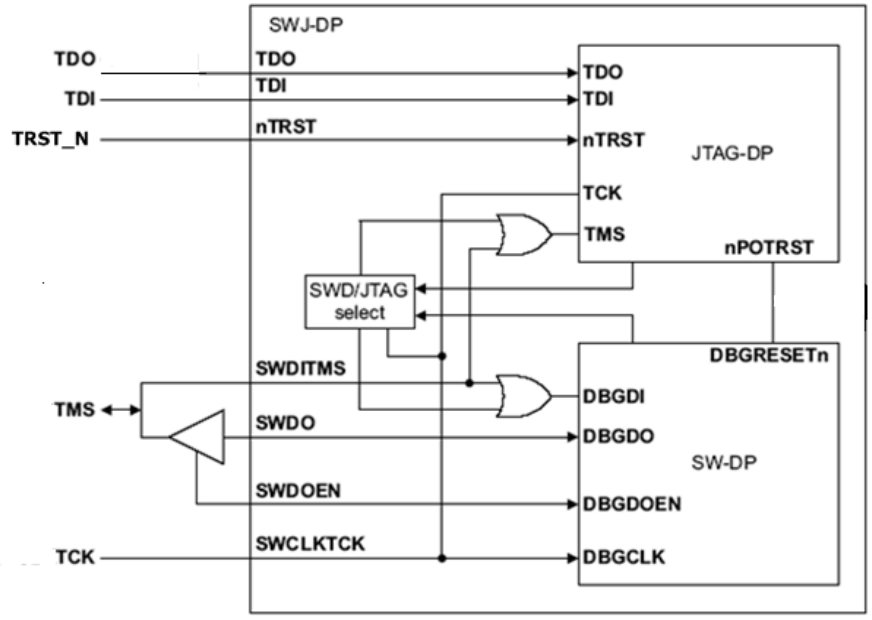


Fig. 13-2 DAP SWJ interface

13.5.2 DAP SW-DP interface

This implementation is taken from ADIv5.1 and operates with a synchronous serial interface. This uses a single bidirectional data signal, and a clock signal.
The figure below describes the interaction between the timing of transactions on the serial wire interface, and the DAP internal bus transfers. It shows when the target responds with a WAIT acknowledgement.

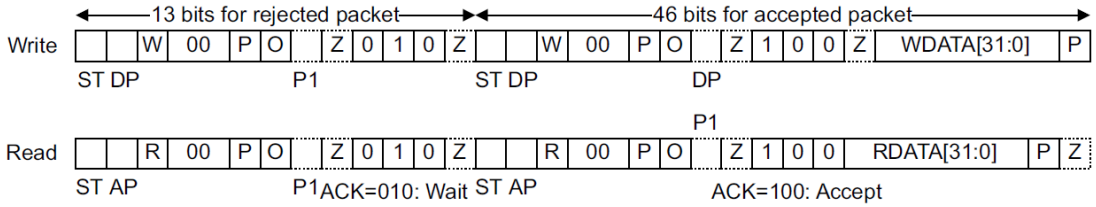


Fig. 13-3 SW-DP acknowledgement timing
Table 13-1 SW-DP Interface Description

Module pin	Direction	Pad name	IOMUX
I2C0 Interface			
jtag_tck	I	IO_MMC0d2_JTAGtck1_GPIO1c4	GRF_GPIO1C_IOMUX[9:8]=2'b10 & sdmmc_detn
jtag_tms	I/O	IO_MMC0d3_JTAGtms1_GPIO1c5	GRF_GPIO1C_IOMUX[11:10]=2'b10 & sdmmc_detn

Note: mmc0_detn, when high, no sd card is used.

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Chapter 14 eFuse

14.1 Overview

EFUSE is a parallel-in/parallel-out Electrical Fuse Macro IP which has 512 bits internal nonvolatile one-time programmable EFUSE storage. With a serial interface, 1-bit can be programmed each time in program mode and 8-bit can be read at one time in read mode. The EFUSE support the following main features:

- One-time programmable nonvolatile EFUSE storage cells organized as 64x8 bit
- 1.1V typical core voltage (DVDD)
- The accumulative total time of 1.21V<AVDD≤2.75V must NOT exceed 1s
- AVDD is NOT allowed to exceed 2.75V, otherwise there will be reliability issue
- Operating junction temperature range of -40℃ to 125℃ (for reading)
- Burning requirements:
  - 2.5V typical burning voltage (AVDD), AVDD must be high during PGM mode. AVDD must be low or floating during READ mode and inactive mode
  - 2us burning pulse width
  - Ambient temperature range of 10~40℃
  - Burning at wafer, package, or field level

14.2 Block Diagram

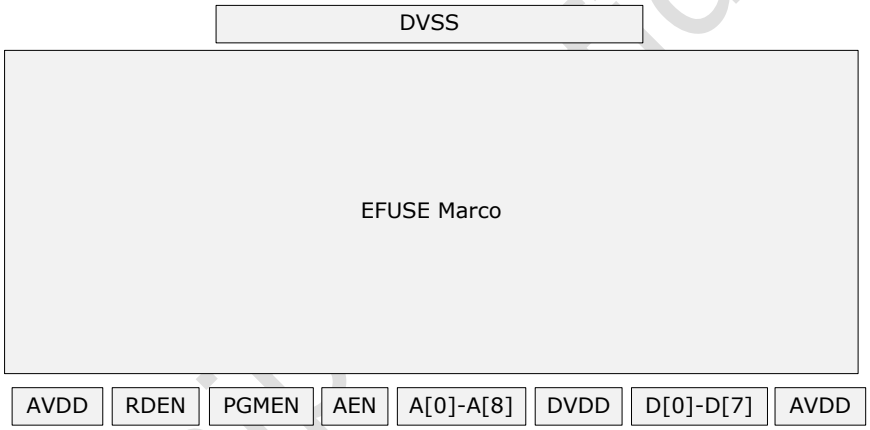


Fig. 14-1 EFUSE Block Diagram

14.3 Function Description

EFUSE has three operation modes:

- Program mode
- Read mode
- Inactive mode

The EFUSE macro enters one of the three modes of operation determine by the logic level of read select signal (RDEN) and program select (PGMEN). See the below table for the corresponding logic levels and operating modes.

Table 14-1 EFUSE operating modes

Mode	PGMEN	RDEN	AVDD	DVDD
PGM mode	H	L	H	H
Read mode	L	H	L or Floating	H
Inactive mode	L	L	L or Floating	H

14.3.1 Program (PGM) Mode

Before burning, initial Fuse output is "0", and written to "1" after burning. When program mode (RDEN=L, PGMEN=H), EFUSE bit specified by address A[8:0] will be burnt by high pulse of AEN. D[7:0] are undefined in PROGRAM mode.

14.3.2 Read Mode

The EFUSE enters read mode if RDEN=H, PGMEN=L. Address signals A[8]~A[6] are invalid.

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Table 14-2 EFUSE Q[0]~Q[7] corresponds with 256 fuse cells

A[5:0]	D[0]	D[1]	D[2]			D[6]	D[7]
000000	Fuse[0]	Fuse[64]	Fuse[64]			Fuse[384]	Fuse[448]
000001	Fuse[1]	Fuse[65]	Fuse[65]			Fuse[385]	Fuse[449]
000010	Fuse[2]	Fuse[66]	Fuse[66]			Fuse[386]	Fuse[450]
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
111111	Fuse[63]	Fuse[127]	Fuse[191]	…	…	Fuse[447]	Fuse[511]

14.3.3 Inactive Mode

The EFUSE enters inactive mode if neither program mode nor read mode is active. The preferred standby conditions in inactive mode are AEN=L, RDEN=L, PGMEN=L. D[7:0] are undefined in inactive mode.

14.4 Register Description

This section describes the control/status registers of the design. Software should read and write these registers using 32-bits accesses.

14.4.1 Registers Summary

Name	Offset	Size	Reset Value	Description
EFUSE_con	0x0000	W	0x00000000	EFUSE control register
EFUSE_data	0x0004	W	0x00000000	EFUSE data out register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

14.4.2 Detail Register Description

EFUSE_con

Address: Operational Base + offset (0x0000)

EFuse control register

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:7	RW	0x00	address address input.
6	RO	0x0	reserved
5	RW	0x0	EFUSE_pd power down enable. active high.
4	RW	0x0	EFUSE_ps high to pass high program voltage to internal for program.
3	RW	0x0	EFUSE_pgenb program enable, low enable.
2	RW	0x0	EFUSE_load high to turn on sense amplifier and load data into latch. Active-High (1.1v) for read mode; when program mode, must be set "low"(0v).
1	RW	0x0	EFUSE_strobe high to trun on the array for read or program access.

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Bit	Attr	Reset Value	Description
0	RW	0x0	EFUSE_csb chip select, low active, to put in low power standby mode.

EFUSE_data
Address: Operational Base + offset (0x0004)
EFUSE data out register

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x00	EFUSE_dout EFUSE data out.

14.5 Timing Diagram

14.5.1 Program(PGM) mode

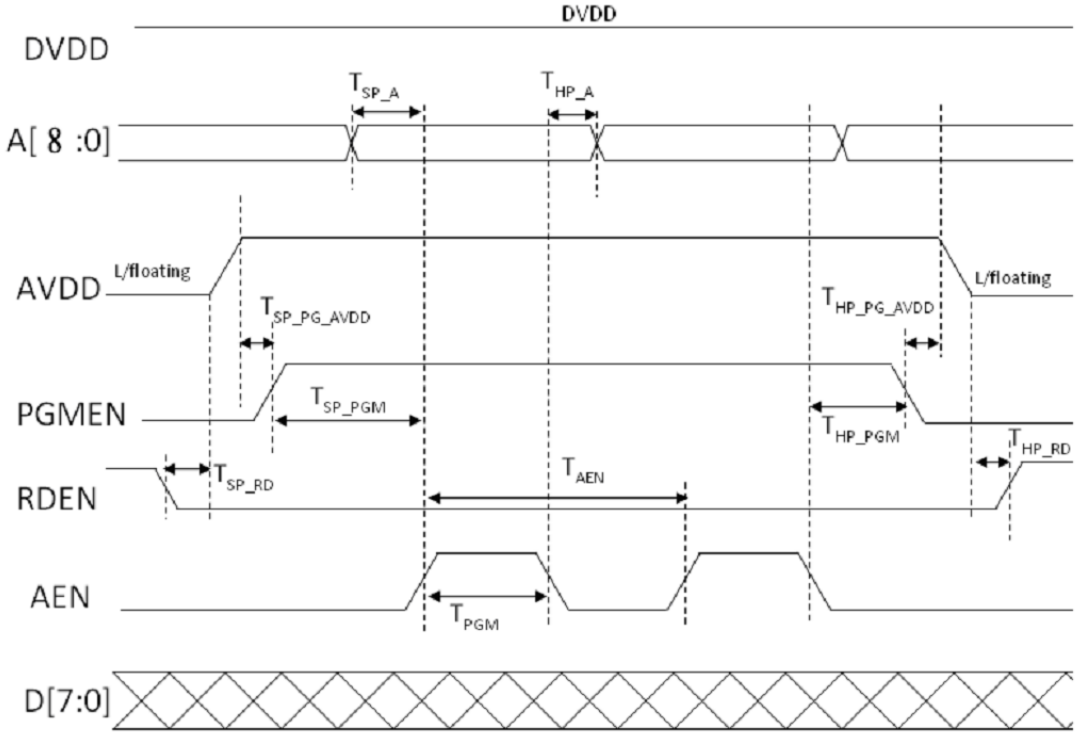


Fig. 14-2 EFUSE timing diagram in program mode

Table 14-3 EFUSE program timing parameters list

Parameter	symbol	value			unit
		min	typ	max	
Burning time	T_{PGM}	2000	2000	10000	ns
Address enable cycle time	T_{AEN}	TPGM+1900			ns
Address to AEN setup time	T_{SP_A}	50			ns
Address hold time from AEN	T_{HP_A}	50			ns
PGMEN signal to AEN setup time	T_{SP_PGM}	100			ns
AEN to PGMEN signal hold time	T_{HP_PGM}	100			ns
RDEN signal to AVDD setup time	T_{SP_RD}	150			ns

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AVDD to RDEN signal hold time	T_{HP_RD}	150			ns
AVDD to PGMEN setup time	$T_{SP_PG_AVDD}$	1000			ns
PGMEN to AVDD hold time	$T_{HP_PG_AVDD}$	1000			ns

Note:

- *The accumulative total time of 1.21V<AVDD≤2.75V must NOT exceed 1s*
- *AVDD is NOT allowed to exceed 2.75V, otherwise there will be reliability issue*
- *Burning time might be changed because of the process later. Please check with RockChip if you have the concern.*
- *When programming the non-secure EFUSE,（GRF_EFUSE_PRG_EN）should be set to 1。*

14.5.2 Read Mode

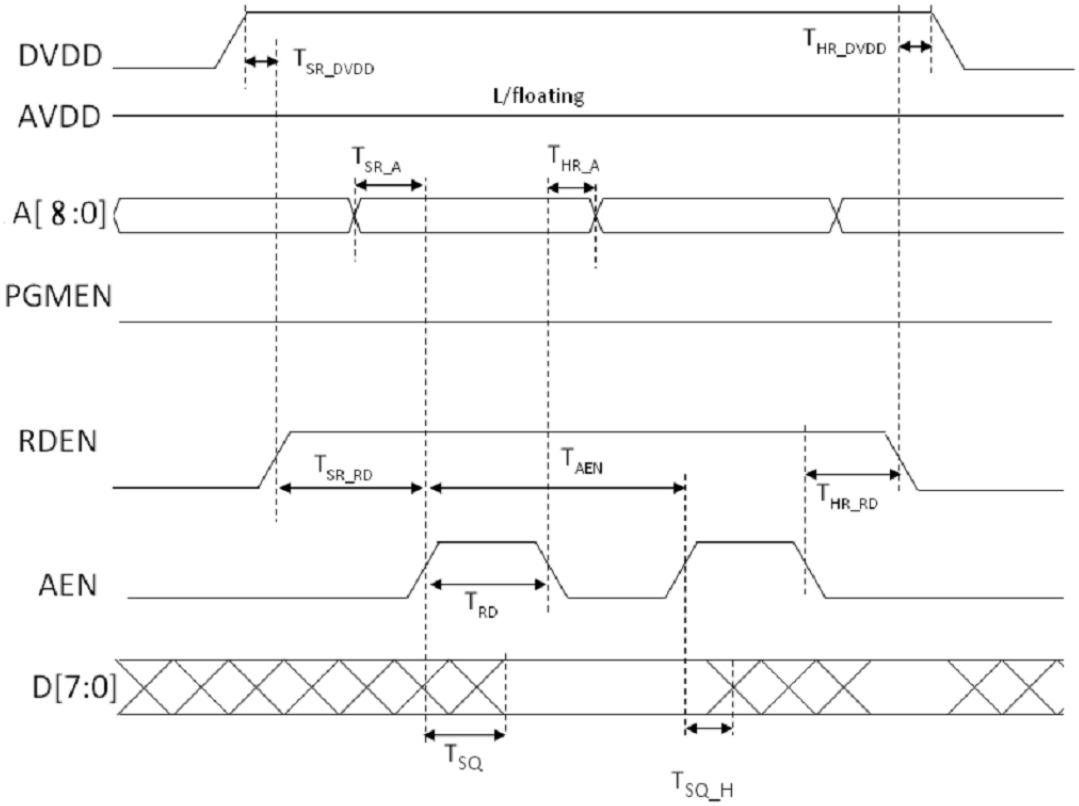


Fig. 14-3 EFUSE timing diagram in read mode

Table 14-4 EFUSE timing parameters list in read mode

Parameter	symbol	value			unit
		min	type	max	
Read time	T_{RD}	40			ns
Address enable cycle time	T_{AEN}	T_{RD}+35			ns
Address to AEN setup time	T_{SP_A}	10			ns
AEN to Address hold time	T_{HR_A}	10			ns
DVDD to RDEN setup time	T_{SR_DVDD}	150			ns
RDEN to DVDD hold time	T_{HR_DVDD}	150			ns
RDEN signal to AEN setup time	T_{SR_RD}	100			ns
Output data steady time with 0 loading	T_{SQ}			45	ns
Output data hold time	T_{SQ_H}	0			ns
AEN to RDEN signal hold time	T_{HR_RD}	100			ns

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14.6 Application Notes

14.6.1 Operating and Burning Conditions

Table 14-5 EFUSE Operating and Burning Conditions

Parameter	Symbol	Values			Unit	Note / Condition
		Min.	Typ.	Max.		
Core voltage (DVDD pin)	*DVDD*	0.99	1.1	1.21	V	–
Burn voltage(AVDD pin)	*AVDD*	2.25	2.5	2.75	V	
Read operating junction temperature	T_{READ}	-40	25	125	℃	–
Burn operating ambient temperature	T_{BURN}	10	25	40	℃	–

14.6.2 Signal Capacitance Requirements

Table 14-6 Signal Capacitance Requirements

Parameter	Symbol	Values			Unit	Note / Condition
		Min	Typ.	Max.		
RDEN Signal Capacitance	C_{RDE}	–	–	1.4	fF	–
PGMEN Signal Capacitance	C_{PGMEN}	-	-	1.4	fF	-
A[12:0] Signal Capacitance	C_D	-	-	3.2	fF	-
AEN Signal Capacitance	C_{AEN}	–	–	1.6	fF	–

14.6.3 Standby and Active Current

Table 14-7 Standby and Active Current Recommendations

Parameter	Symbol	Values			Unit
		Min.	Typ.	Max.	
Standby current	$I_{STANDBY}$	–	1	–	uA
Peak burning current	I_{PROG}	–	15	–	mA
Current during normal reading (10 MHz)	I_{ACTIVE}	–	4	–	mA

14.6.4 Power Supply Sequencing Requirements

At the system/chip level, the following conditions must be guaranteed upon power-up:

- AEN / PGMEN / RDEN signal must be held low until the DVDD and AVDD supplies have reached their minimum values. DVDD should be set up earlier than AVDD. See the following figure. This prevents unintentional burning of the EFUSE macro during power-up.

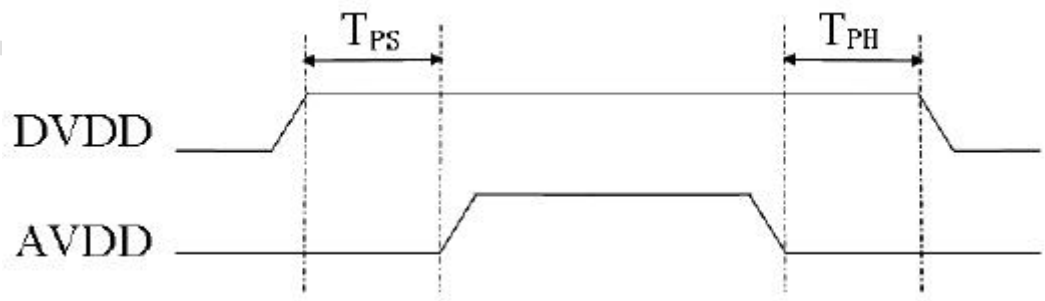


Fig. 14-4 T_{ps}=T_{ph} >= 2 times of T_{AEN} (shown in Table 1-4)

The maximum of the slew rates for the rise of DVDD and AVDD is 5V/us at any time (not average) for this effuse macro only. The minimum of the rise time for DVDD and AVDD is 5us for this EFUSE macro only. Those also needed to meet requirements of ESD, latch up

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and other related IPs' spec.

- Read mode convert to PGM mode directly and PGM mode convert to Read mode directly are not allowed.
- PGM mode convert to inactive mode ,AVDD must change from high to low or floating; inactive mode convert to PGM mode, DVDD must be high before AVDD, the slew rate of AVDD must be less than 5V/us.
- The accumulative total time of 1.21V<AVDD<=2.75V must NOT exceed 1s.
- AVDD is NOT allowed to exceed 2.75V, otherwise there will be reliability issue

14.6.5 Other exceptions and constraints

- PGMEN and RDEN are not allowed to be H at the same time
- AEN high is not allowed except in PGM mode or READ mode
- A port (Address) toggle is not allowed when AEN is high in PGM mode or READ mode
- Neither READ mode transitioning to PGM mode directly nor PGM mode transitioning to READ mode directly is allowed
- For PGM mode converting to inactive mode, AVDD must change from high to low or floating
- All the program timing for each signal must be more than the value defined in the timing table.

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Chapter 15 Watchdog

15.1 Overview

Watchdog Timer (WDT) is an APB slave peripheral that can be used to prevent system lockup that caused by conflicting parts or programs in a SOC. The WDT would generate interrupt or reset signal when its counter reaches zero, then a reset controller would reset the system.

WDT supports the following features:

- 32 bits APB bus width
- WDT counter's clock is pclk
- 32 bits WDT counter width
- Counter counts down from a preset value to 0 to indicate the occurrence of a timeout
- WDT can perform two types of operations when timeout occurs:
  - Generate a system reset
  - First generate an interrupt and if this is not cleared by the service routine by the time a second timeout occurs then generate a system reset
- Programmable reset pulse length
- Total 16 defined-ranges of main timeout period

15.2 Block Diagram

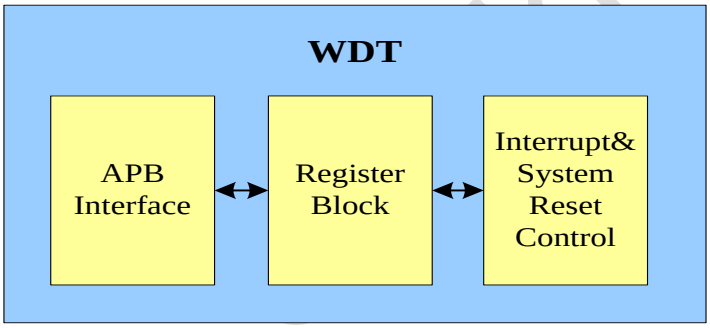


Fig. 15-1 WDT block diagram

- APB Interface

The APB Interface implements the APB slave operation. Its data bus width is 32 bits.

- Register Block

A register block that read coherence for the current count register.

- Interrupt & system reset control

An interrupt/system reset generation block is comprised of a decrementing counter and control logic.

15.3 Function Description

15.3.1 Operation

Counter

The WDT counts from a preset (timeout) value in descending order to zero. When the counter reaches zero, depending on the output response mode selected, either a system reset or an interrupt occurs. When the counter reaches zero, it wraps to the selected timeout value and continues decrementing. The user can restart the counter to its initial value. This is programmed by writing to the restart register at any time. The process of restarting the watchdog counter is sometimes referred as kicking the dog. As a safety feature to prevent accidental restarts, the value 0x76 must be written to the Current Counter Value Register (WDT_CRR).

Interrupts

The WDT can be programmed to generate an interrupt (and then a system reset) when a timeout occurs. When a 1 is written to the response mode field (RMOD, bit 1) of the Watchdog Timer Control Register (WDT_CR), the WDT generates an interrupt. If it is not

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cleared by the time a second timeout occurs, then it generates a system reset. If a restart occurs at the same time the watchdog counter reaches zero, an interrupt is not generated.

System Resets

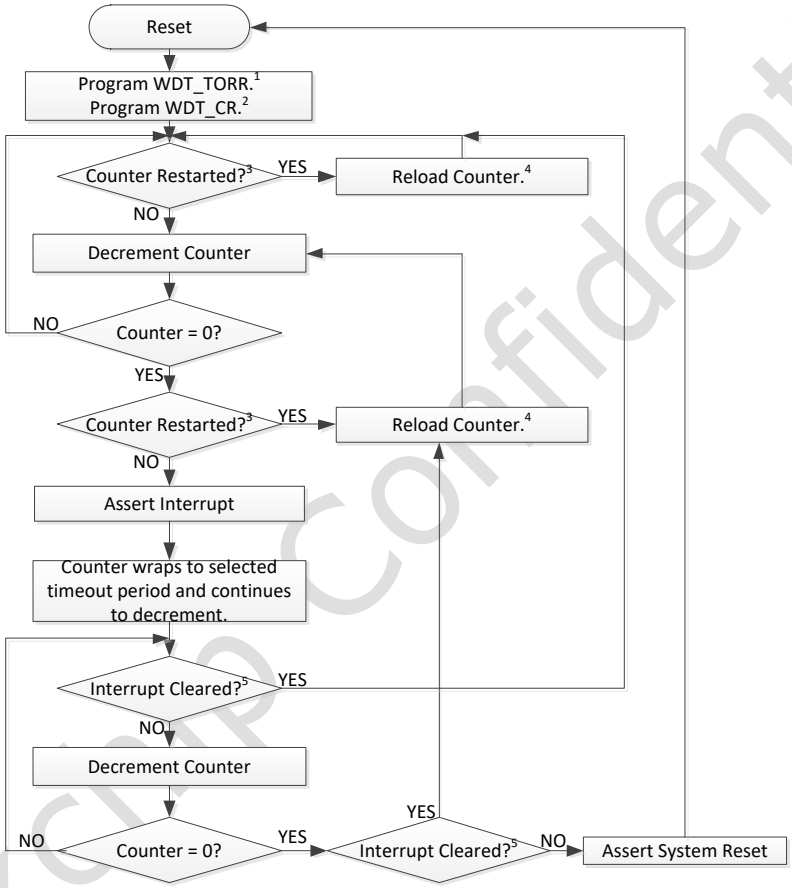
When a 0 is written to the output response mode field (RMOD, bit 1) of the Watchdog Timer Control Register (WDT_CR), the WDT generates a system reset when a timeout occurs.

Reset Pulse Length

The reset pulse length is the number of pclk cycles for which a system reset is asserted. When a system reset is generated, it remains asserted for the number of cycles specified by the reset pulse length or until the system is reset. A counter restart has no effect on the system reset once it has been asserted.

15.3.2 Programming sequence

Operation Flow Chart (Response mode=1)



1. Select required timeout period.
2. Set reset pulse length, response mode, and enable WDT.
3. Write 0x76 to WDT_CRR.
4. Starts back to selected timeout period.
5. Can clear by reading WDT_EOI or restarting (kicking) the counter by writing 0x76 to WDT_CRR.

Fig. 15-2 WDT Operation Flow

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15.4 Register Description

This section describes the control/status registers of the design.

15.4.1 Registers Summary

Name	Offset	Size	Reset Value	Description
WDT_CR	0x0000	W	0x0000000a	Control Register
WDT_TORR	0x0004	W	0x00000000	Timeout range Register
WDT_CCVR	0x0008	W	0x00000000	Current counter value Register
WDT_CRR	0x000c	W	0x00000000	Counter restart Register
WDT_STAT	0x0010	W	0x00000000	Interrupt status Register
WDT_EOI	0x0014	W	0x00000000	Interrupt clear Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

15.4.2 Detail Register Description

WDT_CR

Address: Operational Base + offset (0x0000)

Control Register

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4:2	RW	0x2	rst_pluse_lenth Reset pulse length. This is used to select the number of pclk cycles for which the system reset stays asserted. 3'b000: 2 pclk cycles 3'b001: 4 pclk cycles 3'b010: 8 pclk cycles 3'b011: 16 pclk cycles 3'b100: 32 pclk cycles 3'b101: 64 pclk cycles 3'b110: 128 pclk cycles 3'b111: 256 pclk cycles
1	RW	0x1	resp_mode Response mode. Selects the output response generated to a timeout. 1'b0: Generate a system reset. 1'b1: First generate an interrupt and if it is not cleared by the time a second timeout occurs then generate a system reset.
0	RW	0x0	wdt_en 1'b0: WDT disabled 1'b1: WDT enabled Writable when the configuration parameter WDT_ALWAYS_EN=0, otherwise, it is readable. This bit is used to enable and disable the watchdog. When disabled, the counter dose not decrement .Thus, no interrupt or system reset is generated. Once this bit has been enabled, it can be cleared only by a system reset.

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WDT_TORR
Address: Operational Base + offset (0x0004)
Timeout range Register

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3:0	RW	0x0	timeout_period Timeout period. This field is used to select the timeout period from which the watchdog counter restarts. A change of the timeout period takes effect only after the next counter restart (kick). The range of values available for a 32-bit watchdog counter are: 4'b0000: 0x0000ffff 4'b0001: 0x0001ffff 4'b0010: 0x0003ffff 4'b0011: 0x0007ffff 4'b0100: 0x000fffff 4'b0101: 0x001fffff 4'b0110: 0x003fffff 4'b0111: 0x007fffff 4'b1000: 0x00ffffff 4'b1001: 0x01ffffff 4'b1010: 0x03ffffff 4'b1011: 0x07ffffff 4'b1100: 0x0fffffff 4'b1101: 0x1fffffff 4'b1110: 0x3fffffff 4'b1111: 0x7fffffff

WDT_CCVR
Address: Operational Base + offset (0x0008)
Current counter value Register

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	cur_cnt Current counter value This register, when read, is the current value of the internal counter. This value is read coherently whenever it is read

WDT_CRR
Address: Operational Base + offset (0x000c)
Counter restart Register

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
7:0	W1C	0x00	cnt_restart Counter restart This register is used to restart the WDT counter. As a safety feature to prevent accidental restarts, the value 0x76 must be written. A restart also clears the WDT interrupt. Reading this register returns zero.

WDT_STAT
Address: Operational Base + offset (0x0010)
Interrupt status Register

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RO	0x0	wdt_status This register shows the interrupt status of the WDT. 1'b1: Interrupt is active regardless of polarity; 1'b0: Interrupt is inactive.

WDT_EOI
Address: Operational Base + offset (0x0014)
Interrupt clear Register

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RC	0x0	wdt_int_clr Clears the watchdog interrupt. This can be used to clear the interrupt without restarting the watchdog counter.

15.5 Application Notes

Please refer to the "Function Description" section.

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Chapter 16 Pulse Width Modulation (PWM)

16.1 Overview

The pulse-width modulator (PWM) feature is very common in embedded systems. It provides a way to generate a pulse periodic waveform for motor control or can act as a digital-to-analog converter with some external components.
The PWM Module supports the following features:

- 4-built-in PWM channels (i.e., PWM_CHNx: x=0,1,2,3)
- Configurable to operate in capture mode
  - Measures the high/low polarity effective cycles of this input waveform
  - Generates a single interrupt at the transition of input waveform polarity
  - 32-bit high polarity capture register
  - 32-bit low polarity capture register
  - 32-bit current value register
- Configurable to operate in continuous mode or one-shot mode
  - 32-bit period counter
  - 32-bit duty register
  - 32-bit current value register
  - Configurable PWM output polarity in inactive state and duty period pulse polarity
  - Period and duty cycle are shadow buffered. Change takes effect when the end of the effective period is reached or when the channel is disabled
  - Programmable center or left aligned outputs, and change takes effect when the end of the effective period is reached or when the channel is disabled
  - 8-bit repeat counter for one-shot operation. One-shot operation will produce N + 1 periods of the waveform, where N is the repeat counter value, and generates a single interrupt at the end of operation
  - Continuous mode generates the waveform continuously, and does not generates any interrupts
- pre-scaled operation to bus clock and then further scaled
- Available low-power mode to reduce power consumption when the channel is inactive.

16.2 Block Diagram

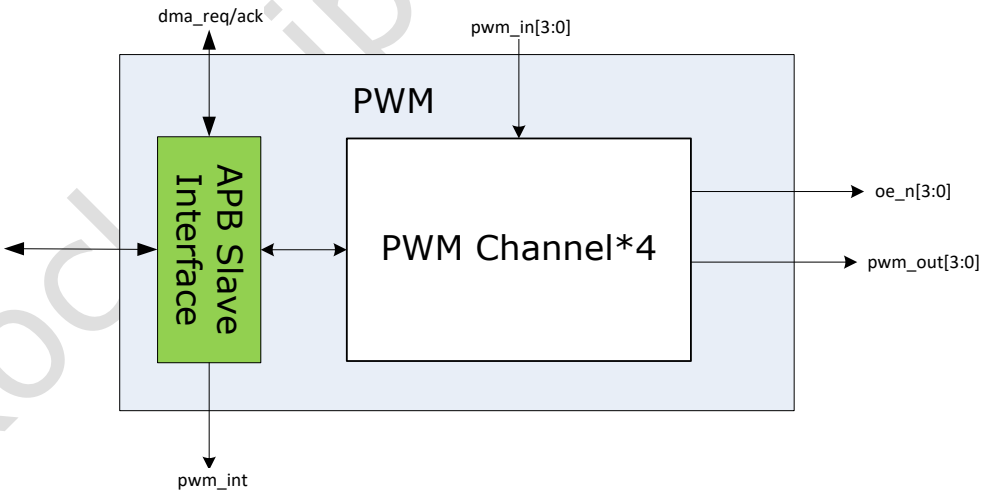


Fig. 16-1 PWM Block Diagram

The host processor gets access to PWM Register Block through the APB slave interface with 32-bit bus width, and asserts the active-high level interrupt. PWM only supports one interrupt output, please refer to interrupt register to know the raw interrupt status when an interrupt is asserted.
PWM Channel is the control logic of PWM module, and controls the operation of PWM module according to the configured working mode.

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16.3 Function Description

The PWM support three operation modes: capture mode, one-shot mode and continuous mode. For the one-shot mode and the continuous mode, the PWM output can be configured as the left-aligned mode or the center-aligned mode.

16.3.1 Capture mode

The capture mode is used to measure the PWM channel input waveform high/low effective cycles with the PWM channel clock, and asserts an interrupt when the polarity of the input waveform changes. The number of the high effective cycles is recorded in the PWM_CHNx_PERIOD_HPC register, while the number of the low effective cycles is recorded in the PWM_CHNx_DUTY_LPC register.

Notes: the PWM input waveform is doubled buffered when the PWM channel is working in order to filter unexpected shot-time polarity transition, and therefore the interrupt is asserted several cycles after the input waveform polarity changes, and so does the change of the values of PWM_CHNx_PERIOD_HPC and PWM_CHNx_DUTY_LPC.

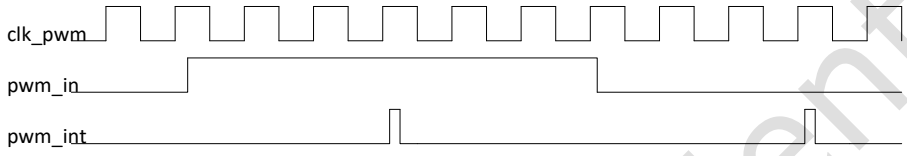


Fig. 16-2 PWM Capture Mode

16.3.2 Continuous mode

The PWM channel generates a series of the pulses continuously as expected once the channel is enabled with continuous mode.

In the continuous mode, the PWM output waveforms can be in one form of the two output mode: left-aligned mode or center-aligned mode.

For the left-aligned output mode, the PWM channel firstly starts the duty cycle with the configured duty polarity (PWM_CHNx_CTRL.duty_pol). Once duty cycle number (PWM_CHNx_DUTY_LPC) is reached, the output is switched to the opposite polarity. After the period number (PWM_CHNx_PERIOD_HPC) is reached, the output is again switched to the opposite polarity to start another period of desired pulse.

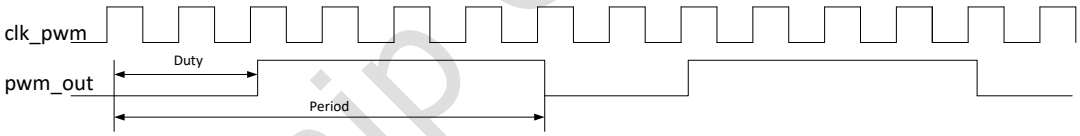


Fig. 16-3 PWM Continuous Left-aligned Output Mode

For the center-aligned output mode, the PWM channel firstly starts the duty cycle with the configured duty polarity (PWM_CHNx_CTRL.duty_pol). Once one half of duty cycle number (PWM_CHNx_DUTY_LPC) is reached, the output is switched to the opposite polarity. Then if there is one half of duty cycle left for the whole period, the output is again switched to the opposite polarity. Finally after the period number (PWM_CHNx_PERIOD_HPC) is reached, the output starts another period of desired pulse.

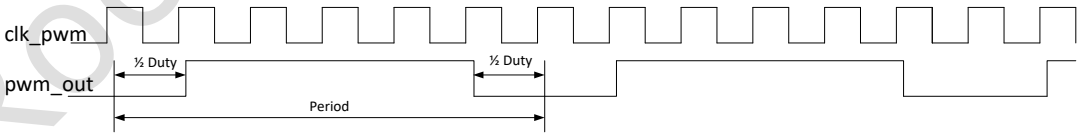


Fig. 16-4 PWM Continuous Center-aligned Output Mode

Once disable the PWM channel, the channel stops generating the output waveforms and output polarity is fixed as the configured inactive polarity (PWM_CHNx_CTRL.inactive_pol).

16.3.3 One-shot mode

Unlike the continuous mode, the PWM channel generates the output waveforms within the configured periods (PWM_CHNx_CTRL.rpt + 1), and then stops. At the same times, an interrupt is asserted to inform that the operation has been finished.

There are also two output modes for the one-shot mode: the left-aligned mode and the center-aligned mode.

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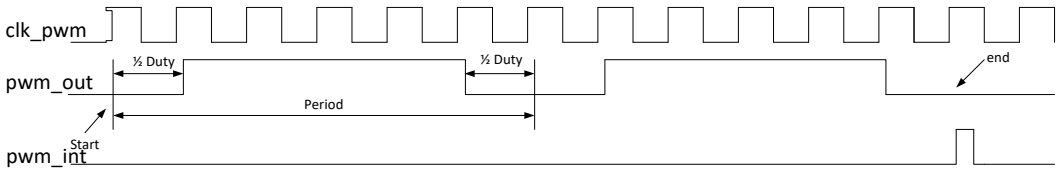


Fig. 16-5 PWM One-shot Center-aligned Output Mode

16.4 Register Description

16.4.1 Registers Summary

Name	Offset	Size	Reset Value	Description
PWM_CHN0_CNT	0x0000	W	0x00000000	PWM Channel 0 Counter Register
PWM_CHN0_PERIOD_HPR	0x0004	W	0x00000000	PWM Channel 0 Period Register/High Polarity Capture Register
PWM_CHN0_DUTY_LPR	0x0008	W	0x00000000	PWM Channel 0 Duty Register/Low Polarity Capture Register
PWM_CHN0_CTRL	0x000c	W	0x00000000	PWM Channel 0 Control Register
PWM_CHN1_CNT	0x0010	W	0x00000000	PWM Channel 1 Counter Register
PWM_CHN1_PERIOD_HPR	0x0014	W	0x00000000	PWM Channel 1 Period Register/High Polarity Capture Register
PWM_CHN1_DUTY_LPR	0x0018	W	0x00000000	PWM Channel 1 Duty Register/Low Polarity Capture Register
PWM_CHN1_CTRL	0x001c	W	0x00000000	PWM Channel 1 Control Register
PWM_CHN2_CNT	0x0020	W	0x00000000	PWM Channel 2 Counter Register
PWM_CHN2_PERIOD_HPR	0x0024	W	0x00000000	PWM Channel 2 Period Register/High Polarity Capture Register
PWM_CHN2_DUTY_LPR	0x0028	W	0x00000000	PWM Channel 2 Duty Register/Low Polarity Capture Register
PWM_CHN2_CTRL	0x002c	W	0x00000000	PWM Channel 2 Control Register
PWM_CHN3_CNT	0x0030	W	0x00000000	PWM Channel 3 Counter Register
PWM_CHN3_PERIOD_HPR	0x0034	W	0x00000000	PWM Channel 3 Period Register/High Polarity Capture Register
PWM_CHN3_DUTY_LPR	0x0038	W	0x00000000	PWM Channel 3 Duty Register/Low Polarity Capture Register
PWM_CHN3_CTRL	0x003c	W	0x00000000	PWM Channel 3 Control Register
PWM_INTSTS	0x0040	W	0x00000000	Interrupt Status Register
PWM_INT_EN	0x0044	W	0x00000000	Interrupt Enable Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

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16.4.2 Detail Register Description

PWM_CHN0_CNT

Address: Operational Base + offset (0x0000)

PWM Channel 0 Counter Register

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	CNT Timer Counter The 32-bit indicates current value of PWM Channel 0 counter. The counter runs at the rate of PWM clock. The value ranges from 0 to (2^32-1).

PWM_CHN0_PERIOD_HPR

Address: Operational Base + offset (0x0004)

PWM Channel 0 Period Register/High Polarity Capture Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PERIOD_HPR Output Waveform Period/Input Waveform High Polarity Cycle If PWM is operated at the continuous mode or one-shot mode, this value defines the period of the output waveform. Note that, if the PWM is operated at the center-aligned mode, the period should be an even one, and therefore only the bit [31:1] is taken into account and bit [0] always considered as 0. If PWM is operated at the capture mode, this value indicates the effective high polarity cycles of input waveform. This value is based on the PWM clock. The value ranges from 0 to (2^32-1).

PWM_CHN0_DUTY_LPR

Address: Operational Base + offset (0x0008)

PWM Channel 0 Duty Register/Low Polarity Capture Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	DUTY_LPR Output Waveform Duty Cycle/Input Waveform Low Polarity Cycle If PWM is operated at the continuous mode or one-shot mode, this value defines the duty cycle of the output waveform. The PWM starts the output waveform with duty cycle. Note that, if the PWM is operated at the center-aligned mode, the period should be an even one, and therefore only the [31:1] is taken into account. If PWM is operated at the capture mode, this value indicates the effective low polarity cycles of input waveform. This value is based on the PWM clock. The value ranges from 0 to (2^32-1).

PWM_CHN0_CTRL

Address: Operational Base + offset (0x000c)

PWM Channel 0 Control Register

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Bit	Attr	Reset Value	Description
31:24	RW	0x00	rpt Repeat Counter This field defines the repeated effective periods of output waveform in one-shot mode. The value N means N+1 repeated effective periods.
23:16	RW	0x00	scale Scale Factor This field defines the scale factor applied to prescaled clock. The value N means the clock is divided by 2*N. If N is 0, it means that the clock is divided by 512(2*256).
15	RO	0x0	reserved
14:12	RW	0x0	prescale Prescale Factor This field defines the prescale factor applied to input clock. The value N means that the input clock is divided by 2^N.
11:10	RO	0x0	reserved
9	RW	0x0	clk_sel Clock Source Select 0: non-scaled clock is selected as PWM clock source. It means that the prescale clock is directly used as the PWM clock source 1: scaled clock is selected as PWM clock source
8	RW	0x0	lp_en Low Power Mode Enable 0: disabled 1: enabled When PWM channel is inactive state and Low Power Mode is enabled, the path to PWM Clock prescale module is blocked to reduce power consumption.
7:6	RO	0x0	reserved
5	RW	0x0	output_mode PWM Output mode 0: left aligned mode 1: center aligned mode
4	RW	0x0	inactive_pol Inactive State Output Polarity This defines the output waveform polarity when PWM channel is in inactive state. The inactive state means that PWM finishes the complete waveform in one-shot mode or PWM channel is disabled. 0: negative 1: positive

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Bit	Attr	Reset Value	Description
3	RW	0x0	duty_pol Duty Cycle Output Polarity This defines the polarity for duty cycle. PWM starts the output waveform with duty cycle. 0: negative 1: positive
2:1	RW	0x0	pwm_mode PWM Operation Mode 00: One shot mode. PWM produces the waveform within the repeated times defined by PWM_CHN0_CTRL.rpt. 01: Continuous mode. PWM produces the waveform continuously 10: Capture mode. PWM measures the cycles of high/low polarity of input waveform. 11: reserved
0	RW	0x0	pwm_en PWM channel enable 0: disabled 1: enabled. If the PWM is worked in the one-shot mode, this bit will be cleared at the end of operation

PWM_CHN1_CNT
Address: Operational Base + offset (0x0010)
PWM Channel 1 Counter Register

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	CNT Timer Counter The 32-bit indicates current value of PWM Channel 1 counter. The counter runs at the rate of PWM clock. The value ranges from 0 to (2^32-1).

PWM_CHN1_PERIOD_HPR
Address: Operational Base + offset (0x0014)
PWM Channel 1 Period Register/High Polarity Capture Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PERIOD_HPR Output Waveform Period/Input Waveform High Polarity Cycle If PWM is operated at the continuous mode or one-shot mode, this value defines the period of the output waveform. Note that, if the PWM is operated at the center-aligned mode, the period should be an even one, and therefore only the bit [31:1] is taken into account and bit [0] always considered as 0. If PWM is operated at the capture mode, this value indicates the effective high polarity cycles of input waveform. This value is based on the PWM clock. The value ranges from 0 to (2^32-1).

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PWM_CHN1_DUTY_LPR
Address: Operational Base + offset (0x0018)
PWM Channel 1 Duty Register/Low Polarity Capture Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	DUTY_LPR Output Waveform Duty Cycle/Input Waveform Low Polarity Cycle If PWM is operated at the continuous mode or one-shot mode, this value defines the duty cycle of the output waveform. The PWM starts the output waveform with duty cycle. Note that, if the PWM is operated at the center-aligned mode, the period should be an even one, and therefore only the [31:1] is taken into account. If PWM is operated at the capture mode, this value indicates the effective low polarity cycles of input waveform. This value is based on the PWM clock. The value ranges from 0 to (2^32-1).

PWM_CHN1_CTRL
Address: Operational Base + offset (0x001c)
PWM Channel 1 Control Register

Bit	Attr	Reset Value	Description
31:24	RW	0x00	rpt Repeat Counter This field defines the repeated effective periods of output waveform in one-shot mode. The value N means N+1 repeated effective periods.
23:16	RW	0x00	scale Scale Factor This field defines the scale factor applied to prescaled clock. The value N means the clock is divided by 2*N. If N is 0, it means that the clock is divided by 512(2*256).
15	RO	0x0	reserved
14:12	RW	0x0	prescale Prescale Factor This field defines the prescale factor applied to input clock. The value N means that the input clock is divided by 2^N.
11:10	RO	0x0	reserved
9	RW	0x0	clk_sel Clock Source Select 0: non-scaled clock is selected as PWM clock source. It means that the prescale clock is directly used as the PWM clock source 1: scaled clock is selected as PWM clock source

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Bit	Attr	Reset Value	Description
8	RW	0x0	lp_en Low Power Mode Enable 0: disabled 1: enabled When PWM channel is inactive state and Low Power Mode is enabled, the path to PWM Clock prescale module is blocked to reduce power consumption.
7:6	RO	0x0	reserved
5	RW	0x0	output_mode PWM Output mode 0: left aligned mode 1: center aligned mode
4	RW	0x0	inactive_pol Inactive State Output Polarity This defines the output waveform polarity when PWM channel is in inactive state. The inactive state means that PWM finishes the complete waveform in one-shot mode or PWM channel is disabled. 0: negative 1: positive
3	RW	0x0	duty_pol Duty Cycle Output Polarity This defines the polarity for duty cycle. PWM starts the output waveform with duty cycle. 0: negative 1: positive
2:1	RW	0x0	pwm_mode PWM Operation Mode 00: One shot mode. PWM produces the waveform within the repeated times defined by PWM_CHN1_CTRL.rpt 01: Continuous mode. PWM produces the waveform continuously 10: Capture mode. PWM measures the cycles of high/low polarity of input waveform. 11: reserved
0	RW	0x0	pwm_en PWM channel enable 0: disabled 1: enabled. If the PWM is worked in the one-shot mode, this bit will be cleared at the end of operation

PWM_CHN2_CNT
Address: Operational Base + offset (0x0020)
PWM Channel 2 Counter Register

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	CNT Timer Counter The 32-bit indicates current value of PWM Channel 2 counter. The counter runs at the rate of PWM clock. The value ranges from 0 to (2^32-1).

PWM_CHN2_PERIOD_HPR
Address: Operational Base + offset (0x0024)
PWM Channel 2 Period Register/High Polarity Capture Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PERIOD_HPR Output Waveform Period/Input Waveform High Polarity Cycle If PWM is operated at the continuous mode or one-shot mode, this value defines the period of the output waveform. Note that, if the PWM is operated at the center-aligned mode, the period should be an even one, and therefore only the bit [31:1] is taken into account and bit [0] always considered as 0. If PWM is operated at the capture mode, this value indicates the effective high polarity cycles of input waveform. This value is based on the PWM clock. The value ranges from 0 to (2^32-1).

PWM_CHN2_DUTY_LPR
Address: Operational Base + offset (0x0028)
PWM Channel 2 Duty Register/Low Polarity Capture Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	DUTY_LPR Output Waveform Duty Cycle/Input Waveform Low Polarity Cycle If PWM is operated at the continuous mode or one-shot mode, this value defines the duty cycle of the output waveform. The PWM starts the output waveform with duty cycle. Note that, if the PWM is operated at the center-aligned mode, the period should be an even one, and therefore only the [31:1] is taken into account. If PWM is operated at the capture mode, this value indicates the effective low polarity cycles of input waveform. This value is based on the PWM clock. The value ranges from 0 to (2^32-1).

PWM_CHN2_CTRL
Address: Operational Base + offset (0x002c)
PWM Channel 2 Control Register

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Bit	Attr	Reset Value	Description
31:24	RW	0x00	rpt Repeat Counter This field defines the repeated effective periods of output waveform in one-shot mode. The value N means N+1 repeated effective periods.
23:16	RW	0x00	scale Scale Factor This field defines the scale factor applied to prescaled clock. The value N means the clock is divided by 2*N. If N is 0, it means that the clock is divided by 512(2*256).
15	RO	0x0	reserved
14:12	RW	0x0	prescale Prescale Factor This field defines the prescale factor applied to input clock. The value N means that the input clock is divided by 2^N.
11:10	RO	0x0	reserved
9	RW	0x0	clk_sel Clock Source Select 0: non-scaled clock is selected as PWM clock source. It means that the prescale clock is directly used as the PWM clock source 1: scaled clock is selected as PWM clock source
8	RW	0x0	lp_en Low Power Mode Enable 0: disabled 1: enabled When PWM channel is inactive state and Low Power Mode is enabled, the path to PWM Clock prescale module is blocked to reduce power consumption.
7:6	RO	0x0	reserved
5	RW	0x0	output_mode PWM Output mode 0: left aligned mode 1: center aligned mode
4	RW	0x0	inactive_pol Inactive State Output Polarity This defines the output waveform polarity when PWM channel is in inactive state. The inactive state means that PWM finishes the complete waveform in one-shot mode or PWM channel is disabled. 0: negative 1: positive

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Bit	Attr	Reset Value	Description
3	RW	0x0	duty_pol Duty Cycle Output Polarity This defines the polarity for duty cycle. PWM starts the output waveform with duty cycle. 0: negative 1: positive
2:1	RW	0x0	pwm_mode PWM Operation Mode 00: One shot mode. PWM produces the waveform within the repeated times defined by PWM_CHN2_CTRL.rpt. 01: Continuous mode. PWM produces the waveform continuously 10: Capture mode. PWM measures the cycles of high/low polarity of input waveform. 11: reserved
0	RW	0x0	pwm_en PWM channel enable 0: disabled 1: enabled. If the PWM is worked in the one-shot mode, this bit will be cleared at the end of operation

PWM_CHN3_CNT
Address: Operational Base + offset (0x0030)
PWM Channel 3 Counter Register

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	CNT Timer Counter The 32-bit indicates current value of PWM Channel 3 counter. The counter runs at the rate of PWM clock. The value ranges from 0 to (2^32-1).

PWM_CHN3_PERIOD_HPR
Address: Operational Base + offset (0x0034)
PWM Channel 3 Period Register/High Polarity Capture Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PERIOD_HPR Output Waveform Period/Input Waveform High Polarity Cycle If PWM is operated at the continuous mode or one-shot mode, this value defines the period of the output waveform. Note that, if the PWM is operated at the center-aligned mode, the period should be an even one, and therefore only the bit [31:1] is taken into account and bit [0] always considered as 0. If PWM is operated at the capture mode, this value indicates the effective high polarity cycles of input waveform. This value is based on the PWM clock. The value ranges from 0 to (2^32-1).

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PWM_CHN3_DUTY_LPR
Address: Operational Base + offset (0x0038)
PWM Channel 3 Duty Register/Low Polarity Capture Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	DUTY_LPR Output Waveform Duty Cycle/Input Waveform Low Polarity Cycle If PWM is operated at the continuous mode or one-shot mode, this value defines the duty cycle of the output waveform. The PWM starts the output waveform with duty cycle. Note that, if the PWM is operated at the center-aligned mode, the period should be an even one, and therefore only the [31:1] is taken into account. If PWM is operated at the capture mode, this value indicates the effective low polarity cycles of input waveform. This value is based on the PWM clock. The value ranges from 0 to (2^32-1).

PWM_CHN3_CTRL
Address: Operational Base + offset (0x003c)
PWM Channel 3 Control Register

Bit	Attr	Reset Value	Description
31:24	RW	0x00	rpt Repeat Counter This field defines the repeated effective periods of output waveform in one-shot mode. The value N means N+1 repeated effective periods.
23:16	RW	0x00	scale Scale Factor This field defines the scale factor applied to prescaled clock. The value N means the clock is divided by 2*N. If N is 0, it means that the clock is divided by 512(2*256).
15	RO	0x0	reserved
14:12	RW	0x0	prescale Prescale Factor This field defines the prescale factor applied to input clock. The value N means that the input clock is divided by 2^N.
11:10	RO	0x0	reserved
9	RW	0x0	clk_sel Clock Source Select 0: non-scaled clock is selected as PWM clock source. It means that the prescale clock is directly used as the PWM clock source 1: scaled clock is selected as PWM clock source

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Bit	Attr	Reset Value	Description
8	RW	0x0	lp_en Low Power Mode Enable 0: disabled 1: enabled When PWM channel is inactive state and Low Power Mode is enabled, the path to PWM Clock prescale module is blocked to reduce power consumption.
7:6	RO	0x0	reserved
5	RW	0x0	output_mode PWM Output mode 0: left aligned mode 1: center aligned mode
4	RW	0x0	inactive_pol Inactive State Output Polarity This defines the output waveform polarity when PWM channel is in inactive state. The inactive state means that PWM finishes the complete waveform in one-shot mode or PWM channel is disabled. 0: negative 1: positive
3	RW	0x0	duty_pol Duty Cycle Output Polarity This defines the polarity for duty cycle. PWM starts the output waveform with duty cycle. 0: negative 1: positive
2:1	RW	0x0	pwm_mode PWM Operation Mode 00: One shot mode. PWM produces the waveform within the repeated times defined by PWM_CHN3_CTRL.rpt 01: Continuous mode. PWM produces the waveform continuously 10: Capture mode. PWM measures the cycles of high/low polarity of input waveform. 11: reserved
0	RW	0x0	pwm_en PWM channel enable 0: disabled 1: enabled. If the PWM is worked in the one-shot mode, this bit will be cleared at the end of operation

PWM_INTSTS

Address: Operational Base + offset (0x0040)

Interrupt Status Register

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
11	RO	0x0	CH3_Pol Channel 3 Interrupt Polarity Flag This bit is used in capture mode in order to identify the transition of the input waveform when interrupt is generated. When bit is 1, please refer to PWM_CHN3_PERIOD_HPR to know the effective high cycle of Channel 3 input waveform. Otherwise, please refer to PWM_CHN3_PERIOD_LPR to know the effective low cycle of Channel 3 input waveform. Write 1 to CH3_IntSts will clear this bit.
10	RO	0x0	CH2_Pol Channel 2 Interrupt Polarity Flag This bit is used in capture mode in order to identify the transition of the input waveform when interrupt is generated. When bit is 1, please refer to PWM_CHN2_PERIOD_HPR to know the effective high cycle of Channel 2 input waveform. Otherwise, please refer to PWM_CHN2_PERIOD_LPR to know the effective low cycle of Channel 2 input waveform. Write 1 to CH2_IntSts will clear this bit.
9	RO	0x0	CH1_Pol Channel 1 Interrupt Polarity Flag This bit is used in capture mode in order to identify the transition of the input waveform when interrupt is generated. When bit is 1, please refer to PWM_CHN1_PERIOD_HPR to know the effective high cycle of Channel 1 input waveform. Otherwise, please refer to PWM_CHN1_PERIOD_LPR to know the effective low cycle of Channel 1 input waveform. Write 1 to CH1_IntSts will clear this bit.
8	RO	0x0	CH0_Pol Channel 0 Interrupt Polarity Flag This bit is used in capture mode in order to identify the transition of the input waveform when interrupt is generated. When bit is 1, please refer to PWM_CHN0_PERIOD_HPR to know the effective high cycle of Channel 0 input waveform. Otherwise, please refer to PWM_CHN0_PERIOD_LPR to know the effective low cycle of Channel 0 input waveform. Write 1 to CH0_IntSts will clear this bit.
7:4	RO	0x0	reserved
3	RW	0x0	CH3_IntSts Channel 3 Interrupt Status 0: Channel 3 Interrupt not generated 1: Channel 3 Interrupt generated
2	RW	0x0	CH2_IntSts Channel 2 Interrupt Status 0: Channel 2 Interrupt not generated 1: Channel 2 Interrupt generated

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Bit	Attr	Reset Value	Description
1	RW	0x0	CH1_IntSts Channel 1 Interrupt Status 0: Channel 1 Interrupt not generated 1: Channel 1 Interrupt generated
0	RW	0x0	CH0_IntSts Channel 0 Raw Interrupt Status 0: Channel 0 Interrupt not generated 1: Channel 0 Interrupt generated

PWM_INT_EN
Address: Operational Base + offset (0x0044)
Interrupt Enable Register

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3	RW	0x0	CH3_Int_en Channel 3 Interrupt Enable 0: Channel 3 Interrupt disabled 1: Channel 3 Interrupt enabled
2	RW	0x0	CH2_Int_en Channel 2 Interrupt Enable 0: Channel 2 Interrupt disabled 1: Channel 2 Interrupt enabled
1	RW	0x0	CH1_Int_en Channel 1 Interrupt Enable 0: Channel 1 Interrupt disabled 1: Channel 1 Interrupt enabled
0	RW	0x0	CH0_Int_en Channel 0 Interrupt Enable 0: Channel 0 Interrupt disabled 1: Channel 0 Interrupt enabled

16.5 Interface Description

Table 16-1 PWM Interface Description

Module Pin	Direction	Pad Name	IOMUX Setting
PWM0	I/O	IO_PWM0_GPIO0d2	GRF_GPIO0D_IOMUX[4]=1'b1
PWM1	I/O	IO_PWM1_GPIO0d3	GRF_GPIO0D_IOMUX[6]=1'b1
PWM2	I/O	IO_PWM2_GPIO0d4	GRF_GPIO0D_IOMUX[8]=1'b1
PWM3	I/O	IO_PWMirin_GPIO3d2	GRF_GPIO3D_IOMUX[4]=1'b1

Notes: I=input, O=output, I/O=input/output.

16.6 Application Notes

16.6.1 PWM Capture Mode Standard Usage Flow

1. Set PWM_CHNx_CTRL.pwm_en to '0' to disable the PWM channel.
2. Choose the prescale factor and the scale factor for pclk by programming

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PWM_CHNx_CTRL.prescale and PWM_CHNx_CTRL.scale, and select the clock needed by setting PWM_CHNx_CTRL.clk_sel.
3. Configure the channel to work in the capture mode.
4. Enable the INT_EN.chx_int_en to enable the interrupt generation.
5. Enable the channel by writing '1' to PWM_CHNx_CTRL.pwm_en bit to start the channel.
6. When an interrupt is asserted, refer to INTSTS register to know the raw interrupt status. If the corresponding polarity flag is set, turn to PWM_CHNx_PERIOD_HPC register to know the effective high cycles of input waveforms, otherwise turn to PWM_CHNx_DUTY_LPC register to know the effective low cycles.
7. Write '0' to PWM_CHNx_CTRL.pwm_en to disable the channel.

16.6.2 PWM One-shot Mode/Continuous Standard Usage Flow

1. Set PWM_CHNx_CTRL.pwm_en to '0' to disable the PWM channel.
2. Choose the prescale factor and the scale factor for pclk by programming PWM_CHNx_CTRL.prescale and PWM_CHNx_CTRL.scale, and select the clock needed by setting PWM_CHNx_CTRL.clk_sel.
3. Choose the output mode by setting PWM_CHNx_CTRL.output_mode, and set the duty polarity and inactive polarity by programming PWM_CHNx_CTRL.duty_pol and PWM_CHNx_CTRL.inactive_pol.
4. Set the PWM_CHNx_CTRL.rpt if the channel is desired to work in the one-shot mode.
5. Configure the channel to work in the one-shot mode or the continuous mode.
6. Enable the INT_EN.chx_int_en to enable the interrupt generation if if the channel is desired to work in the one-shot mode.
7. If the channel is working in the one-shot mode, an interrupt is asserted after the end of operation, and the PWM_CHNx_CTRL.pwm_en is automatically cleared. Whatever mode the channel is working in, write '0' to PWM_CHNx_CTRL.pwm_en bit to disable the PWM channel.

16.6.3 Low-power mode

Setting PWM_CHNx_CTRL.lp_en to '1' makes the channel enter the low-power mode. When the PWM channel is inactive, the APB bus clock to the clock prescale module is gated in order to reduce the power consumption. It is recommended to disable the channel before entering the low-power mode, and quit the low-power mode before enabling the channel.

16.6.4 Other notes

When the channel is active to produce waveforms, it is free to program the PWM_CHNx_PERIOD_HPC and PWM_CHNx_DUTY_LPC register. The change will not take effect immediately until the current period ends.
An active channel can be changed to another operation mode without disable the PWM channel. However, during the transition of the operation mode there may be some irregular output waveforms.
If the PWM operational frequency is desired to changed, it is recommended to disable the channel first, and then make the channel enter the low-power mode to gate the clock. It is free to change clock setting. After clock setting is changed, quit the lower-power mode and enable the channel to take the change into effect.

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Chapter 17 UART

17.1 Overview

The Universal Asynchronous Receiver/Transmitter (UART) is used for serial communication with a peripheral, modem (data carrier equipment, DCE) or data set. Data is written from a master (CPU) over the APB bus to the UART and it is converted to serial form and transmitted to the destination device. Serial data is also received by the UART and stored for the master (CPU) to read back.
The UART Controller supports the following features:

- Support 3 independent UART controller: UART0, UART1, UART2
- UART0 contains two 64Bytes FIFOs for BT transfer, UART1/UART2 contains two 32Bytes FIFOs for data receive and transmit
- UART0/UART1/UART2 supports auto flow-control
- Support bit rates 115.2Kbps, 460.8Kbps, 921.6Kbps, 1.5Mbps, 3Mbps, 4Mbps
- Support programmable baud rates, even with non-integer clock divider
- Standard asynchronous communication bits (start, stop and parity)
- Support interrupt-based or DMA-based mode
- Support 5-8 bits width transfer

17.2 Block Diagram

This section provides a description about the function and behavior under various conditions. The UART Controller comprises with:

- AMBA APB interface
- FIFO controllers
- Register block
- Modem synchronization block and baud clock generation block
- Serial receiver and serial transmitter

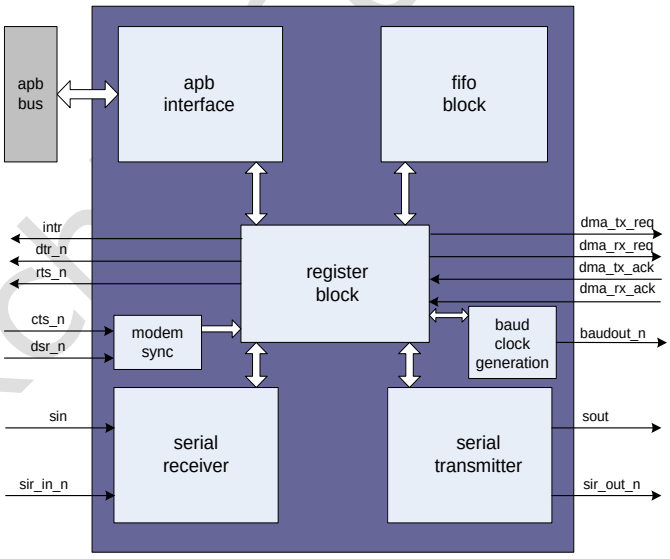


Fig. 17-1 UART Block Diagram

APB INTERFACE
The host processor accesses data, control, and status information on the UART through the APB interface. The UART supports APB data bus widths of 8, 16, and 32 bits.
Register block
Be responsible for the main UART functionality including control, status and interrupt generation.
Modem Synchronization block
Synchronizes the modem input signal.
FIFO block
Be responsible for FIFO control and storage (when using internal RAM) or signaling to control external RAM (when used).

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Baud Clock Generator
Generates the transmitter and receiver baud clock along with the output reference clock signal (baudout_n).
Serial Transmitter
Converts the parallel data, written to the UART, into serial form and adds all additional bits, as specified by the control register, for transmission. This makeup of serial data, referred to as a character can exit the block in two forms, either serial UART format or IrDA 1.0 SIR format.
Serial Receiver
Converts the serial data character (as specified by the control register) received in either the UART or IrDA 1.0 SIR format to parallel form. Parity error detection, framing error detection and line break detection is carried out in this block.

17.3 Function Description

17.3.1 UART (RS232) Serial Protocol

Because the serial communication is asynchronous, additional bits (start and stop) are added to the serial data to indicate the beginning and end. An additional parity bit may be added to the serial character. This bit appears after the last data bit and before the stop bit(s) in the character structure to perform simple error checking on the received data, as shown in below figure.

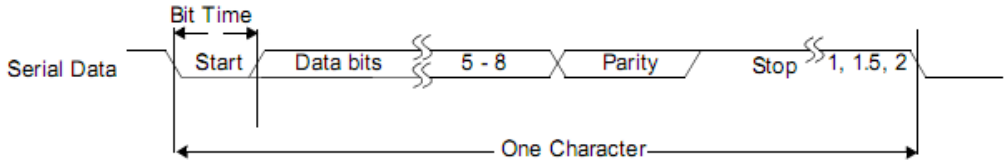


Fig. 17-2 UART Serial protocol

17.3.2 IrDA 1.0 SIR Protocol

The Infrared Data Association (IrDA) 1.0 Serial Infrared (SIR) mode supports bi-directional data communications with remote devices using infrared radiation as the transmission medium. IrDA 1.0 SIR mode specifies a maximum baud rate of 115.2Kbaud.
Transmitting a single infrared pulse signals a logic zero, while a logic one is represented by not sending a pulse. The width of each pulse is 3/16ths of a normal serial bit time. Data transfers can only occur in half-duplex fashion when IrDA SIR mode is enabled.

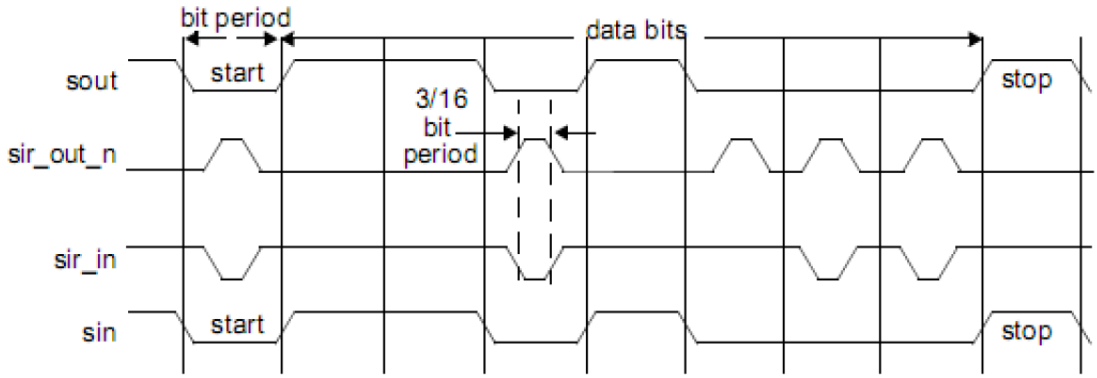


Fig. 17-3 IrDA 1.0

17.3.3 Baud Clock

The baud rate is controlled by the serial clock (sclk or pclk in a single clock implementation) and the Divisor Latch Register (UART_DLH and UART_DLL). As the exact number of baud clocks that each bit was transmitted for is known, calculating the mid-point for sampling is not difficult, that is every 16 baud clocks after the mid-point sample of the start bit.

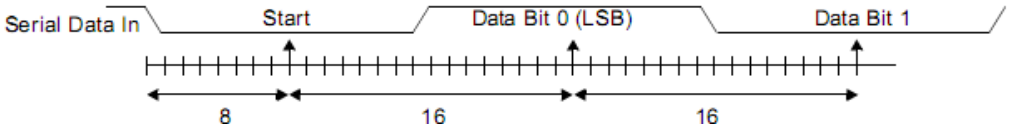


Fig. 17-4 UART baud rate

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17.3.4 FIFO Support

NONE FIFO MODE

If FIFO support is not selected, then no FIFOs are implemented. Only a single received data byte can be stored at a time in the UART_RBR or a single transmitted data byte can be sent at a time in the UART_THR.

FIFO MODE

The FIFO mode is enabled by register UART_FCR[0].

17.3.5 Interrupts

The following interrupt types can be enabled with the UART_IER register.

- Receiver Error
- Receiver Data Available
- Character Timeout (in FIFO mode only)
- Transmitter Holding Register Empty at/below threshold (in Programmable UART_THRE Interrupt mode)
- Modem Status

17.3.6 DMA Support

The UART supports DMA signaling with the use of two output signals (dma_tx_req_n and dma_rx_req_n) to indicate when data is ready to be read or when the transmit FIFO is empty.

The dma_tx_req_n signal is asserted under the following conditions:

- When the Transmitter Holding Register is empty in non-FIFO mode.
- When the transmitter FIFO is empty in FIFO mode with Programmable THRE interrupt mode disabled.
- When the transmitter FIFO is at or below the programmed threshold with Programmable THRE interrupt mode enabled.

The dma_rx_req_n signal is asserted under the following conditions:

- When there is a single character available in the Receive Buffer Register in non-FIFO mode.
- When the Receiver FIFO is at or above the programmed trigger level in FIFO mode.

17.3.7 Auto Flow Control

The UART can be configured to have a 16750-compatible Auto RTS and Auto CTS serial data flow control mode available. If FIFOs are not implemented, then this mode cannot be selected. When Auto Flow Control mode has been selected, it can be enabled with the Modem Control Register (UART_MCR[5]). Following figure shows a block diagram of the Auto Flow Control functionality.

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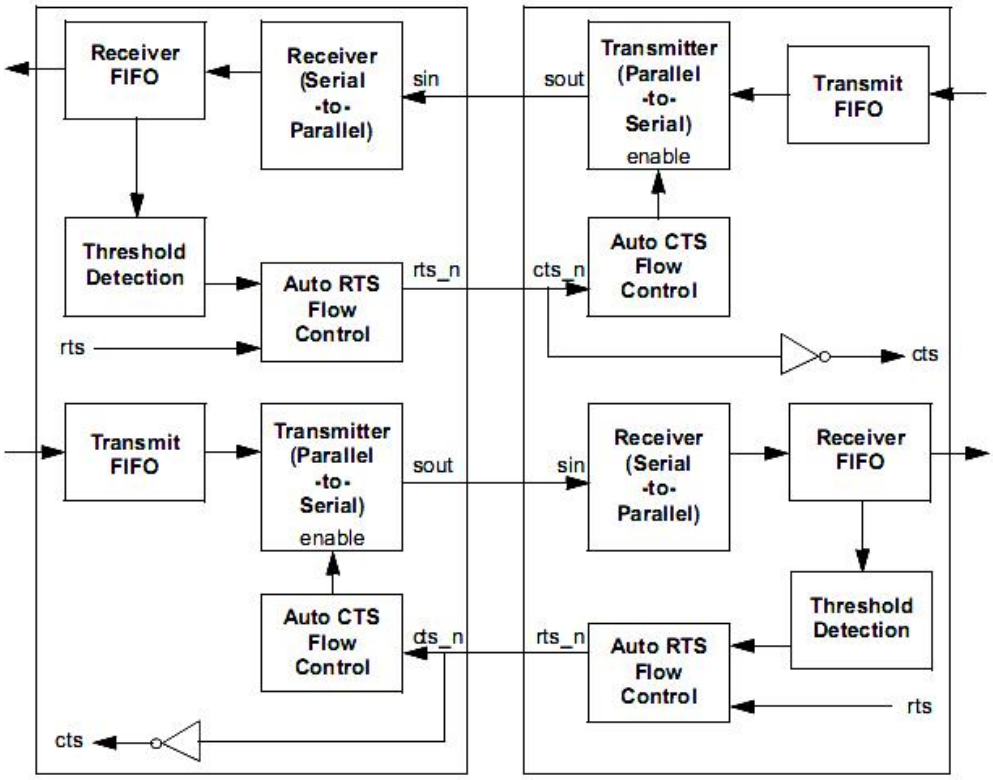


Fig. 17-5 UART Auto flow control block diagram

Auto RTS – Becomes active when the following occurs:

- Auto Flow Control is selected during configuration (UART_MCR[5] is set to 1)
- FIFOs are implemented
- RTS (UART_MCR[1] bit and UART_MCR[5]bit are both set to 1)
- FIFOs are enabled (UART_FCR[0]) bit is set to 1)
- SIR mode is disabled (UART_MCR[6] bit is set to 0)

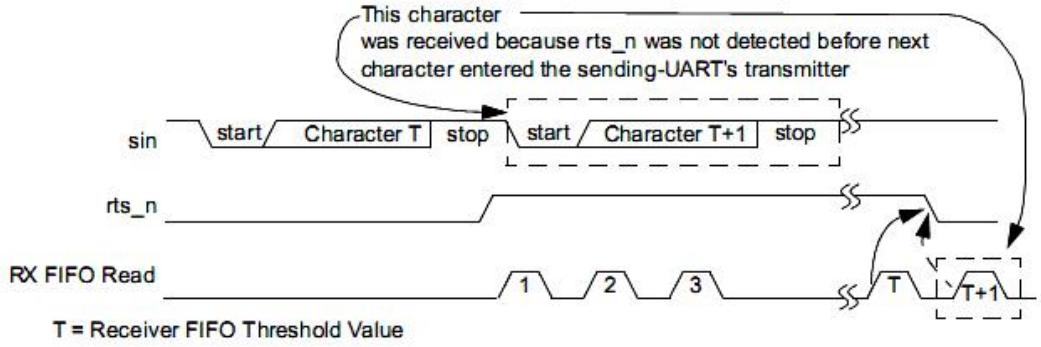


Fig. 17-6 UART AUTO RTS TIMING

Auto CTS – becomes active when the following occurs:

- Auto Flow Control is selected during configuration (UART_MCR[5] is set to 1)
- FIFOs are implemented
- AFCE (UART_MCR[5] bit is set to 1)
- FIFOs are enabled (UART_FCR[0]) bit is set to 1)
- SIR mode is disabled (UART_MCR[6] bit is set to 0)

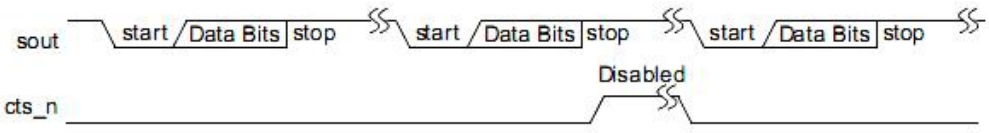


Fig. 17-7 UART AUTO CTS TIMING

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17.4 Register Description

ALL the UARTs have the same register information, and with its own Base Address respectively.
The UART0's Base Address is 0x20060000.
The UART1's Base Address is 0x20064000.
The UART2's Base Address is 0x20068000.

17.4.1 Registers Summary

Name	Offset	Size	Reset Value	Description
UART_RBR	0x0000	W	0x00000000	Receive Buffer Register
UART_THR	0x0000	W	0x00000000	Transmit Holding Register
UART_DLL	0x0000	W	0x00000000	Divisor Latch (Low) Register
UART_DLH	0x0004	W	0x00000000	Divisor Latch (High) Register
UART_IER	0x0004	W	0x00000000	Interrupt Enable Register
UART_IIR	0x0008	W	0x00000000	Interrupt Identification Register
UART_FCR	0x0008	W	0x00000000	FIFO Control Register
UART_LCR	0x000c	W	0x00000000	Line Control Register
UART_MCR	0x0010	W	0x00000000	Modem Control Register
UART_LSR	0x0014	W	0x00000000	Line Status Register
UART_MSR	0x0018	W	0x00000000	Modem Status Register
UART_SCR	0x001c	W	0x00000000	Scratchpad Register
UART_SRBR	0x0030	W	0x00000000	Shadow Receive Buffer Register
UART_STHR	0x006c	W	0x00000000	Shadow Transmit Holding Register
UART_FAR	0x0070	W	0x00000000	FIFO Access Register
UART_TFR	0x0074	W	0x00000000	Transmit FIFO Read Register
UART_RFW	0x0078	W	0x00000000	Receive FIFO Write Register
UART_USR	0x007c	W	0x00000000	UART Status Register
UART_TFL	0x0080	W	0x00000000	Transmit FIFO Level Register
UART_RFL	0x0084	W	0x00000000	Receive FIFO Level Register
UART_SRR	0x0088	W	0x00000000	Software Reset Register
UART_SRTS	0x008c	W	0x00000000	Shadow Request to Send Register
UART_SBCR	0x0090	W	0x00000000	Shadow Break Control Register
UART_SDMAM	0x0094	W	0x00000000	Shadow DMA Mode Register
UART_SFE	0x0098	W	0x00000000	Shadow FIFO Enable Register
UART_SRT	0x009c	W	0x00000000	Shadow RCVR Trigger Register
UART_STET	0x00a0	W	0x00000000	Shadow TX Empty Trigger Register
UART_HTX	0x00a4	W	0x00000000	Halt TX Register
UART_DMASA	0x00a8	W	0x00000000	DMA Software Acknowledge Register
UART_CPR	0x00f4	W	0x00000000	Component Parameter Register
UART_UCV	0x00f8	W	0x0330372a	UART Component Version Register
UART_CTR	0x00fc	W	0x44570110	Component Type Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

17.4.2 Detail Register Description

UART_RBR

Address: Operational Base + offset (0x0000)
Receive Buffer Register

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Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x00	data_input Data byte received on the serial input port (sin) in UART mode, or the Serial Infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line Status Register (UART_LCR) is set. If in non-FIFO mode or FIFOs are disabled (UART_FCR[0] is set to 0), the data in the UART_RBR must be read before the next data arrives, otherwise it is overwritten, resulting in an over-run error. If in FIFO mode and FIFOs are enabled (UART_FCR[0] is set to 1), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO is preserved, but any incoming data are lost and an over-run error occurs.

UART_THR
Address: Operational Base + offset (0x0000)
Transmit Holding Register

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x00	data_output Data to be transmitted on the serial output port (sout) in UART mode or the Serial Infrared output (sir_out_n) in infrared mode. Data should only be written to the UART_THR when the THR Empty (THRE) bit (UART_LSR[5]) is set to 1. If in non-FIFO mode or FIFOs are disabled (UART_FCR[0] is set to 0) and THRE is set, writing a single character to the THR clears the THRE. Any additional writes to the UART_THR before the THRE is set again causes the UART_THR data to be overwritten. If in FIFO mode and FIFOs are enabled (UART_FCR[0] is set to 1) and THRE is set, x number of characters of data may be written to the UART_THR before the FIFO is full. The number x (default=16) is determined by the value of FIFO Depth that you set during configuration. Any attempt to write data when the FIFO is full results in the write data being lost.

UART_DLL
Address: Operational Base + offset (0x0000)
Divisor Latch (Low) Register

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	baud_rate_divisor_L Lower 8-bits of a 16-bit Divisor Latch register that contains the baud rate divisor for the UART. This register may only be accessed when the DLAB bit (UART_LCR[7]) is set to 1 and the UART is not busy (UART_USR[0] is 0). The output baud rate is equal to the serial clock (sclk) frequency divided by 16 times the value of the baud rate divisor, as follows: baud rate = (serial clock freq) / (16 * divisor). Note that with the Divisor Latch Registers (UART_DLL and UART_DLH) are set to 0, the baud clock is disabled and no serial communications occur. Also, once the UART_DLH is set, at least 8 clock cycles of the slowest UART clock should be allowed to pass before transmitting or receiving data.

UART_DLH
Address: Operational Base + offset (0x0004)
Divisor Latch (High) Register

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x00	baud_rate_divisor_H Upper 8 bits of a 16-bit Divisor Latch register that contains the baud rate divisor for the UART.

UART_IER
Address: Operational Base + offset (0x0004)
Interrupt Enable Register

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7	RW	0x0	prog_thre_int_en This is used to enable/disable the generation of THRE Interrupt. 1'b0: disabled 1'b1: enabled
6:4	RO	0x0	reserved
3	RW	0x0	modem_status_int_en This is used to enable/disable the generation of Modem Status Interrupt. This is the fourth highest priority interrupt. 1'b0: disabled 1'b1: enabled
2	RW	0x0	receive_line_status_int_en This is used to enable/disable the generation of Receiver Line Status Interrupt. This is the highest priority interrupt. 1'b0: disabled 1'b1: enabled

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Bit	Attr	Reset Value	Description
1	RW	0x0	trans_hold_empty_int_en This is used to enable/disable the generation of Transmit Holding Register Empty Interrupt. This is the highest priority interrupt. 1'b0: disabled 1'b1: enabled
0	RW	0x0	receive_data_available_int_en This is used to enable/disable the generation of Received Data Available Interrupt and the Character Timeout Interrupt (if in FIFO mode and FIFOs enabled). These are the second highest priority interrupts. 1'b0: disabled 1'b1: enabled

UART_IIR
Address: Operational Base + offset (0x0008)
Interrupt Identification Register

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:6	RO	0x0	fifos_en This is used to indicate whether the FIFOs are enabled or disabled. 2'b00: disabled 2'b11: enabled
5:4	RO	0x0	reserved
3:0	RO	0x0	int_id This indicates the highest priority pending interrupt which can be one of the following types: 4'b0000: modem status 4'b0001: no interrupt pending 4'b0010: THR empty 4'b0100: received data available 4'b0110: receiver line status 4'b0111: busy detect 4'b1100: character timeout

UART_FCR
Address: Operational Base + offset (0x0008)
FIFO Control Register

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
7:6	WO	0x0	rcvr_trigger This is used to select the trigger level in the receiver FIFO at which the Received Data Available Interrupt is generated. In auto flow control mode it is used to determine when the rts_n signal is de-asserted. It also determines when the dma_rx_req_n signal is asserted in certain modes of operation. The following trigger levels are supported: 2'b00: 1 character in the FIFO 2'b01: FIFO 1/4 full 2'b10: FIFO 1/2 full 2'b11: FIFO 2 less than ful
5:4	WO	0x0	tx_empty_trigger This is used to select the empty threshold level at which the THRE Interrupts are generated when the mode is active. It also determines when the dma_tx_req_n signal is asserted when in certain modes of operation. The following trigger levels are supported: 2'b00: FIFO empty 2'b01: 2 characters in the FIFO 2'b10: FIFO 1/4 full 2'b11: FIFO 1/2 full
3	WO	0x0	dma_mode This determines the DMA signalling mode used for the dma_tx_req_n and dma_rx_req_n output signals when additional DMA handshaking signals are not selected. 1'b0: mode 0 1'b1: mode 11100 = character timeout.
2	WO	0x0	xmit_fifo_reset This resets the control portion of the transmit FIFO and treats the FIFO as empty. This also de-asserts the DMA TX request and single signals when additional DMA handshaking signals are selected. Note that this bit is 'self-clearing'. It is not necessary to clear this bit. 1'b0: disabled 1'b1: enabled
1	WO	0x0	rcvr_fifo_reset This resets the control portion of the receive FIFO and treats the FIFO as empty. This also de-asserts the DMA RX request and single signals when additional DMA handshaking signals are selected. Note that this bit is 'self-clearing'. It is not necessary to clear this bit. 1'b0: disabled 1'b1: enabled

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Bit	Attr	Reset Value	Description
0	WO	0x0	fifo_en FIFO Enable. This enables/disables the transmit (XMIT) and receive (RCVR) FIFOs. Whenever the value of this bit is changed both the XMIT and RCVR controller portion of FIFOs is reset. 1'b0: disabled 1'b1: enabled

UART_LCR

Address: Operational Base + offset (0x000c)

Line Control Register

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7	RW	0x0	div_lat_access Writeable only when UART is not busy (UART_USR[0] is zero), always readable. This bit is used to enable reading and writing of the Divisor Latch register (UART_DLL and UART_DLH) to set the baud rate of the UART. This bit must be cleared after initial baud rate setup in order to access other registers.
6	RW	0x0	break_ctrl Break Control Bit. This is used to cause a break condition to be transmitted to the receiving device. If set to 1 the serial output is forced to the spacing (logic 0) state. When not in Loopback Mode, as determined by UART_MCR[4], the sout line is forced low until the Break bit is cleared. If UART_MCR[6] set to 1, the sir_out_n line is continuously pulsed. When in Loopback Mode, the break condition is internally looped back to the receiver and the sir_out_n line is forced low.
5	RO	0x0	reserved
4	RW	0x0	even_parity_sel Even Parity Select. Writeable only when UART is not busy (UART_USR[0] is zero), always readable. This is used to select between even and odd parity, when parity is enabled (UART_LCR[3] set to 1). If set to 1, an even number of logic 1s is transmitted or checked. If set to 0, an odd number of logic 1s is transmitted or checked.
3	RW	0x0	parity_en Parity Enable. Writeable only when UART is not busy (UART_USR[0] is zero), always readable. This bit is used to enable and disable parity generation and detection in transmitted and received serial character respectively. 1'b0: parity disabled 1'b1: parity enabled

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Bit	Attr	Reset Value	Description
2	RW	0x0	stop_bits_num Number of stop bits. Writeable only when UART is not busy (UART_USR[0] is zero), always readable. This is used to select the number of stop bits per character that the peripheral transmits and receives. If set to 0, one stop bit is transmitted in the serial data. If set to 1 and the data bits are set to 5 (UART_LCR[1:0] set to 0) one and a half stop bits is transmitted. Otherwise, two stop bits are transmitted. Note that regardless of the number of stop bits selected, the receiver checks only the first stop bit. 1'b0: 1 stop bit 1'b1: 1.5 stop bits when DLS (UART_LCR[1:0]) is zero, else 2 stop bit.
1:0	RW	0x0	data_length_sel Data Length Select. Writeable only when UART is not busy (UART_USR[0] is zero), always readable. This is used to select the number of data bits per character that the peripheral transmits and receives. The number of bit that may be selected areas follows: 2'b00: 5 bits 2'b01: 6 bits 2'b10: 7 bits 2'b11: 8 bits

UART_MCR

Address: Operational Base + offset (0x0010)

Modem Control Register

Bit	Attr	Reset Value	Description
31:7	RO	0x0	reserved
6	RW	0x0	sir_mode_en SIR Mode Enable. This is used to enable/disable the IrDA SIR Mode. 1'b0: IrDA SIR Mode disabled 1'b1: IrDA SIR Mode enabled
5	RW	0x0	auto_flow_ctrl_en Auto Flow Control Enable. 1'b0: Auto Flow Control Mode disabled 1'b1: Auto Flow Control Mode enabled
4	RW	0x0	loopback LoopBack Bit. This is used to put the UART into a diagnostic mode for test purposes.

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Bit	Attr	Reset Value	Description
3	RW	0x0	out2 This is used to directly control the user-designated Output2 (out2_n) output. The value written to this location is inverted and driven out on out2_n, that is: 1'b0: out2_n de-asserted (logic 1) 1'b1: out2_n asserted (logic 0)
2	RW	0x0	out1 This is used to directly control the user-designated Output2 (out2_n) output. The value written to this location is inverted and driven out on out2_n, that is: 1'b0: out2_n de-asserted (logic 1) 1'b1: out2_n asserted (logic 0)
1	RW	0x0	req_to_send Request to Send. This is used to directly control the Request to Send (rts_n) output. The Request To Send (rts_n) output is used to inform the modem or data set that the UART is ready to exchange data.
0	RW	0x0	data_terminal_ready Data Terminal Ready. This is used to directly control the Data Terminal Ready (dtr_n) output. The value written to this location is inverted and driven out on dtr_n, that is: 1'b0: dtr_n de-asserted (logic 1) 1'b1: dtr_n asserted (logic 0)

UART_LSR
Address: Operational Base + offset (0x0014)
Line Status Register

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7	RO	0x0	receiver_fifo_error Receiver FIFO Error bit. This bit is relevant FIFOs are enabled (UART_FCR[0] set to 1). This is used to indicate if there is at least one parity error, framing error, or break indication in the FIFO. 1'b0: no error in RX FIFO 1'b1: error in RX FIFO
6	RO	0x0	trans_empty Transmitter Empty bit. If FIFOs enabled (UART_FCR[0] set to 1), this bit is set whenever the Transmitter Shift Register and the FIFO are both empty. If FIFOs are disabled, this bit is set whenever the Transmitter Holding Register and the Transmitter Shift Register are both empty.

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Bit	Attr	Reset Value	Description
5	RO	0x0	trans_hold_reg_empty Transmit Holding Register Empty bit. If THRE mode is disabled (UART_IER[7] set to 0) and regardless of FIFO's being implemented/enabled or not, this bit indicates that the UART_THR or TX FIFO is empty. This bit is set whenever data is transferred from the UART_THR or TX FIFO to the transmitter shift register and no new data has been written to the UART_THR or TX FIFO. This also causes a THRE Interrupt to occur, if the THRE Interrupt is enabled. If UART_IER[7] set to 1 and UART_FCR[0] set to 1 respectively, the functionality is switched to indicate the transmitter FIFO is full, and no longer controls THRE interrupts, which are then controlled by the UART_FCR[5:4] threshold setting.
4	RO	0x0	break_int Break Interrupt bit. This is used to indicate the detection of a break sequence on the serial input data.
3	RO	0x0	framing_error Framing Error bit. This is used to indicate the occurrence of a framing error in the receiver. A framing error occurs when the receiver does not detect a valid STOP bit in the received data.
2	RO	0x0	parity_eror Parity Error bit. This is used to indicate the occurrence of a parity error in the receiver if the Parity Enable (PEN) bit (UART_LCR[3]) is set.
1	RO	0x0	overrun_error Overrun error bit. This is used to indicate the occurrence of an overrun error. This occurs if a new data character was received before the previous data was read.
0	RO	0x0	data_ready Data Ready bit. This is used to indicate that the receiver contains at least one character in the UART_RBR or the receiver FIFO. 1'b0: no data ready 1'b1: data ready

UART_MSR
Address: Operational Base + offset (0x0018)
Modem Status Register

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7	RO	0x0	data_carrior_detect Data Carrier Detect. This is used to indicate the current state of the modem control line dcd_n.
6	RO	0x0	ring_indicator Ring Indicator. This is used to indicate the current state of the modem control line ri_n.

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Bit	Attr	Reset Value	Description
5	RO	0x0	data_set_ready Data Set Ready. This is used to indicate the current state of the modem control line dsr_n.
4	RO	0x0	clear_to_send Clear to Send. This is used to indicate the current state of the modem control line cts_n.
3	RO	0x0	delta_data_carrier_detect Delta Data Carrier Detect. This is used to indicate that the modem control line dcd_n has changed since the last time the UART_MSR was read.
2	RO	0x0	trailing_edge_ring_indicator Trailing Edge of Ring Indicator. This is used to indicate that a change on the input ri_n (from an active-low to an inactive-high state) has occurred since the last time the UART_MSR was read.
1	RO	0x0	delta_data_set_ready Delta Data Set Ready. This is used to indicate that the modem control line dsr_n has changed since the last time the UART_MSR was read.
0	RO	0x0	delta_clear_to_send Delta Clear to Send. This is used to indicate that the modem control line cts_n has changed since the last time the UART_MSR was read.

UART_SCR
Address: Operational Base + offset (0x001c)
Scratchpad Register

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x00	temp_store_space This register is for programmers to use as a temporary storage space.

UART_SRBR
Address: Operational Base + offset (0x0030)
Shadow Receive Buffer Register

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
7:0	RO	0x00	shadow_rbr This is a shadow register for the UART_RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART mode or the Serial Infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (UART_LSR) is set. If FIFOs are disabled (UART_FCR[0] set to 0), the data in the RBR must be read before the next data arrives, otherwise it is overwritten, resulting in an overrun error. If FIFOs are enabled (UART_FCR[0] set to 1), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO are preserved, but any incoming data is lost. An overrun error also occurs.

UART_STHR
Address: Operational Base + offset (0x006c)
Shadow Transmit Holding Register

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RO	0x00	shadow_thr This is a shadow register for the UART_THR.

UART_FAR
Address: Operational Base + offset (0x0070)
FIFO Access Register

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	fifo_access_test_en This register is use to enable a FIFO access mode for testing, so that the receive FIFO can be written by the master and the transmit FIFO can be read by the master when FIFOs are implemented and enabled. When FIFOs are not enabled it allows the UART_RBR to be written by the master and the UART_THR to be read by the master. 1'b0: FIFO access mode disabled 1'b1: FIFO access mode enabled

UART_TFR
Address: Operational Base + offset (0x0074)
Transmit FIFO Read Register

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
7:0	RO	0x00	trans_fifo_read Transmit FIFO Read. These bits are only valid when FIFO access mode is enabled (UART_FAR[0] is set to 1).When FIFOs are implemented and enabled, reading this register gives the data at the top of the transmit FIFO. Each consecutive read pops the transmit FIFO and gives the next data value that is currently at the top of the FIFO.

UART_RFW
Address: Operational Base + offset (0x0078)
Receive FIFO Write Register

Bit	Attr	Reset Value	Description
31:10	RO	0x0	reserved
9	WO	0x0	receive_fifo_framing_error Receive FIFO Framing Error. These bits are only valid when FIFO access mode is enabled (UART_FAR[0] is set to 1).
8	WO	0x0	receive_fifo_parity_error Receive FIFO Parity Error. These bits are only valid when FIFO access mode is enabled (UART_FAR[0] is set to 1).
7:0	WO	0x00	receive_fifo_write Receive FIFO Write Data. These bits are only valid when FIFO access mode is enabled (UART_FAR[0] is set to 1). When FIFOs are enabled, the data that is written to the RFWD is pushed into the receive FIFO. Each consecutive write pushes the new data to the next write location in the receive FIFO. When FIFOs not enabled, the data that is written to the RFWD is pushed into the UART_RBR.

UART_USR
Address: Operational Base + offset (0x007c)
UART Status Register

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4	RO	0x0	receive_fifo_full Receive FIFO Full. This is used to indicate that the receive FIFO is completely full. 1'b0: Receive FIFO not full 1'b1: Receive FIFO Full This bit is cleared when the RX FIFO is no longer full.
3	RO	0x0	receive_fifo_not_empty Receive FIFO Not Empty. This is used to indicate that the receive FIFO contains one or more entries. 1'b0: Receive FIFO is empty 1'b1: Receive FIFO is not empty This bit is cleared when the RX FIFO is empty.

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Bit	Attr	Reset Value	Description
2	RO	0x0	trasn_fifo_empty Transmit FIFO Empty. This is used to indicate that the transmit FIFO is completely empty. 1'b0: Transmit FIFO is not empty 1'b1: Transmit FIFO is empty This bit is cleared when the TX FIFO is no longer empty
1	RO	0x0	trans_fifo_not_full Transmit FIFO Not Full. This is used to indicate that the transmit FIFO in not full. 1'b0: Transmit FIFO is full 1'b1: Transmit FIFO is not full This bit is cleared when the TX FIFO is full.
0	RO	0x0	uart_busy UART Busy. This is indicates that a serial transfer is in progress, when cleared indicates that the UART is idle or inactive. 1'b0: UART is idle or inactive 1'b1: UART is busy (actively transferring data)

UART_TFL
Address: Operational Base + offset (0x0080)
Transmit FIFO Level Register

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4:0	RW	0x00	trans_fifo_level Transmit FIFO Level. This is indicates the number of data entries in the transmit FIFO.

UART_RFL
Address: Operational Base + offset (0x0084)
Receive FIFO Level Register

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4:0	RO	0x00	receive_fifo_level Receive FIFO Level. This is indicates the number of data entries in the receive FIFO.

UART_SRR
Address: Operational Base + offset (0x0088)
Software Reset Register

Bit	Attr	Reset Value	Description
31:3	RO	0x0	reserved
2	WO	0x0	xmit_fifo_reset XMIT FIFO Reset. This is a shadow register for the XMIT FIFO Reset bit (UART_FCR[2]).

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Bit	Attr	Reset Value	Description
1	WO	0x0	rcvr_fifo_reset RCVR FIFO Reset. This is a shadow register for the RCVR FIFO Reset bit (UART_FCR[1]).
0	WO	0x0	uart_reset UART Reset. This asynchronously resets the UART and synchronously removes the reset assertion. For a two clock implementation both pclk and sclk domains are reset.

UART_SRTS
Address: Operational Base + offset (0x008c)
Shadow Request to Send Register

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	shadow_req_to_send Shadow Request to Send. This is a shadow register for the RTS bit (UART_MCR[1]), this can be used to remove the burden of having to performing a read-modify-write on the UART_MCR.

UART_SBCR
Address: Operational Base + offset (0x0090)
Shadow Break Control Register

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	shadow_break_ctrl Shadow Break Control Bit. This is a shadow register for the Break bit (UART_LCR[6]), this can be used to remove the burden of having to performing a read modify write on the UART_LCR.

UART_SDMAM
Address: Operational Base + offset (0x0094)
Shadow DMA Mode Register

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	shadow_dma_mode Shadow DMA Mode. This is a shadow register for the DMA mode bit (UART_FCR[3]).

UART_SFE
Address: Operational Base + offset (0x0098)
Shadow FIFO Enable Register

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	shadow_fifo_en Shadow FIFO Enable. This is a shadow register for the FIFO enable bit (UART_FCR[0]).

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UART_SRT
Address: Operational Base + offset (0x009c)
Shadow RCVR Trigger Register

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	shadow_rcvr_trigger Shadow RCVR Trigger. This is a shadow register for the RCVR trigger bits (UART_FCR[7:6]).

UART_STET
Address: Operational Base + offset (0x00a0)
Shadow TX Empty Trigger Register

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	shadow_tx_empty_trigger Shadow TX Empty Trigger. This is a shadow register for the TX empty trigger bits (UART_FCR[5:4]).

UART_HTX
Address: Operational Base + offset (0x00a4)
Halt TX Register

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	halt_tx_en This register is use to halt transmissions for testing, so that the transmit FIFO can be filled by the master when FIFOs are implemented and enabled. 1'b0: Halt TX disabled 1'b1: Halt TX enabled

UART_DMASA
Address: Operational Base + offset (0x00a8)
DMA Software Acknowledge Register

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	WO	0x0	dma_software_ack This register is use to perform a DMA software acknowledge if a transfer needs to be terminated due to an error condition.

UART_CPR
Address: Operational Base + offset (0x00f4)
Component Parameter Register

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
23:16	RO	0x00	FIFO_MODE 8'h00: 0 8'h01: 16 8'h02: 32 …… 8'h80: 2048 8'h81- 8'hff: reserved
15:14	RO	0x0	reserved
13	RO	0x0	DMA_EXTRA 1'b0: FALSE 1'b1: TRUE
12	RO	0x0	UART_ADD_ENCODED_PARAMS 1'b0: FALSE 1'b1: TRUE
11	RO	0x0	SHADOW 1'b0: FALSE 1'b1: TRUE
10	RO	0x0	FIFO_STAT 1'b0: FALSE 1'b1: TRUE
9	RO	0x0	FIFO_ACCESS 1'b0: FALSE 1'b1: TRUE
8	RO	0x0	NEW_FEAT 1'b0: FALSE 1'b1: TRUE
7	RO	0x0	SIR_LP_MODE 1'b0: FALSE 1'b1: TRUE
6	RO	0x0	SIR_MODE 1'b0: FALSE 1'b1: TRUE
5	RO	0x0	THRE_MODE 1'b0: FALSE 1'b1: TRUE
4	RO	0x0	AFCE_MODE 1'b0: FALSE 1'b1: TRUE
3:2	RO	0x0	reserved
1:0	RO	0x0	APB_DATA_WIDTH 2'b00: 8 bits 2'b01: 16 bits 2'b10: 32 bits 2'b11: reserved

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UART_UCV
Address: Operational Base + offset (0x00f8)
UART Component Version Register

Bit	Attr	Reset Value	Description
31:0	RO	0x0330372a	ver ASCII value for each number in the version

UART_CTR
Address: Operational Base + offset (0x00fc)
Component Type Register

Bit	Attr	Reset Value	Description
31:0	RO	0x44570110	peripheral_id This register contains the peripherals identification code.

17.5 Interface Description

Table 17-1 UART0 Interface Description

Module Pin	Direction	Pad Name	IOMUX
uart0_sin	I	IO_SCclk_URT0sin_GPIO2d3	GRF_GPIO2D_IOMUX[7:6]=2'b10
uart0_sout	O	IO_SCrst_URT0sout_GPIO2d2	GRF_GPIO2D_IOMUX[5:4]=2'b10
uart0_cts_n	I	IO_SCdetect_URT0Ctsn_GPIO2d5	GRF_GPIO2D_IOMUX[11:10]=2'b10
uart0_rts_n	O	IO_Scio_URT0rtsn_GPIO0c1	GRF_GPIO0C_IOMUX[3:2]=2'b10

Notes: I=input, O=output, I/O=input/output, bidirectional

Table 17-2 UART1 Interface Description

Module Pin	Direction	Pad Name	IOMUX
uart1_sin	I	IO_SPIrxd_UART1sin_GPIO1b2	GRF_GPIO1B_IOMUX[5:4]=2'b10
uart1_sout	O	IO_SPItxd_UART1sout_GPIO1b1	GRF_GPIO1B_IOMUX[3:2]=2'b10
uart1_cts_n	I	IO_SPIclk_UART1ctsn_GPIO1b0	GRF_GPIO1B_IOMUX[1:0]=2'b10
uart1_rts_n	O	IO_SPIcsn0_UART1rtsn_GPIO1b3	GRF_GPIO1B_IOMUX[7:6]=2'b10

Notes: I=input, O=output, I/O=input/output, bidirectional

Table 17-3 UART2 Interface Description

Module Pin	Direction	Pad Name	IOMUX
uart2_sin	I	IO_MMC0d1_UART2rx_GPIO1c3	GRF_GPIO1C_IOMUX[7:6]=2'b10
uart2_sout	O	IO_MMC0d0_UART2tx_GPIO1c2	GRF_GPIO1C_IOMUX[5:4]=2'b10
uart2_cts_n	I	IO_URT2ctsn_GPIO0d1	GRF_GPIO0D_IOMUX[2]=1'b1
uart2_rts_n	O	IO_URT2rtsn_PMICsleep0_GPIO0d0	GRF_GPIO0D_IOMUX[1:0]=2'b01

Notes: I=input, O=output, I/O=input/output, bidirectional

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17.6 Application Notes

17.6.1 None FIFO Mode Transfer Flow

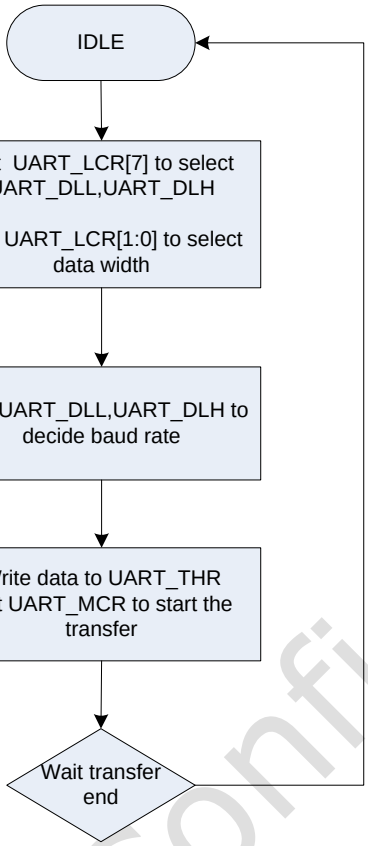


Fig. 17-8 UART none fifo mode

17.6.2 FIFO Mode Transfer Flow

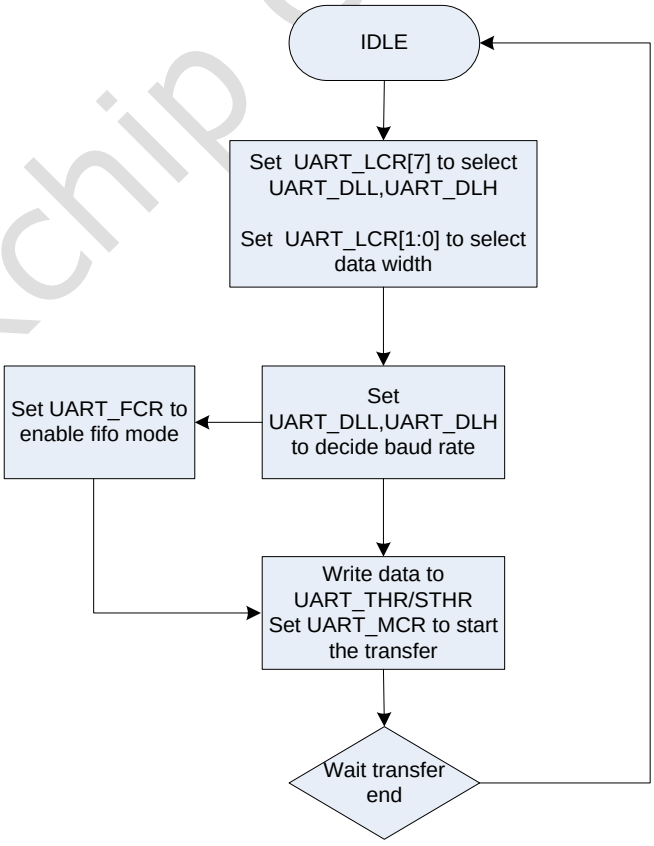


Fig. 17-9 UART fifo mode

The UART is an APB slave performing:

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Serial-to-parallel conversion on data received from a peripheral device.
Parallel-to-serial conversion on data transmitted to the peripheral device.
The CPU reads and writes data and control/status information through the APB interface.
The transmitting and receiving paths are buffered with internal FIFO memories enabling up to 64-bytes to be stored independently in both transmit and receive modes. A baud rate generator can generate a common transmit and receive internal clock input. The baud rates will depend on the internal clock frequency. The UART will also provide transmit, receive and exception interrupts to system.

17.6.3 Baud Rate Calculation

UART clock generation

The following figures shows the UART clock generation.
UART0 source clocks can be selected from four PLL outputs (CODEC PLL/GENERAL PLL/GENERAL PLL D2/USBPHY_480M). UART1 and UART2 source clocks can be selected from three PLL outputs (CODEC PLL/GENERAL PLL/GENERAL PLL D2). UART clocks can be generated by 1 to 64 division of its source clock, or can be fractionally divided again.

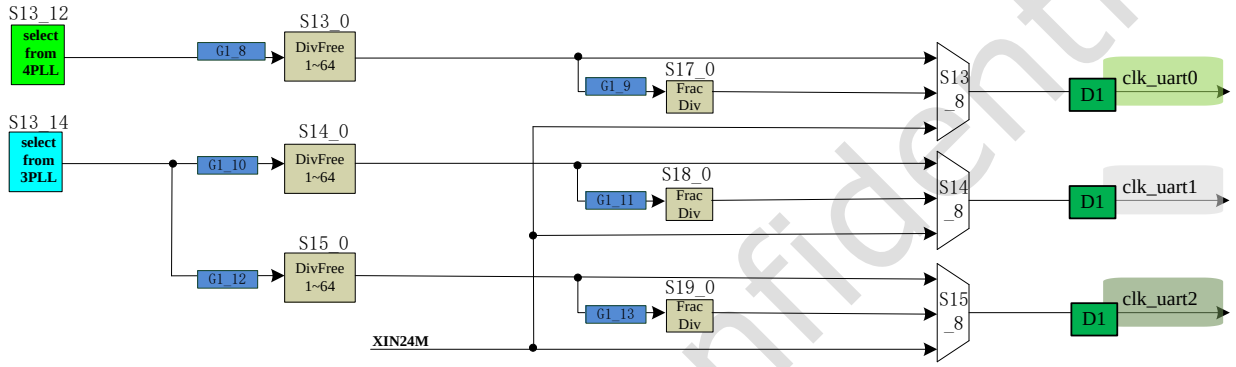


Fig. 17-10 UART clock generation

UART baud rate configuration

The following table provides some reference configuration for different UART baud rates.

Table 17-4 UART baud rate configuration

Baud Rate	Reference Configuration
115.2 Kbps	Configure SOURCE PLL to get 648MHz clock output; Divide 648MHz clock by 1152/50625 to get 14.7456MHz clock; Configure UART_DLL to 8.
460.8 Kbps	Configure SOURCE PLL to get 648MHz clock output; Divide 648MHz clock by 1152/50625 to get 14.7456MHz clock; Configure UART_DLL to 2.
921.6 Kbps	Configure SOURCE PLL to get 648MHz clock output; Divide 648MHz clock by 1152/50625 to get 14.7456MHz clock; Configure UART_DLL to 1.
1.5 Mbps	Choose SOURCE PLL to get 384MHz clock output; Divide 384MHz clock by 16 to get 24MHz clock; Configure UART_DLL to 1
3 Mbps	Choose SOURCE PLL to get 384MHz clock output; Divide 384MHz clock by 8 to get 48MHz clock; Configure UART_DLL to 1
4 Mbps	Configure SOURCE PLL to get 384MHz clock output; Divide 384MHz clock by 6 to get 64MHz clock; Configure UART_DLL to 1

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Chapter 18 General-Purpose I/O Ports(GPIO)

18.1 Overview

GPIO is a programmable General Purpose Programming I/O peripheral. This component is a APB slave device. GPIO controls the output data and direction of external I/O pads. It also can read back the data on external pads using memory-mapped registers.
GPIO supports the following features:

- 32 bits APB bus width
- 32 independently configurable signals
- Separate data registers and data direction registers for each signal
- Software control for each signal, or for each bit of each signal
- Configurable interrupt mode for Port A
- Port A has 32 bits

Notes: Port A 32bits are corresponding to port A/B/C/D 8bits

18.2 Block Diagram

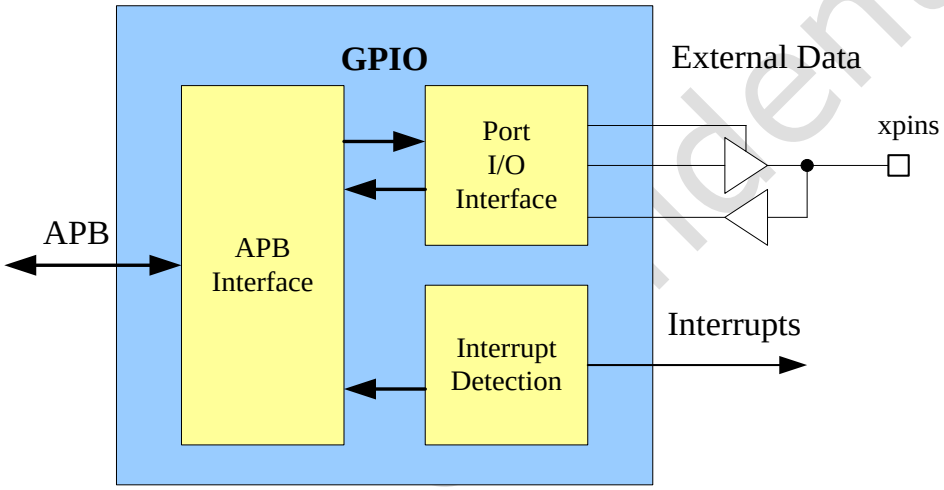


Fig. 18-1 GPIO Block Diagram

GPIO comprises with:

- APB Interface: The APB Interface implements the APB slave operation. Its data bus width is 32 bits
- Port I/O Interface: External data Interface to or from I/O pads
- Interrupt Detection: Interrupt interface to or from interrupt controller

18.3 Function Description

18.3.1 Control Mode

GPIO in PX3 SE is under software control mode, and the data and direction control for the signal are sourced from the data register (GPIO_SWPORTA_DR) and direction control register (GPIO_SWPORTA_DDR).
The direction of the external I/O pad is controlled by a write to the Porta data direction register (GPIO_SWPORTA_DDR). The data written to this memory-mapped register gets mapped onto an output signal, GPIO_PORTA_DDR, of the GPIO peripheral. This output signal controls the direction of an external I/O pad.
The data written to the Porta data register (GPIO_SWPORTA_DR) drives the output buffer of the I/O pad. External data are input on the external data signal, GPIO_EXT_PORTA. Reading the external signal register (GPIO_EXT_PORTA) shows the value on the signal, regardless of the direction. This register is read-only, meaning that it cannot be written from the APB software interface.

18.3.2 Operation

- Reading Data on External Signals

The data on the GPIO_EXT_PORTA external signal can always be read. The data on the external GPIO signal is read by an APB read of the memory-mapped register,

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GPIO_EXT_PORTA.
An APB read to the GPIO_EXT_PORTA register yields a value equal to that which is on the GPIO_EXT_PORTA signal.

- Accept External Interrupts

Port A can be programmed to accept external signals as interrupt sources on any of the bits of the signal. The type of interrupt is programmable with one of the following settings:

- Active-high and level
- Active-low and level
- Rising edge
- Falling edge

The interrupts can be masked by programming the GPIO_INTMASK register. The interrupt status can be read before masking (called raw status) and after masking.
The interrupts are combined into a single interrupt output signal, which has the same polarity as the individual interrupts. In order to mask the combined interrupt, all individual interrupts have to be masked. The single combined interrupt does not have its own mask bit.
Whenever Port A is configured for interrupts, the data direction must be set to Input. If the data direction register is reprogrammed to Output, then any pending interrupts are not lost. However, no new interrupts are generated.
For edge-detected interrupts, the ISR can clear the interrupt by writing a 1 to the GPIO_PORTA_EOI register for the corresponding bit to disable the interrupt. This write also clears the interrupt status and raw status registers. Writing to the GPIO_PORTA_EOI register has no effect on level-sensitive interrupts. If level-sensitive interrupts cause the processor to interrupt, then the ISR can poll the GPIO_INT_RAWSTATUS register until the interrupt source disappears, or it can write to the GPIO_INTMASK register to mask the interrupt before exiting the ISR. If the ISR exits without masking or disabling the interrupt prior to exiting, then the level-sensitive interrupt repeatedly requests an interrupt until the interrupt is cleared at the source.

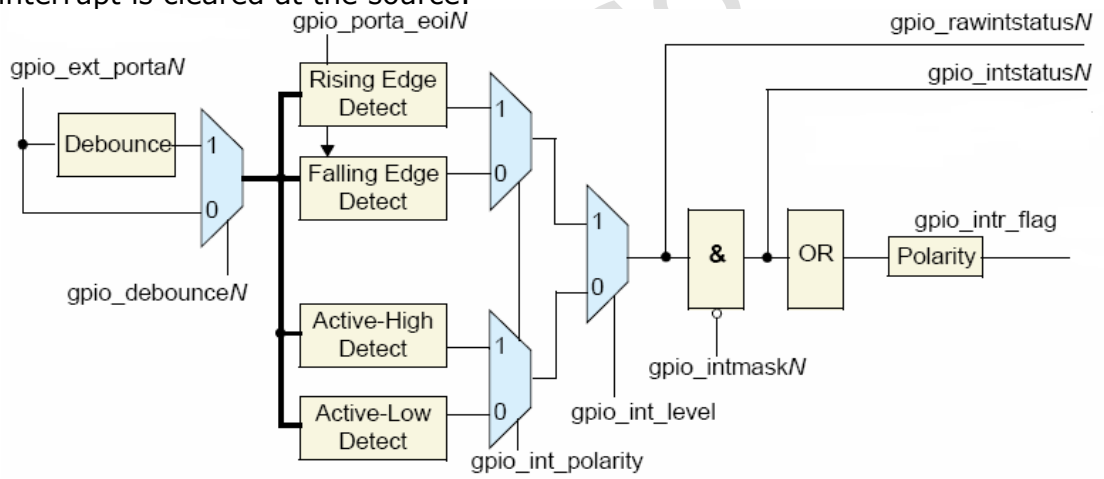


Fig. 18-2 GPIO Interrupt RTL Block Diagram

- Debounce operation

Port A has been configured to include the debounce capability interrupt feature. The external signal can be debounced to remove any spurious glitches that are less than one period of the external debouncing clock.
When input interrupt signals are debounced using a debounce clock (pclk), the signals must be active for a minimum of two cycles of the debounce clock to guarantee that they are registered. Any input pulse widths less than a debounce clock period are bounced. A pulse width between one and two debounce clock widths may or may not propagate, depending on its phase relationship to the debounce clock. If the input pulse spans two rising edges of the debounce clock, it is registered. If it spans only one rising edge, it is not registered.

- Synchronization of Interrupt Signals to the System Clock

Interrupt signals are internally synchronized to pclk. Synchronization to pclk must occur for edge-detect signals. With level-sensitive interrupts, synchronization is optional and under software control(GPIO_LS_SYNC).

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18.3.3 Programming Considerations

- Reading from an unused location or unused bits in a particular register always returns zeros. There is no error mechanism in the APB.
- Programming the GPIO registers for interrupt capability, edge-sensitive or level-sensitive interrupts, and interrupt polarity should be completed prior to enabling the interrupts on PortA in order to prevent spurious glitches on the interrupt lines to the interrupt controller.
- Writing to the interrupt clear register clears an edge-detected interrupt and has no effect on a level-sensitive interrupt.

18.3.4 GPIOs' hierarchy in the chip

GPIO1, GPIO2 are in cpu subsystem, GPIO3 is in peripheral subsystem, and GPIO0 is in alive subsystem.

18.4 Register Description

This section describes the control/status registers of the design. Software should read and write these registers using 32-bits accesses. There are 4 GPIOs (GPIO0 ~ GPIO3), and each of them has same register group. Therefore, 4 GPIOs' register groups have 4 different base addresses.

18.4.1 Registers Summary

Name	Offset	Size	Reset Value	Description
GPIO_SWPORTA_DR	0x0000	W	0x00000000	Port A data register
GPIO_SWPORTA_DDR	0x0004	W	0x00000000	Port A data direction register
GPIO_INTEN	0x0030	W	0x00000000	Interrupt enable register
GPIO_INTMASK	0x0034	W	0x00000000	Interrupt mask register
GPIO_INTTYPE_LEVEL	0x0038	W	0x00000000	Interrupt level register
GPIO_INT_POLARITY	0x003c	W	0x00000000	Interrupt polarity register
GPIO_INT_STATUS	0x0040	W	0x00000000	Interrupt status of port A
GPIO_INT_RAWSTATUS	0x0044	W	0x00000000	Raw Interrupt status of port A
GPIO_DEBOUNCE	0x0048	W	0x00000000	Debounce enable register
GPIO_PORTA_EOI	0x004c	W	0x00000000	Port A clear interrupt register
GPIO_EXT_PORTA	0x0050	W	0x00000000	Port A external port register
GPIO_LS_SYNC	0x0060	W	0x00000000	Level_sensitive synchronization enable register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

18.4.2 Detail Register Description

GPIO_SWPORTA_DR

Address: Operational Base + offset (0x0000)

PortA data register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	GPIO_swporta_dr Values written to this register are output on the I/O signals for Port A if the corresponding data direction bits for Port A are set to Output mode .The value read back is equal to the last value written to this register.

GPIO_SWPORTA_DDR

Address: Operational Base + offset (0x0004)

Port A data direction register

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	GPIO_swporta_ddr Values written to this register independently control the direction of the corresponding data bit in Port A. 1'b0: Input (default) 1'b1: Output

GPIO_INTEN
Address: Operational Base + offset (0x0030)
Interrupt enable register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	GPIO_int_en Allows each bit of Port A to be configured for interrupts. Whenever a 1 is written to a bit of this register, it configures the corresponding bit on Port A to become an interrupt; otherwise, Port A operates as a normal GPIO signal. Interrupts are disabled on the corresponding bits of Port A if the corresponding data direction register is set to Output. 1'b0: Configure Port A bit as normal GPIO signal (default) 1'b1: Configure Port A bit as interrupt

GPIO_INTMASK
Address: Operational Base + offset (0x0034)
Interrupt mask register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	GPIO_int_mask Controls whether an interrupt on Port A can create an interrupt for the interrupt controller by not masking it. Whenever a 1 is written to a bit in this register, it masks the interrupt generation capability for this signal; otherwise interrupts are allowed through. 1'b0: Interrupt bits are unmasked (default) 1'b1: Mask interrupt

GPIO_INTTYPE_LEVEL
Address: Operational Base + offset (0x0038)
Interrupt level register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	GPIO_inttype_level Controls the type of interrupt that can occur on Port A. 1'b0: Level-sensitive (default) 1'b1: Edge-sensitive

GPIO_INT_POLARITY
Address: Operational Base + offset (0x003c)
Interrupt polarity register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	GPIO_int_polarity Controls the polarity of edge or level sensitivity that can occur on input of Port A. 1'b0: Active-low (default) 1'b1: Active-high

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GPIO_INT_STATUS
Address: Operational Base + offset (0x0040)
Interrupt status of port A

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	GPIO_int_status Interrupt status of Port A

GPIO_INT_RAWSTATUS
Address: Operational Base + offset (0x0044)
Raw Interrupt status of port A

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	GPIO_int_rawstatus Raw interrupt of status of Port A (premasking bits)

GPIO_DEBOUNCE
Address: Operational Base + offset (0x0048)
Debounce enable register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	GPIO_debounce Controls whether an external signal that is the source of an interrupt needs to be debounced to remove any spurious glitches. Writing a 1 to a bit in this register enables the debouncing circuitry. A signal must be valid for two periods of an external clock before it is internally processed. 1'b0: No debounce (default) 1'b1: Enable debounce

GPIO_PORTA_EOI
Address: Operational Base + offset (0x004c)
Port A clear interrupt register

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	GPIO_porta_eoi Controls the clearing of edge type interrupts from Port A. When a 1 is written into a corresponding bit of this register, the interrupt is cleared. All interrupts are cleared when Port A is not configured for interrupts. 1'b0: No interrupt clear (default) 1'b1: Clear interrupt

GPIO_EXT_PORTA
Address: Operational Base + offset (0x0050)
Port A external port register

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	GPIO_ext_porta When Port A is configured as Input, then reading this location reads the values on the signal. When the data direction of Port A is set as Output, reading this location reads the data register for Port A.

GPIO_LS_SYNC
Address: Operational Base + offset (0x0060)

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Level_sensitive synchronization enable register

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	GPIO_ls_sync Writing a 1 to this register results in all level-sensitive interrupts being synchronized to pclk_intr. 1'b0: No synchronization to pclk_intr (default) 1'b1: Synchronize to pclk_intr

18.5 Interface description

Table 18-1 GPIO interface description

Module Pin	Direction	Pad Name	Descriptions
GPIO0 Interface			
GPIO0_porta[7:0]	I/O	GPIO0_A[7:0]	GRF_GPIO0A_IOMUX[15:0]=16'h0000
GPIO0_porta[15:8]	I/O	GPIO0_B[7:0]	GRF_GPIO0B_IOMUX[15:0]=16'h0000
GPIO0_porta[23:16]	I/O	GPIO0_C[7:0]	GRF_GPIO0C_IOMUX[15:0]=16'h0000
GPIO0_porta[31:24]	I/O	GPIO0_D[7:0]	GRF_GPIO0D_IOMUX[15:0]=16'h0000
GPIO1 Interface			
GPIO1_porta[7:0]	I/O	GPIO1_A[7:0]	GRF_GPIO1A_IOMUX[15:0]=16'h0000
GPIO1_porta[15:8]	I/O	GPIO1_B[7:0]	GRF_GPIO1B_IOMUX[15:0]=16'h0000
GPIO1_porta[23:16]	I/O	GPIO1_C[7:0]	GRF_GPIO1C_IOMUX[15:0]=16'h0000
GPIO1_porta[31:24]	I/O	GPIO1_D[7:0]	GRF_GPIO1D_IOMUX[15:0]=16'h0000
GPIO2 Interface			
GPIO2_porta[7:0]	I/O	GPIO2_A[7:0]	GRF_GPIO2A_IOMUX[15:0]=16'h0000
GPIO2_porta[15:8]	I/O	GPIO2_B[7:0]	GRF_GPIO2B_IOMUX[15:0]=16'h0000
GPIO2_porta[23:16]	I/O	GPIO2_C[7:0]	GRF_GPIO2C_IOMUX[7:0]=8'h00 GRF_GPIO2C_IOMUX2[15:0]=16'h0000
GPIO2_porta[31:24]	I/O	GPIO2_D[7:0]	GRF_GPIO2D_IOMUX[15:0]=16'h0000
GPIO3 Interface			
GPIO3_porta[7:0]	I/O	GPIO3_A[7:0]	GRF_GPIO3A_IOMUX[15:0]=16'h0000
GPIO3_porta[15:8]	I/O	GPIO3_B[7:0]	GRF_GPIO3B_IOMUX[15:0]=16'h0000
GPIO3_porta[23:16]	I/O	GPIO3_C[7:0]	GRF_GPIO3C_IOMUX[15:0]=16'h0000
GPIO3_porta[31:24]	I/O	GPIO3_D[7:0]	GRF_GPIO3D_IOMUX[15:0]=16'h0000

18.6 Application Notes

Each GPIO controls 32 bits output data and the corresponding directions of external 32 I/O pads. It also can read back the 32 bits data on external pads using memory-mapped registers. So each bit values written to GPIO registers independently control the data and the direction of corresponding I/O pad .And the valid value of x in square brackets is 0 to 31.

- Steps to set GPIO's direction
  - Write GPIO_SWPORT_DDR[x] as 1 to set this GPIO as output direction and Write GPIO_SWPORT_DDR[x] as 0 to set this GPIO as input direction.
  - Default GPIO's direction is input direction.
- Steps to set GPIO's direction
  - Write GPIO_SWPORT_DDR[x] as 1 to set this GPIO as output direction.
  - Write GPIO_SWPORT_DR[x] as v to set this GPIO's value.
- Steps to get GPIO's level
  - Write GPIO_SWPORT_DDR[x] as 0 to set this GPIO as input direction.

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- Read from GPIO_EXT_PORT[x] to get GPIO's value

- Steps to set GPIO as interrupt source
  - Write GPIO_SWPORT_DDR[x] as 0 to set this GPIO as input direction.
  - Write GPIO_INTTYPE_LEVEL[x] as v1 and write GPIO_INT_POLARITY[x] as v2 to set interrupt type
  - Write GPIO_INTEN[x] as 1 to enable GPIO's interrupt

Note: Please switch IOMUX to GPIO mode first!

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Chapter 19 I2C Interface

19.1 Overview

The Inter-Integrated Circuit (I2C) is a two wired (SCL and SDA), bi-directional serial bus that provides an efficient and simple method of information exchange between devices. This I2C bus controller supports master mode acting as a bridge between AMBA protocol and generic I2C bus system.
I2C Controller supports the following features:

- AMBA APB slave interface
- Supports master mode of I2C bus
- Software programmable clock frequency and transfer rate up to 400Kbit/sec
- Supports 7 bits and 10 bits addressing modes
- Interrupt or polling driven multiple bytes data transfer
- Clock stretching and wait state generation
- Four I2Cs(I2C0/I2C1/I2C2/I2C3) in peripheral sub-system

19.2 Block Diagram

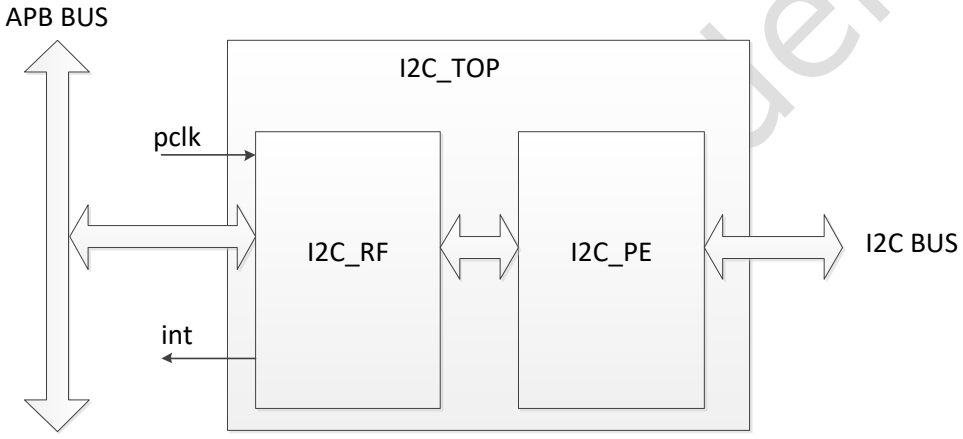


Fig. 19-1 I2C architecture

19.2.1 I2C_RF

I2C_RF module is used to control the I2C controller operation by the host with APB interface. It implements the register set and the interrupt functionality. The CSR component operates synchronously with the pclk clock.

19.2.2 I2C_PE

I2C_PE module implements the I2C master operation for transmit data to and receive data from other I2C devices. The I2C master controller operates synchronously with the clk_i2c.

19.2.3 I2C_TOP

I2C_TOP module is the top module of the I2C controller.

19.3 Function Description

This chapter provides a description about the functions and behavior under various conditions.
The I2C controller supports only Master function. It supports the 7-bits/10-bits addressing mode and support general call address. The maximum clock frequency and transfer rate can be up to 400Kbit/sec.
The operations of I2C controller is divided to 2 parts and described separately: initialization and master mode programming.

19.3.1 Initialization

The I2C controller is based on AMBA APB bus architecture and usually is part of a SOC. So before I2C operates, some system setting and configuration must be conformed, which includes:

- I2C interrupt connection type: CPU interrupt scheme should be considered. If the I2C

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interrupt is connected to extra Interrupt Controller module, we need to decide the INTC vector.

- I2C Clock Rate: The I2C controller uses the APB clock as the working clock. The APB clock will determine the I2C bus clock. The correct register setting is subject to the system requirement.

19.3.2 Master Mode Programming

- SCL Clock
  When the I2C controller is programmed in Master mode, the SCL frequency is determined by I2C_CLKDIV register. The SCL frequency is calculated by the following formula:
  SCL Divisor = 8*(CLKDIVL + 1 + CLKDIVH + 1)
  SCL = clk_i2c/ SCLK Divisor

- Data Receiver Register Access
  When the I2C controller received MRXCNT bytes data, CPU can get the data through register RXDATA0 ~ RXDATA7. The controller can receive up to 32 bytes' data in one transaction.
  When MRXCNT register is written, the I2C controller will start to drive SCL to receive data.

- Transmit Transmitter Register
  Data to transmit are written to TXDATA0~7 by CPU. The controller can transmit up to 32 bytes' data in one transaction. The lower byte will be transmitted first.
  When MTXCNT register is written, the I2C controller will start to transmit data.

- Start Command
  Write 1 to I2C_CON[3], the controller will send I2C start command.

- Stop Command
  Write 1 to I2C_CON[4], the controller will send I2C stop command

- I2C Operation mode
  There are four i2c operation modes.
  - When I2C_CON[2:1] is 2'b00, the controller transmit all valid data in TXDATA0~TXDATA7 byte by byte. The controller will transmit lower byte first.
  - When I2C_CON[2:1] is 2'b01,the controller will transmit device address in MRXADDR first (Write/Read bit = 0) and then transmit device register address in MRXRADDR. After that, the controller will assert restart signal and resend MRXADDR (Write/Read bit = 1). At last, the controller enter receive mode.
  - When I2C_CON[2:1] is 2'b10, the controller is in receive mode, it will trigger clock to read MRXCNT byte data.
  - When I2C_CON[2:1] is 2'b11, the controller will transmit device address in MRXADDR first (Write/Read bit = 1) and then transmit device register address in MRXRADDR . After that, the controller will assert restart signal and resend MRXADDR (Write/Read bit = 1). At last, the controller enter receive mode.

- Read/Write Command
  - When I2C_OPMODE(I2C_CON[2:1]) is 2'b01 or 2'b11, the Read/Write command bit is decided by controller itself.
  - In RX only mode (I2C_CON[2:1] is 2'b10), the Read/Write command bit is decided by MRXADDR[0].
  - In TX only mode (I2C_CON[[2:1] is 2'b00), the Read/Write command bit is decided by TXDATA[0].

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- Master Interrupt Condition
  There are 7 interrupt bits in I2C_ISR register related to master mode.
  - Byte transmitted finish interrupt (Bit 0): The bit is asserted when Master completed transmitting a byte.
  - Byte received finish interrupt (Bit 1): The bit is asserted when Master completed receiving a byte.
  - MTXCNT bytes data transmitted finish interrupt (Bit 2): The bit is asserted when Master completed transmitting MTXCNT bytes.
  - MRXCNT bytes data received finish interrupt (Bit 3): The bit is asserted when Master completed receiving MRXCNT bytes.
  - Start interrupt (Bit 4): The bit is asserted when Master finished asserting start command to I2C bus.
  - Stop interrupt (Bit 5): The bit is asserted when Master finished asserting stop command to I2C bus.
  - NAK received interrupt (Bit 6): The bit is asserted when Master received a NAK handshake.

- Last byte acknowledge control
  - If I2C_CON[5] is 1, the I2C controller will transmit NAK handshake to slave when the last byte received in RX only mode.
  - If I2C_CON[5] is 0, the I2C controller will transmit ACK handshake to slave when the last byte received in RX only mode.

- How to handle NAK handshake received
  - If I2C_CON[6] is 1, the I2C controller will stop all transactions when NAK handshake received. And the software should take responsibility to handle the problem.
  - If I2C_CON[6] is 0, the I2C controller will ignore all NAK handshake received.

- I2C controller data transfer waveform
  - Bit transferring
    - Data Validity
      The SDA line must be stable during the high period of SCL, and the data on SDA line can only be changed when SCL is in low state.

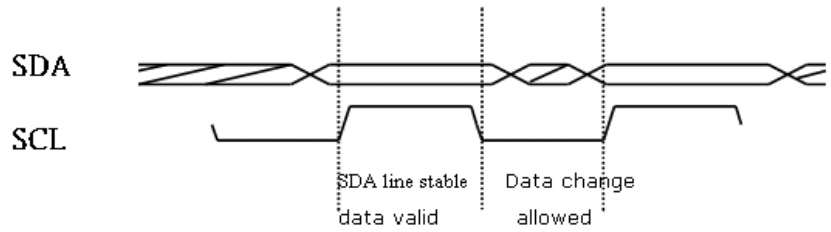


Fig. 19-2 I2C DATA Validity

    - START and STOP conditions
      START condition occurs when SDA goes low while SCL is in high period. STOP condition is generated when SDA line goes high while SCL is in high state.

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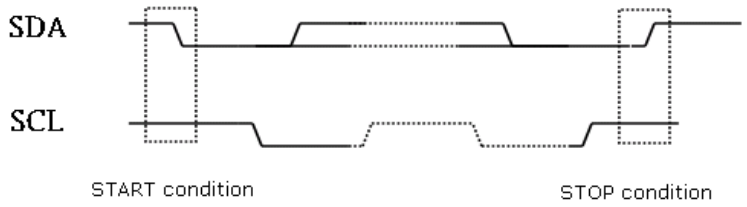


Fig. 19-3 I2C Start and stop conditions

- Data transfer
  - Acknowledge

After a byte of data transferring (clocks labeled as 1~8), in 9th clock the receiver must assert an ACK signal on SDA line, if the receiver pulls SDA line to low, it means "ACK", on the contrary, it's "NOT ACK".

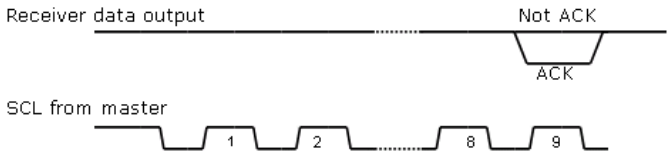


Fig. 19-4 I2C Acknowledge

- Byte transfer

The master own I2C bus might initiate multi byte to transfer to a slave. The transfer starts from a "START" command and ends in a "STOP" command. After every byte transfer, the receiver must reply an ACK to transmitter.

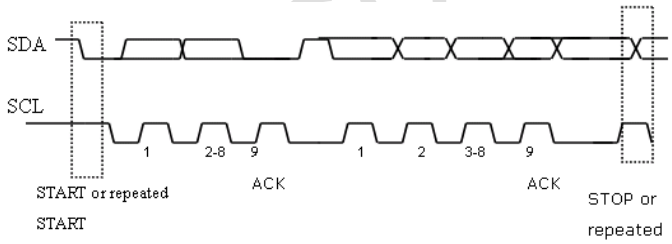


Fig. 19-5 I2C byte transfer

19.4 Register Description

19.4.1 Registers Summary

Name	Offset	Size	Reset Value	Description
I2C_CON	0x0000	W	0x00000000	I2C Control Register
I2C_CLKDIV	0x0004	W	0x00000001	I2C Clock Divider Register
I2C_MRXADDR	0x0008	W	0x00000000	I2C Slave Address Register For Master Receive Mode
I2C_MRXRADDR	0x000c	W	0x00000000	I2C Slave Register Address Register For Master Receive Mode
I2C_MTXCNT	0x0010	W	0x00000000	I2C Master Transmit Count Register
I2C_MRXCNT	0x0014	W	0x00000000	I2C Master Receive Count Register

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Name	Offset	Size	Reset Value	Description
I2C_IEN	0x0018	W	0x00000000	I2C Interrupt Enable Register
I2C_IPD	0x001c	W	0x00000000	I2C Interrupt Pending Register
I2C_FCNT	0x0020	W	0x00000000	I2C Finished Count Register
I2C_TXDATA0	0x0100	W	0x00000000	I2C Transmit Data Register 0
I2C_TXDATA1	0x0104	W	0x00000000	I2C Transmit Data Register 1
I2C_TXDATA2	0x0108	W	0x00000000	I2C Transmit Data Register 2
I2C_TXDATA3	0x010c	W	0x00000000	I2C Transmit Data Register 3
I2C_TXDATA4	0x0110	W	0x00000000	I2C Transmit Data Register 4
I2C_TXDATA5	0x0114	W	0x00000000	I2C Transmit Data Register 5
I2C_TXDATA6	0x0118	W	0x00000000	I2C Transmit Data Register 6
I2C_TXDATA7	0x011c	W	0x00000000	I2C Transmit Data Register 7
I2C_RXDATA0	0x0200	W	0x00000000	I2C Receive Data Register 0
I2C_RXDATA1	0x0204	W	0x00000000	I2C Receive Data Register 1
I2C_RXDATA2	0x0208	W	0x00000000	I2C Receive Data Register 2
I2C_RXDATA3	0x020c	W	0x00000000	I2C Receive Data Register 3
I2C_RXDATA4	0x0210	W	0x00000000	I2C Receive Data Register 4
I2C_RXDATA5	0x0214	W	0x00000000	I2C Receive Data Register 5
I2C_RXDATA6	0x0218	W	0x00000000	I2C Receive Data Register 6
I2C_RXDATA7	0x021c	W	0x00000000	I2C Receive Data Register 7

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

19.4.2 Detail Register Description

I2C_CON

Address: Operational Base + offset (0x0000)

I2C Control Register

Bit	Attr	Reset Value	Description
31:7	RO	0x0000	version Version information
6	RW	0x0	act2nak Operation when NAK handshake is received 1'b0: ignored 1'b1: stop transaction
5	RW	0x0	ack Last byte acknowledge control in master receive mode 1'b0: ACK 1'b1: NAK
4	RW	0x0	stop enable When this bit is written to 1，I2C will generate stop signal. It cleared itself when stop operation ends.
3	RW	0x0	start enable When this bit is written to 1，I2C will generate start signal. It cleared itself when start operation ends.

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Bit	Attr	Reset Value	Description
2:1	RW	0x0	i2c_mode I2C mode select. 2'b00: transmit only 2'b01: transmit address (device + register address) --> restart --> transmit address -> receive only 2'b10: receive only 2'b11: transmit address (device + register address, write/read bit is 1) --> restart --> transmit address (device address) --> receive data
0	RW	0x0	i2c_en I2C module enable 1'b0: not enable 1'b1: enable

I2C_CLKDIV
Address: Operational Base + offset (0x0004)
I2C Clock Divider Register

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	CLKDIVH SCL high level clock count T(SCL_HIGH) = Tclk_i2c * (CLKDIVH + 1) * 8
15:0	RW	0x0001	CLKDIVL SCL low level clock count T(SCL_LOW) = Tclk_i2c * (CLKDIVL + 1) * 8

I2C_MRXADDR
Address: Operational Base + offset (0x0008)
I2C Slave Address Register For Master Receive Mode

Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved
26	RW	0x0	addhvld Address high byte valid indication 1'b0: invalid 1'b1: valid
25	RW	0x0	addmvld Address middle byte valid indication 1'b0: invalid 1'b1: valid
24	RW	0x0	addlvld Address low byte valid indication 1'b0: invalid 1'b1: valid
23:0	RW	0x000000	saddr Master address register. The lowest bit indicate write or read.

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I2C_MRXRADDR
Address: Operational Base + offset (0x000c)
I2C Slave Register Address Register For Master Receive Mode

Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved
26	RW	0x0	sraddhvld Address high byte valid indication 1'b0: invalid 1'b1: valid
25	RW	0x0	sraddmvld Address middle byte valid indication 1'b0: invalid 1'b1: valid
24	RW	0x0	sraddlvld Address low byte valid indication 1'b0: invalid 1'b1: valid
23:0	RW	0x000000	sraddr Slave register address accessed

I2C_MTXCNT
Address: Operational Base + offset (0x0010)
I2C Master Transmit Count Register

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5:0	RW	0x00	mtxcnt Master transmit count

I2C_MRXCNT
Address: Operational Base + offset (0x0014)
I2C Master Receive Count Register

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5:0	RW	0x00	mrxcnt Master receive count

I2C_IEN
Address: Operational Base + offset (0x0018)
I2C Interrupt Enable Register

Bit	Attr	Reset Value	Description
31:7	RO	0x0	reserved
6	RW	0x0	nakrcvien NAK handshake received interrupt enable 1'b0: disable 1'b1: enable

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Bit	Attr	Reset Value	Description
5	RW	0x0	stopien Stop operation finished interrupt enable 1'b0: disable 1'b1: enable
4	RW	0x0	startien Start operation finished interrupt enable 1'b0: disable 1'b1: enable
3	RW	0x0	mbrfien MRXCNT data received finished interrupt enable 1'b0: disable 1'b1: enable
2	RW	0x0	mbtfien MTXCNT data transfer finished interrupt enable 1'b0: disable 1'b1: enable
1	RW	0x0	brfien Byte receive finished interrupt enable 1'b0: disable 1'b1: enable
0	RW	0x0	btfien Byte transmit finished interrupt enable 1'b0: disable 1'b1: enable

I2C_IPD
Address: Operational Base + offset (0x001c)
I2C Interrupt Pending Register

Bit	Attr	Reset Value	Description
31:7	RO	0x0	reserved
6	W1C	0x0	nakrcvipd NAK handshake received interrupt pending bit 1'b0: no interrupt available 1'b1: NAK handshake received interrupt appear, write 1 to clear
5	W1C	0x0	stopipd Stop operation finished interrupt pending bit 1'b0: no interrupt available 1'b1: stop operation finished interrupt appear, write 1 to clear
4	W1C	0x0	startipd Start operation finished interrupt pending bit 1'b0: no interrupt available 1'b1: start operation finished interrupt appear, write 1 to clear

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Bit	Attr	Reset Value	Description
3	W1C	0x0	mbrfipd MRXCNT data received finished interrupt pending bit 1'b0: no interrupt available 1'b1: MRXCNT data received finished interrupt appear, write 1 to clear
2	W1C	0x0	mbtfipd MTXCNT data transfer finished interrupt pending bit 1'b0: no interrupt available 1'b1: MTXCNT data transfer finished interrupt appear, write 1 to clear
1	W1C	0x0	brfipd Byte receive finished interrupt pending bit 1'b0: no interrupt available 1'b1: byte receive finished interrupt appear, write 1 to clear
0	W1C	0x0	btfipd Byte transmit finished interrupt pending bit 1'b0: no interrupt available 1'b1: byte transmit finished interrupt appear, write 1 to clear

I2C_FCNT
Address: Operational Base + offset (0x0020)
I2C Finished Count Register

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5:0	RO	0x00	fcnt Finished count. The count of data which has been transmitted or received. Used for debug purpose.

I2C_TXDATA0
Address: Operational Base + offset (0x0100)
I2C Transmit Data Register 0

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	txdata0 Data0 to be transmitted

I2C_TXDATA1
Address: Operational Base + offset (0x0104)
I2C Transmit Data Register 1

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	txdata1 Data1 to be transmitted

I2C_TXDATA2
Address: Operational Base + offset (0x0108)

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I2C Transmit Data Register 2

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	txdata2 Data2 to be transmitted

I2C_TXDATA3
Address: Operational Base + offset (0x010c)
I2C Transmit Data Register 3

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	txdata3 Data3 to be transmitted

I2C_TXDATA4
Address: Operational Base + offset (0x0110)
I2C Transmit Data Register 4

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	txdata4 Data4 to be transmitted

I2C_TXDATA5
Address: Operational Base + offset (0x0114)
I2C Transmit Data Register 5

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	txdata5 Data5 to be transmitted

I2C_TXDATA6
Address: Operational Base + offset (0x0118)
I2C Transmit Data Register 6

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	txdata6 Data6 to be transmitted

I2C_TXDATA7
Address: Operational Base + offset (0x011c)
I2C Transmit Data Register 7

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	txdata7 Data7 to be transmitted

I2C_RXDATA0
Address: Operational Base + offset (0x0200)
I2C Receive Data Register 0

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rxdata0 Data0 received

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I2C_RXDATA1
Address: Operational Base + offset (0x0204)
I2C Receive Data Register 1

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rxdata1 Data1 received

I2C_RXDATA2
Address: Operational Base + offset (0x0208)
I2C Receive Data Register 2

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rxdata2 Data2 received

I2C_RXDATA3
Address: Operational Base + offset (0x020c)
I2C Receive Data Register 3

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rxdata3 Data3 received

I2C_RXDATA4
Address: Operational Base + offset (0x0210)
I2C Receive Data Register 4

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rxdata4 Data4 received

I2C_RXDATA5
Address: Operational Base + offset (0x0214)
I2C Receive Data Register 5

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rxdata5 Data5 received

I2C_RXDATA6
Address: Operational Base + offset (0x0218)
I2C Receive Data Register 6

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rxdata6 Data6 received

I2C_RXDATA7
Address: Operational Base + offset (0x021c)

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I2C Receive Data Register 7

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rxdata7 Data7 received

19.5 Interface Description

Table 19-1 I2C0 Interface Description

Module Pin	Direction	Pad Name	IOMUX
i2c0_sda	I/O	IO_I2C0pmusda_GPIO0a1	GRF_GPIO0A_IOMUX[2]=1'b1
i2c0_scl	I/O	IO_I2C0pmuscl_GPIO0a0	GRF_GPIO0A_IOMUX[0]=1'b1

Table 19-2 I2C1 Interface Description

Module Pin	Direction	Pad Name	IOMUX
i2c1_sda	I/O	IO_I2C1tpsda_GPIO0a3	GRF_GPIO0A_IOMUX[6]=1'b1
i2c1_scl	I/O	IO_I2C1tpscl_GPIO0a2	GRF_GPIO0A_IOMUX[4]=1'b1

Table 19-3 I2C2 Interface Description

Module Pin	Direction	Pad Name	IOMUX
i2c2_sda	I/O	IO_LCD0d18_EBCgdrl_I2C2sda_GPIO2c4	GRF_GPIO2C_IOMUX[9:8]=2'b11
i2c2_scl	I/O	IO_LCD0d19_EBCsdshr_I2C2scl_GPIO2c5	GRF_GPIO2C_IOMUX[11:10]=2'b11

Table 19-4 I2C3 Interface Description

Module Pin	Direction	Pad Name	IOMUX
i2c3_sda	I/O	IO_I2C3cifsda_HDMIddcsda_GPIO0a7	GRF_GPIO0A_IOMUX[15:14]=2'b01
i2c3_scl	I/O	IO_I2C3cifscl_HDMIddcscl_GPIO0a6	GRF_GPIO0A_IOMUX[13:12]=2'b01

19.6 Application Notes

The I2C controller core operation flow chart below is to describe how the software configures and performs an I2C transaction through this I2C controller core. Descriptions are divided into 3 sections, transmit only mode, receive only mode, and mix mode. Users are strongly advised to follow them.

- Transmit only mode (I2C_CON[1:0]=2'b00)

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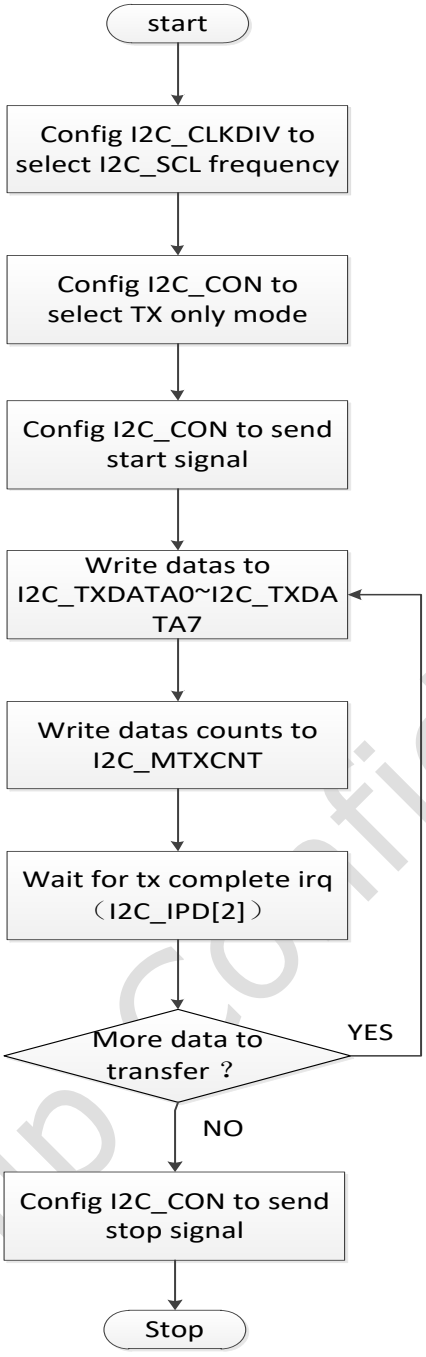


Fig. 19-6 I2C Flow chat for transmit only mode

- Receive only mode (I2C_CON[1:0]=2'b10)

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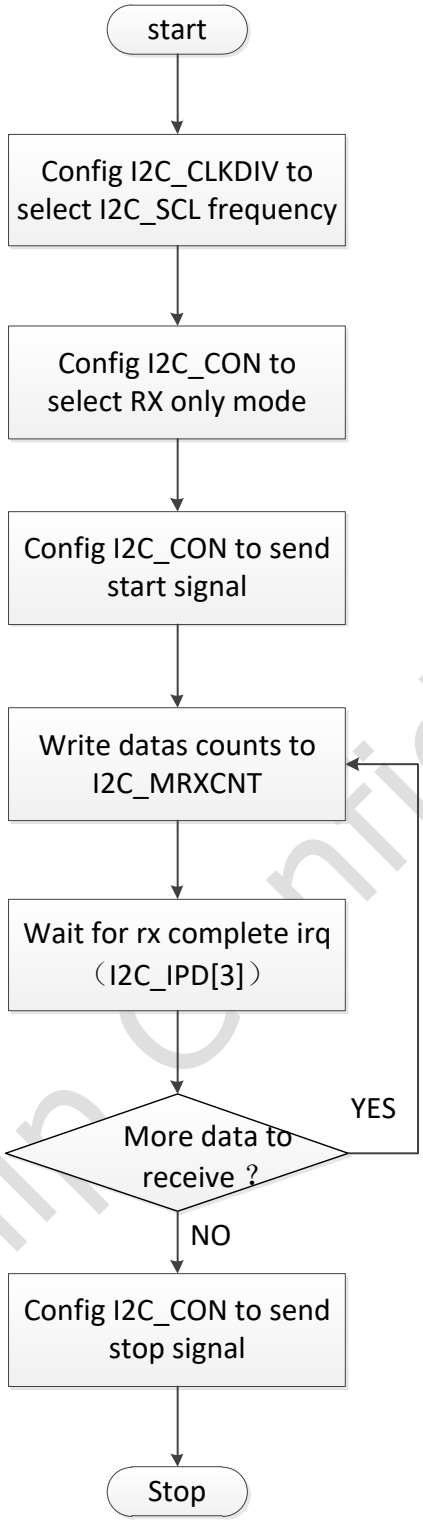


Fig. 19-7 I2C Flow chat for receive only mode

- Mix mode (I2C_CON[1:0]=2'b01 or I2C_CON[1:0]=2'b11)

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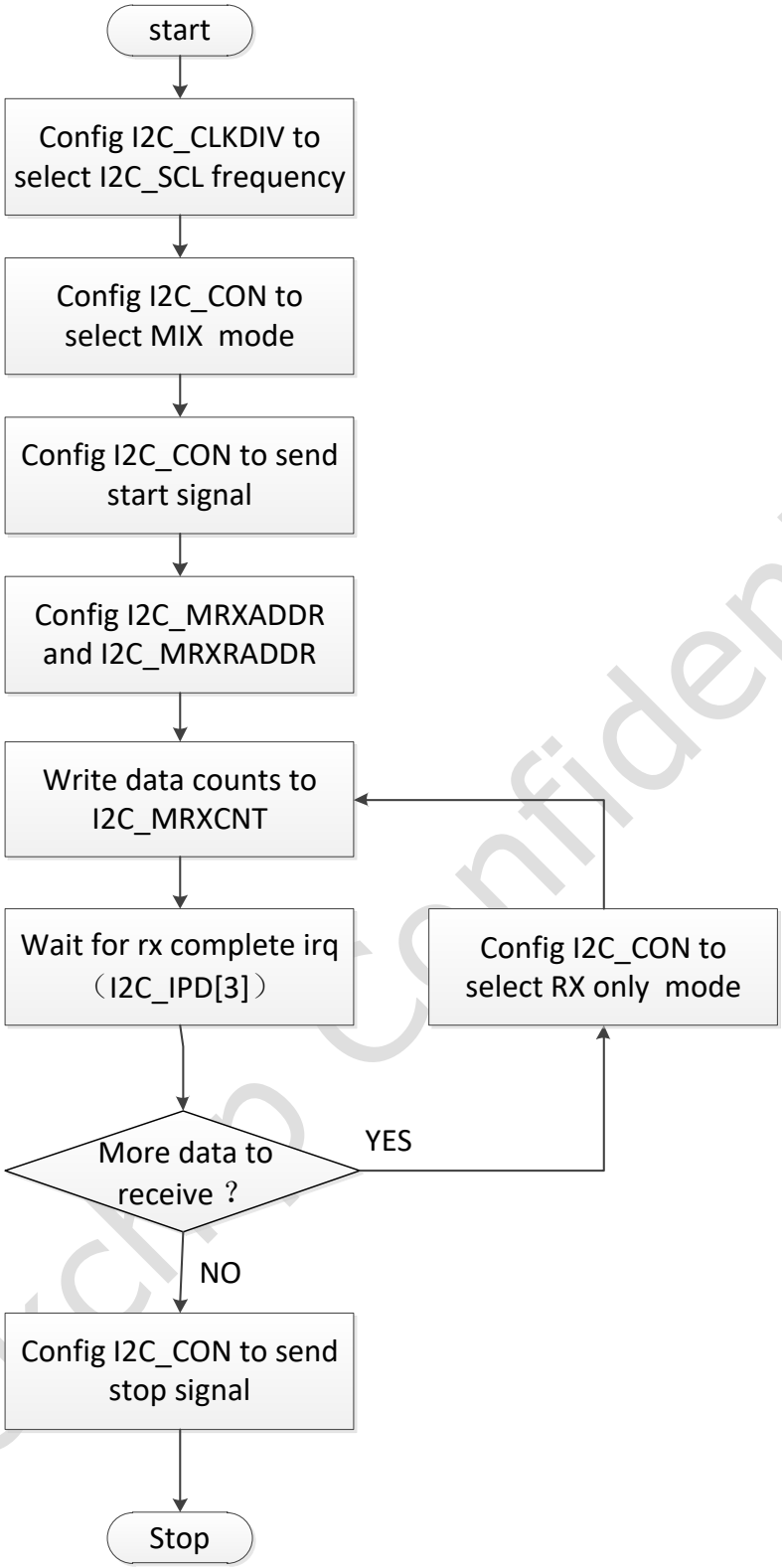


Fig. 19-8 I2C Flow chat for mix mode

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Chapter 20 I2S 8-channel

20.1 Overview

The I2S/PCM controller is designed for interfacing between the AHB bus and the I2S bus. The I2S bus (Inter-IC sound bus) is a serial link for digital audio data transfer between devices in the system and be invented by Philips Semiconductor. Now it is widely used by many semiconductor manufacturers.
Devices often use the I2S bus are ADC, DAC, DSP, CPU, etc. With the I2S interface, we can connect audio devices and the embedded SoC platform together and provide an audio interface solution for the system.

20.1.1 Features

Not only I2S but also PCM mode surround audio output (up to 7.1channel) and stereo input are supported in I2S/PCM controller.

- Support five internal 32-bit wide and 32-location deep FIFOs, four for transmitting and one for receiving audio data
- Support AHB bus interface
- Support 16 ~ 32 bits audio data transfer
- Support master and slave mode
- Support DMA handshake interface and configurable DMA water level
- Support transmit FIFO empty, underflow, receive FIFO full, overflow interrupt and all interrupts can be masked
- Support configurable water level of transmit FIFO empty and receive FIFO full interrupt
- Support combine interrupt output
- Support 2,4,6,8 channels audio transmitting in I2S and PCM mode
- Support 2 channels audio receiving in I2S and PCM mode
- Support up to 192kHz sample rate
- Support I2S normal, left and right justified mode serial audio data transfer
- Support PCM early, late1, late2, late3 mode serial audio data transfer
- Support MSB or LSB first serial audio data transfer
- Support 16 to 31 bit audio data left or right justified in 32-bit wide FIFO
- Support two 16-bit audio data store together in one 32-bit wide location
- Support 3 independent LRCK signals, one for receiving and two for transmitting audio data
- Support configurable SCLK and LRCK polarity
- Support SCLK is equivalent to MCLK divided by an even number range from 2 to 64 in master mode

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20.2 Block Diagram

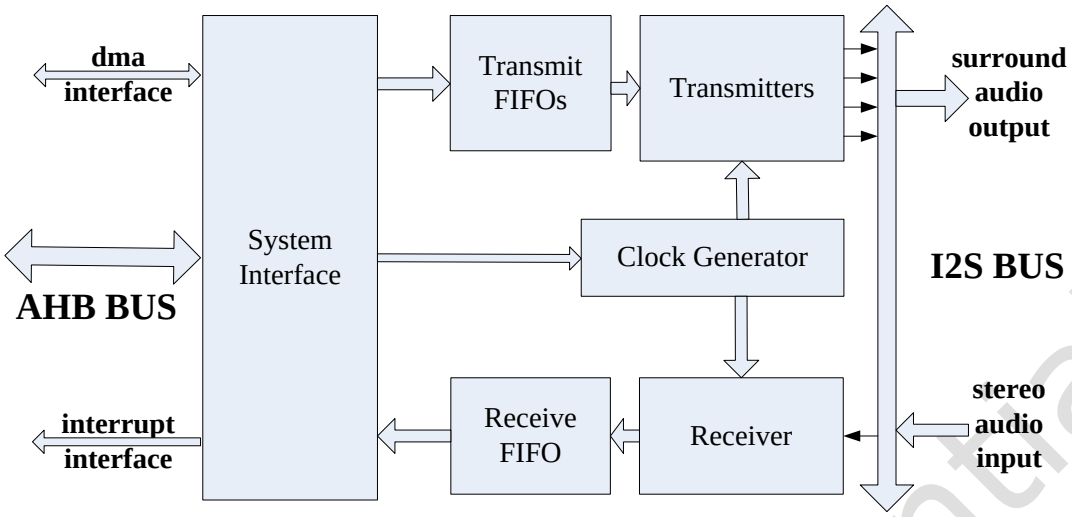


Fig. 20-1 I2S/PCM controller (8 channel) Block Diagram

System Interface

The system interface implements the AHB slave operation. It contains not only control registers of transmitters and receiver inside but also interrupt and DMA handshake interface.

Clock Generator

The Clock Generator implements clock generation function. The input source clock to the module is MCLK_I2S, and by the divider of the module, the clock generator generates SCLK and LRCK to transmitter and receiver.

Transmitters

The Transmitters implement transmission operation. The transmitters can act as either master or slave, with I2S or PCM mode surround (up to 7.1 channel) serial audio interface.

Receiver

The Receiver implements receive operation. The receiver can act as either master or slave, with I2S or PCM mode stereo serial audio interface.

Transmit FIFOs

The Transmit FIFOs are the buffer to store transmitted audio data. Each of the size of the four FIFOs is 32bits x 32.

Receive FIFO

The Receive FIFO is the buffer to store received audio data. The size of the FIFO is 32bits x 32.

20.3 Function description

In the I2S/PCM controller, there are four conditions: transmitter-master & receiver-master; transmitter-master & receiver-slave; transmitter-slave & receiver-master; transmitter-slave & receiver-slave.

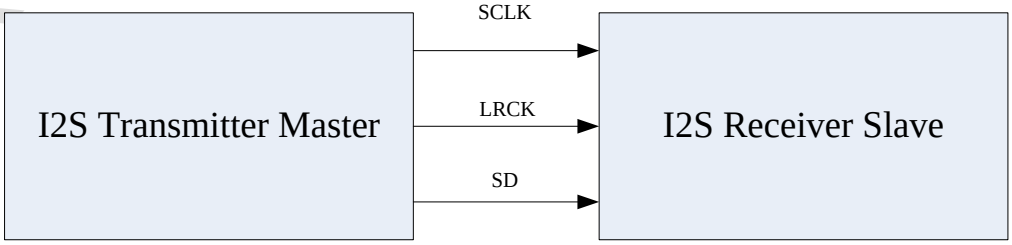


Fig. 20-2 I2S transmitter-master & receiver-slave condition

When transmitter acts as a master, it sends all signals to receiver (slave), and CPU control when to send clock and data to the receiver. When acting as a slave, SD signal still goes from transmitter to receiver, but SCLK and LRCK signals are from receiver (master) to transmitter. Based on three interface specifications, transmitting data should be ready

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before transmitter receives SCLK and LRCK signals. CPU should know when the receiver to initialize a transaction and when to send data.

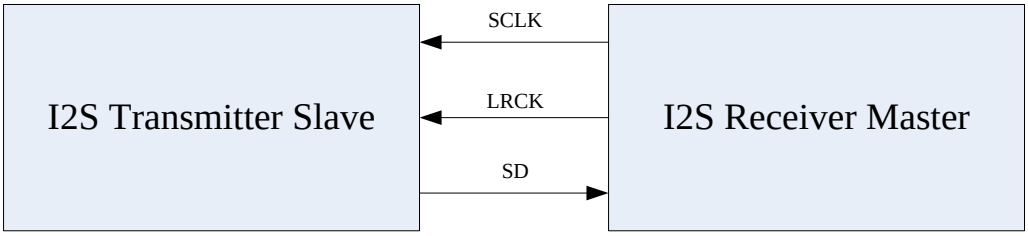


Fig. 20-3 I2S transmitter-slave& receiver-master condition

When the receiver acts as a master, it sends SCLK and LRCK signals to the transmitter (slave) and receives serial data. So CPU must tell the transmitter when to start a transaction for it to prepare transmitting data then start a transfer and send clock and channel-select signals. When the receiver acts as a slave, CPU should only do initial setting and wait for all signals and then start reading data.

Before transmitting or receiving data, CPU need do initial setting to the I2S register. These includes CPU settings, I2S interface registers settings, and maybe the embedded SoC platform settings. These registers must be set before starting data transfer.

20.3.1 I2S normal mode

This is the waveform of I2S normal mode. For LRCK (i2s_lrck_rx/i2s_lrck_tx0) signal, it goes low to indicate left channel and high to right channel. For SD (i2s_sdo0, i2s_sdo1, i2s_sdo2, i2s_sdo3, i2s_sdi) signal, it transfers MSB or LSB first and sends the first bit one SCLK clock cycle after LRCK changes. The range of SD signal width is from 16 to 32bits.

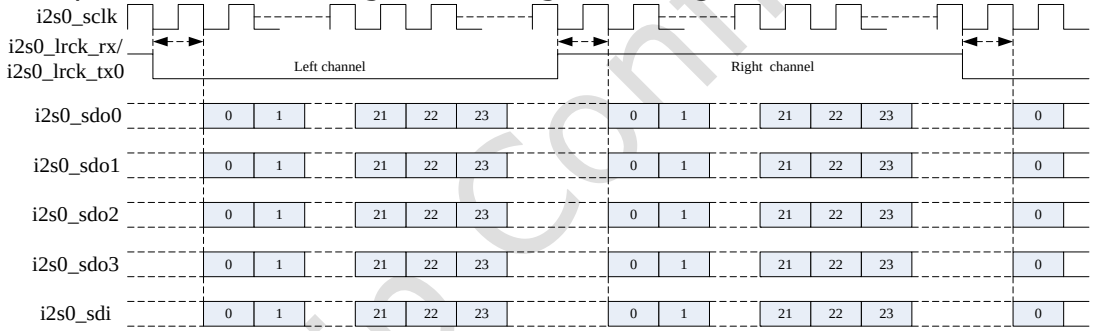


Fig. 20-4 I2S normal mode timing format

20.3.2 I2S left justified mode

This is the waveform of I2S left justified mode. For LRCK (i2s_lrck_rx / i2s_lrck_tx0) signal, it goes high to indicate left channel and low to right channel. For SD (i2s_sdo0, i2s_sdo1, i2s_sdo2, i2s_sdo3, i2s_sdi) signal, it transfers MSB or LSB first and sends the first bit at the same time when LRCK changes. The range of SD signal width is from 16 to 32bits.

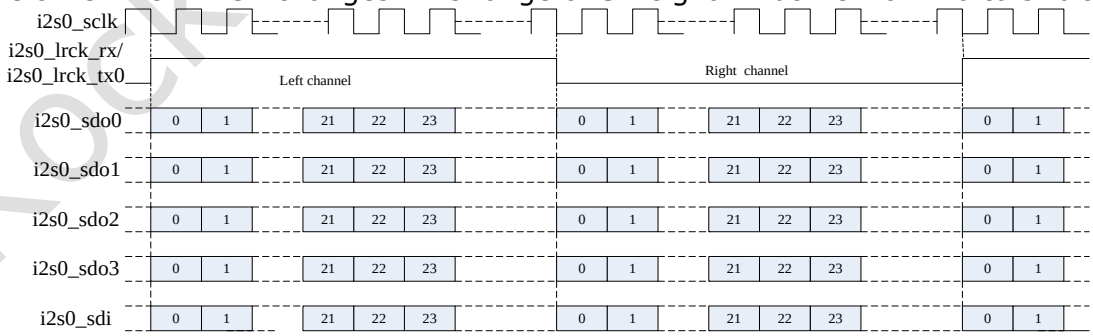


Fig. 20-5 I2S left justified mode timing format

20.3.3 I2S right justified mode

This is the waveform of I2S right justified mode. For LRCK (i2s_lrck_rx / i2s_lrck_tx0) signal, it goes high to indicate left channel and low to right channel. For SD (i2s_sdo0, i2s_sdo1, i2s_sdo2, i2s_sdo3, i2s_sdi) signal, it transfers MSB or LSB first; but different from I2S normal or left justified mode, its data is aligned to last bit at the edge of the LRCK signal. The range of SD signal width is from 16 to 32bits.

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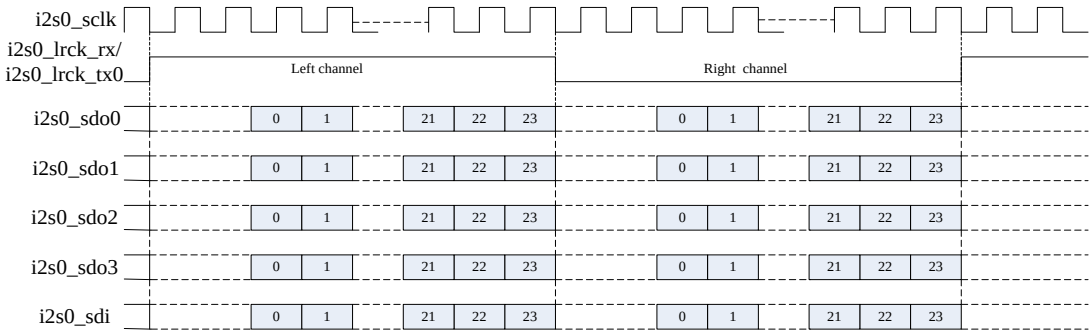


Fig. 20-6 I2S right justified mode timing format

20.3.4 PCM early mode

This is the waveform of PCM early mode. For LRCK (i2s_lrck_rx / i2s_lrck_tx0) signal, it goes high to indicate the start of a group of audio channels. For SD (i2s_sdo0, i2s_sdi) signal, it transfers MSB or LSB first and sends the first bit at the same time when LRCK goes high. The range of SD signal width is from 16 to 32bits.

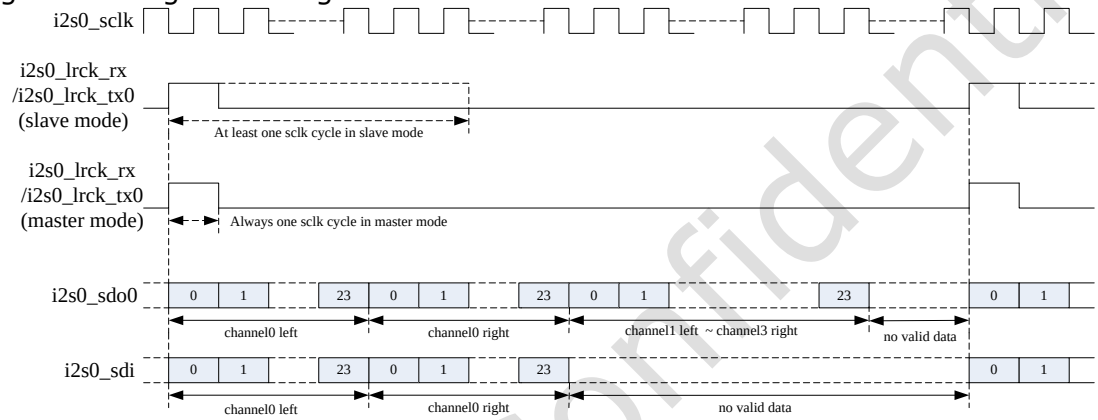


Fig. 20-7 PCM early mode timing format

20.3.5 PCM late1 mode

This is the waveform of PCM early mode. For LRCK (i2s_lrck_rx / i2s_lrck_tx0) signal, it goes high to indicate the start of a group of audio channels. For SD (i2s_sdo0, i2s_sdi) signal, it transfers MSB or LSB first and sends the first bit one SCLK clock cycle after LRCK goes high. The range of SD signal width is from 16 to 32bits.

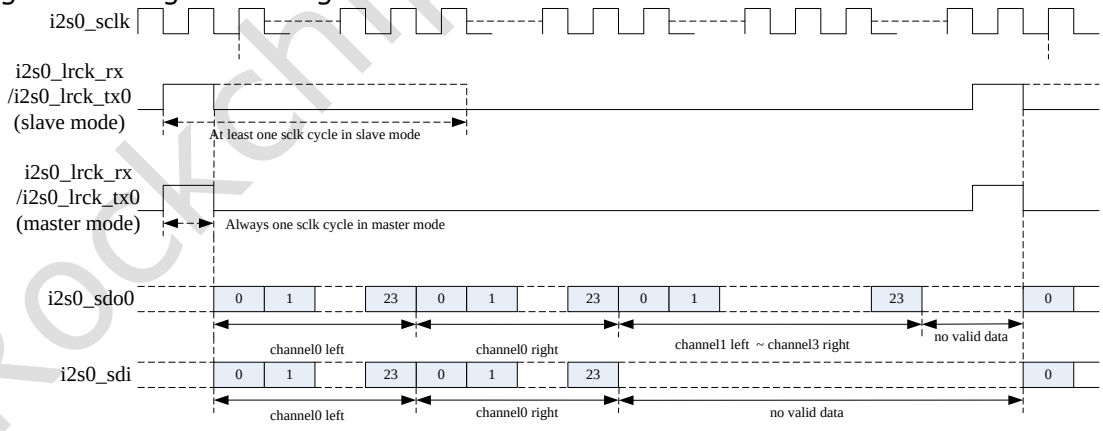


Fig. 20-8 PCM late1 mode timing format

20.3.6 PCM late2 mode

This is the waveform of PCM early mode. For LRCK (i2s_lrck_rx / i2s_lrck_tx0) signal, it goes high to indicate the start of a group of audio channels. For SD (i2s_sdo0, i2s_sdi) signal, it transfers MSB or LSB first and sends the first bit two SCLK clock cycles after LRCK goes high. The range of SD signal width is from 16 to 32bits.

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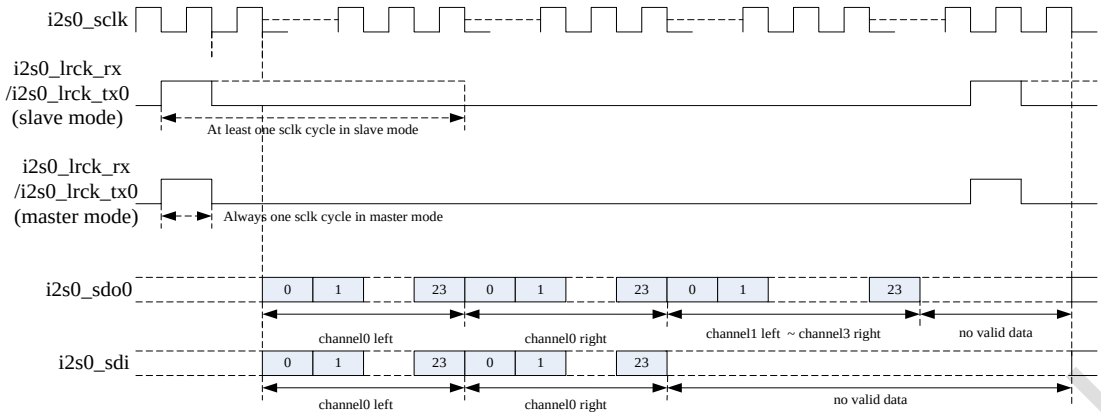


Fig. 20-9 PCM late2 mode timing format

20.3.7 PCM late3 mode

This is the waveform of PCM early mode. For LRCK (i2s_lrck_rx / i2s_lrck_tx0) signal, it goes high to indicate the start of a group of audio channels. For SD (i2s_sdo0, i2s_sdi) signal, it transfers MSB or LSB first and sends the first bit three SCLK clock cycles after LRCK goes high. The range of SD signal width is from 16 to 32bits.

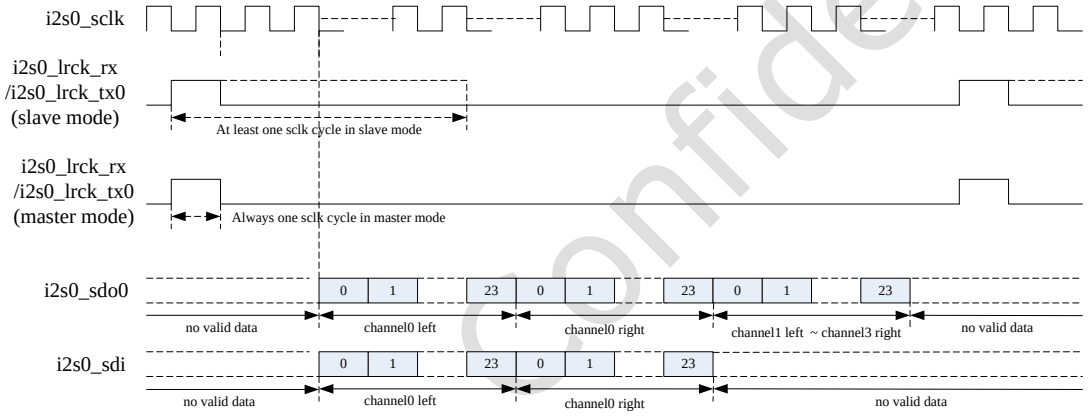


Fig. 20-10 PCM late3 mode timing format

20.4 Register Description

20.4.1 Registers Summary

Name	Offset	Size	Reset Value	Description
I2S_TXCR	0x0000	W	0x0000000f	transmit operation control register
I2S_RXCR	0x0004	W	0x0000000f	receive operation control register
I2S_CKR	0x0008	W	0x00071f1f	clock generation register
I2S_FIFOLR	0x000c	W	0x00000000	FIFO level register
I2S_DMACR	0x0010	W	0x001f0000	DMA control register
I2S_INTCR	0x0014	W	0x00000000	interrupt control register
I2S_INTSR	0x0018	W	0x00000000	interrupt status register
I2S_XFER	0x001c	W	0x00000000	Transfer Start Register
I2S_CLR	0x0020	W	0x00000000	SCLK domain logic clear Register
I2S_TXDR	0x0024	W	0x00000000	Transmit FIFO Data Register
I2S_RXDR	0x0028	W	0x00000000	Receive FIFO Data Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

20.4.2 Detail Register Description

I2S_TXCR

Address: Operational Base + offset (0x0000)

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transmit operation control register

Bit	Attr	Reset Value	Description
31:23	RO	0x0	reserved
22:17	RW	0x00	RCNT right justified counter (Can be written only when XFER[0] bit is 0.) Only valid in I2S Right justified format and slave tx mode is selected. Start to transmit data RCNT sclk cycles after left channel valid.
16:15	RW	0x0	CSR Channel select register 2'b00:2 channel 2'b01:4 channel 2'b10:6 channel 2'b11:8 channel
14	RW	0x0	HWT Halfword word transform (Can be written only when XFER[0] bit is 0.) Only valid when VDW select 16bit data. 0:32 bit data valid from AHB/APB bus. Low 16 bit for left channel and high 16 bit for right channel. 1:low 16bit data valid from AHB/APB bus, high 16 bit data invalid.
13	RO	0x0	reserved
12	RW	0x0	SJM Store justified mode (Can be written only when XFER[0] bit is 0.) 16bit~31bit DATA stored in 32 bits width fifo. If VDW select 16bit data, this bit is valid only when HWT select 0.Because if HWT is 1, every fifo unit contain two 16bit data and 32 bit space is full, it is impossible to choose justified mode. 0:right justified 1:left justified
11	RW	0x0	FBM First Bit Mode (Can be written only when XFER[0] bit is 0.) 0:MSB 1:LSB
10:9	RW	0x0	IBM I2S bus mode (Can be written only when XFER[0] bit is 0.) 0:I2S normal 1:I2S Left justified 2:I2S Right justified 3:reserved

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Bit	Attr	Reset Value	Description
8:7	RW	0x0	PBM PCM bus mode (Can be written only when XFER[0] bit is 0.) 0:PCM no delay mode 1:PCM delay 1 mode 2:PCM delay 2 mode 3:PCM delay 3 mode
6	RO	0x0	reserved
5	RW	0x0	TFS Transfer format select (Can be written only when XFER[0] bit is 0.) 0: I2S format 1: PCM format
4:0	RW	0x0f	VDW Valid Data width (Can be written only when XFER[0] bit is 0.) 0~14:reserved 15:16bit 16:17bit 17:18bit 18:19bit …… 28:29bit 29:30bit 30:31bit 31:32bit

I2S_RXCR

Address: Operational Base + offset (0x0004)

receive operation control register

Bit	Attr	Reset Value	Description
31:15	RO	0x0	reserved
14	RW	0x0	HWT Halfword word transform (Can be written only when XFER[1] bit is 0.) Only valid when VDW select 16bit data. 0:32 bit data valid to AHB/APB bus. Low 16 bit for left channel and high 16 bit for right channel. 1:low 16bit data valid to AHB/APB bus, high 16 bit data invalid.
13	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
12	RW	0x0	SJM Store justified mode (Can be written only when XFER[1] bit is 0.) 16bit~31bit DATA stored in 32 bits width fifo. If VDW select 16bit data, this bit is valid only when HWT select 0.Because if HWT is 1, every fifo unit contain two 16bit data and 32 bit space is full, it is impossible to choose justified mode. 0:right justified 1:left justified
11	RW	0x0	FBM First Bit Mode (Can be written only when XFER[1] bit is 0.) 0:MSB 1:LSB
10:9	RW	0x0	IBM I2S bus mode (Can be written only when XFER[1] bit is 0.) 0:I2S normal 1:I2S Left justified 2:I2S Right justified 3:reserved
8:7	RW	0x0	PBM PCM bus mode (Can be written only when XFER[1] bit is 0.) 0:PCM no delay mode 1:PCM delay 1 mode 2:PCM delay 2 mode 3:PCM delay 3 mode
6	RO	0x0	reserved
5	RW	0x0	TFS Transfer format select (Can be written only when XFER[1] bit is 0.) 0:i2s 1:pcm

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Bit	Attr	Reset Value	Description
4:0	RW	0x0f	VDW Valid Data width (Can be written only when XFER[1] bit is 0.) 0~14:reserved 15:16bit 16:17bit 17:18bit 18:19bit …… 28:29bit 29:30bit 30:31bit 31:32bit

I2S_CKR
Address: Operational Base + offset (0x0008)
clock generation register

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27	RW	0x0	MSS Master/slave mode select (Can be written only when XFER[1] or XFER[0] bit is 0.) 0:master mode(sclk output) 1:slave mode(sclk input)
26	RW	0x0	CKP Sclk polarity (Can be written only when XFER[1] or XFER[0] bit is 0.) 0: sample data at posedge sclk and drive data at negedge sclk 1: sample data at negedge sclk and drive data at posedge sclk
25	RW	0x0	RLP Receive lrck polarity (Can be written only when XFER[1] or XFER[0] bit is 0.) 0:normal polarity (I2S normal: low for left channel, high for right channel I2S left/right just: high for left channel, low for right channel PCM start signal:high valid) 1:oppsite polarity (I2S normal: high for left channel, low for right channel I2S left/right just: low for left channel, high for right channel PCM start signal:low valid)

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Bit	Attr	Reset Value	Description
24	RW	0x0	TLP Transmit lrck polarity (Can be written only when XFER[1] or XFER[0] bit is 0.) 0:normal polarity (I2S normal: low for left channel, high for right channel I2S left/right just: high for left channel, low for right channel PCM start signal:high valid) 1:oppsite polarity (I2S normal: high for left channel, low for right channel I2S left/right just: low for left channel, high for right channel PCM start signal:low valid)
23:16	RW	0x07	MDIV mclk divider (Can be written only when XFER[1] or XFER[0] bit is 0.) mclk divider = mclk / (sclk-1). For example, if mclk divider is 5, then the frequency of sclk is mclk/6
15:8	RW	0x1f	RSD Receive sclk divider (Can be written only when XFER[1] or XFER[0] bit is 0.) 0~30:reserved 31~255:frequency of rx_lrck= (Receive sclk divider[7:1]+1)*2*frequency of sclk
7:0	RW	0x1f	TSD Transmit sclk divider (Can be written only when XFER[1] or XFER[0] bit is 0.) 0~30:reserved 31~255:frequency of tx_lrck= (Transmit sclk divider[7:1]+1)*2*frequency of sclk

I2S_FIFOLR

Address: Operational Base + offset (0x000c)

FIFO level register

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RO	0x00	RFL Receive FIFO Level Contains the number of valid data entries in the receive FIFO.
23:18	RO	0x00	TFL3 Transmit FIFO3 Level Contains the number of valid data entries in the transmit FIFO3.
17:12	RO	0x00	TFL2 Transmit FIFO2 Level Contains the number of valid data entries in the transmit FIFO2.

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Bit	Attr	Reset Value	Description
11:6	RO	0x00	TFL1 Transmit FIFO1 Level Contains the number of valid data entries in the transmit FIFO1.
5:0	RO	0x00	TFL0 Transmit FIFO0 Level Contains the number of valid data entries in the transmit FIFO0.

I2S_DMACR

Address: Operational Base + offset (0x0010)

DMA control register

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24	RW	0x0	RDE Receive DMA Enable 0 : Receive DMA disabled 1 : Receive DMA enabled
23:21	RO	0x0	reserved
20:16	RW	0x1f	RDL Receive Data Level This bit field controls the level at which a DMA request is made by the receive logic. The watermark level = DMARDL+1; that is, dma_rx_req is generated when the number of valid data entries in the receive FIFO is equal to or above this field value + 1.
15:9	RO	0x0	reserved
8	RW	0x0	TDE Transmit DMA Enable 0 : Transmit DMA disabled 1 : Transmit DMA enabled
7:5	RO	0x0	reserved
4:0	RW	0x00	TDL Transmit Data Level This bit field controls the level at which a DMA request is made by the transmit logic. It is equal to the watermark level; that is, the dma_tx_req signal is generated when the number of valid data entries in the TXFIFO(TXFIFO0 if CSR=00;TXFIFO1 if CSR=01,TXFIFO2 if CSR=10,TXFIFO3 if CSR=11)is equal to or below this field value.

I2S_INTCR

Address: Operational Base + offset (0x0014)

interrupt control register

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
24:20	RW	0x00	RFT Receive FIFO Threshold When the number of receive FIFO entries is more than or equal to this threshold plus 1, the receive FIFO full interrupt is triggered.
19	RO	0x0	reserved
18	WO	0x0	RXOIC RX overrun interrupt clear Write 1 to clear RX overrun interrupt.
17	RW	0x0	RXOIE RX overrun interrupt enable 0:disable 1:enable
16	RW	0x0	RXFIE RX full interrupt enable 0:disable 1:enable
15:9	RO	0x0	reserved
8:4	RW	0x00	TFT Transmit FIFO Threshold When the number of transmit FIFO (TXFIFO0 if CSR=00; TXFIFO1 if CSR=01, TXFIFO2 if CSR=10, TXFIFO3 if CSR=11) entries is less than or equal to this threshold, the transmit FIFO empty interrupt is triggered.
3	RO	0x0	reserved
2	WO	0x0	TXUIC TX underrun interrupt clear Write 1 to clear TX underrun interrupt.
1	RW	0x0	TXUIE TX underrun interrupt enable 0:disable 1:enable
0	RW	0x0	TXEIE TX empty interrupt enable 0:disable 1:enable

I2S_INTSR

Address: Operational Base + offset (0x0018)

interrupt status register

Bit	Attr	Reset Value	Description
31:18	RO	0x0	reserved
17	RO	0x0	RXOI RX overrun interrupt 0:inactive 1:active

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Bit	Attr	Reset Value	Description
16	RO	0x0	RXFI RX full interrupt 0:inactive 1:active
15:2	RO	0x0	reserved
1	RO	0x0	TXUI TX underrun interrupt 0:inactive 1:active
0	RO	0x0	TXEI TX empty interrupt 0:inactive 1:active

I2S_XFER
Address: Operational Base + offset (0x001c)
Transfer Start Register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x0	RXS RX Transfer start bit 0:stop RX transfer. 1:start RX transfer
0	RW	0x0	TXS TX Transfer start bit 0:stop TX transfer. 1:start TX transfer

I2S_CLR
Address: Operational Base + offset (0x0020)
SCLK domain logic clear Register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x0	RXC RX logic clear This is a self cleared bit. Write 1 to clear all receive logic.
0	RW	0x0	TXC TX logic clear This is a self cleared bit. Write 1 to clear all transmit logic.

I2S_TXDR
Address: Operational Base + offset (0x0024)
Transmit FIFO Data Register

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Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	TXDR Transmit FIFO Data Register When it is written to, data are moved into the transmit FIFO.

I2S_RXDR
Address: Operational Base + offset (0x0028)
Receive FIFO Data Register

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXDR Receive FIFO Data Register When the register is read, data in the receive FIFO is accessed.

20.5 Interface Description

I2S 8ch is internally connected to the HDMI and audio codec. Following tables show the connection.

Table 20-1 Interface connection between I2s 8ch and HDMI

Module Pin	Direction	Module Pin	Direction
i2s_sclk	O	pin_sck	I
i2s_lrck_tx	O	pin_ws	I
i2s_sdo[3:0]	O	pin_sd[3:0]	I

Table 20-2 Interface connection between I2s 8ch and audio codec

Module Pin	Direction	Module Pin	Direction
i2s_sclk	I/O	pin_sck	I/O
i2s_lrck_rx	I/O	pin_adc_ws	I/O
i2s_lrck_tx	I/O	pin_dac_ws	I/O
i2s_sdo[0]	O	pin_dac_sd_i	I
i2s_sdi[0]	I	pin_adc_sd_o	O

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20.6 Application Notes

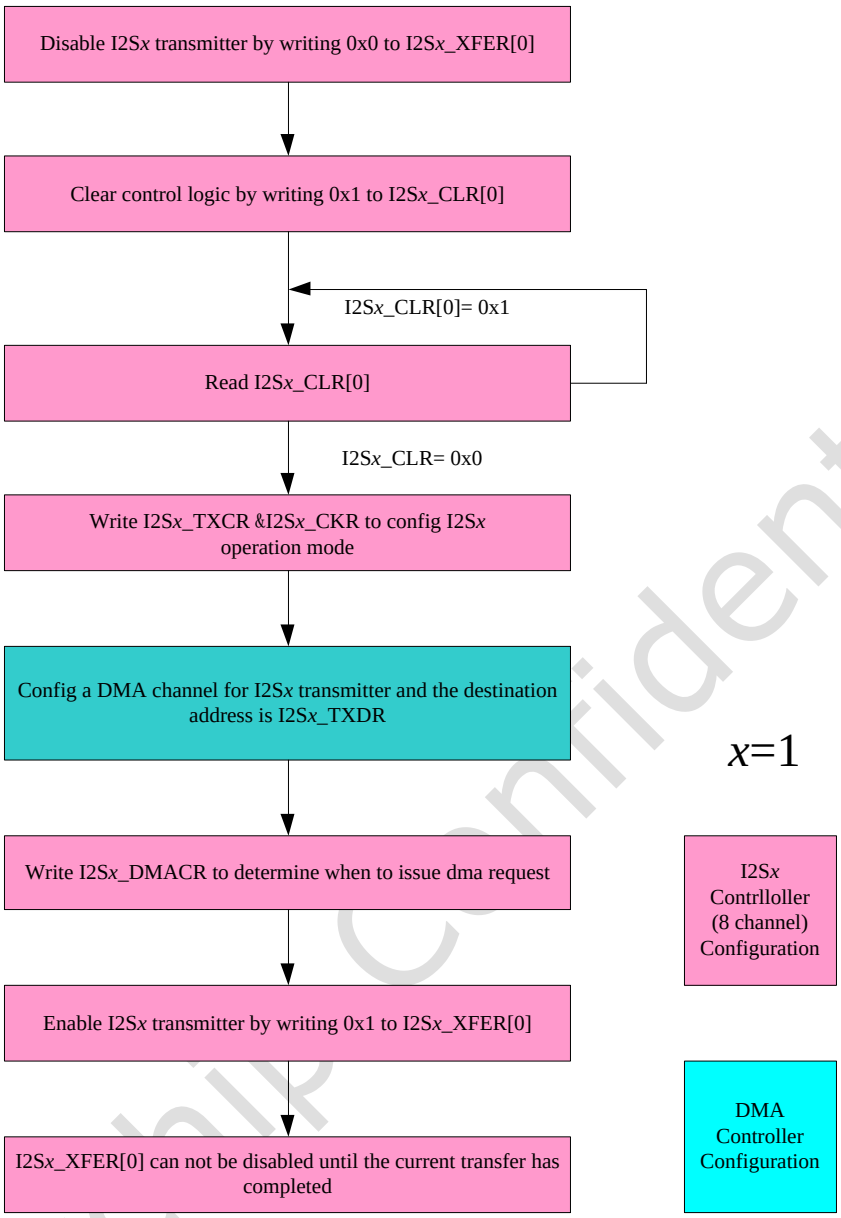


Fig. 20-11 I2S/PCM controller transmit operation flow chart

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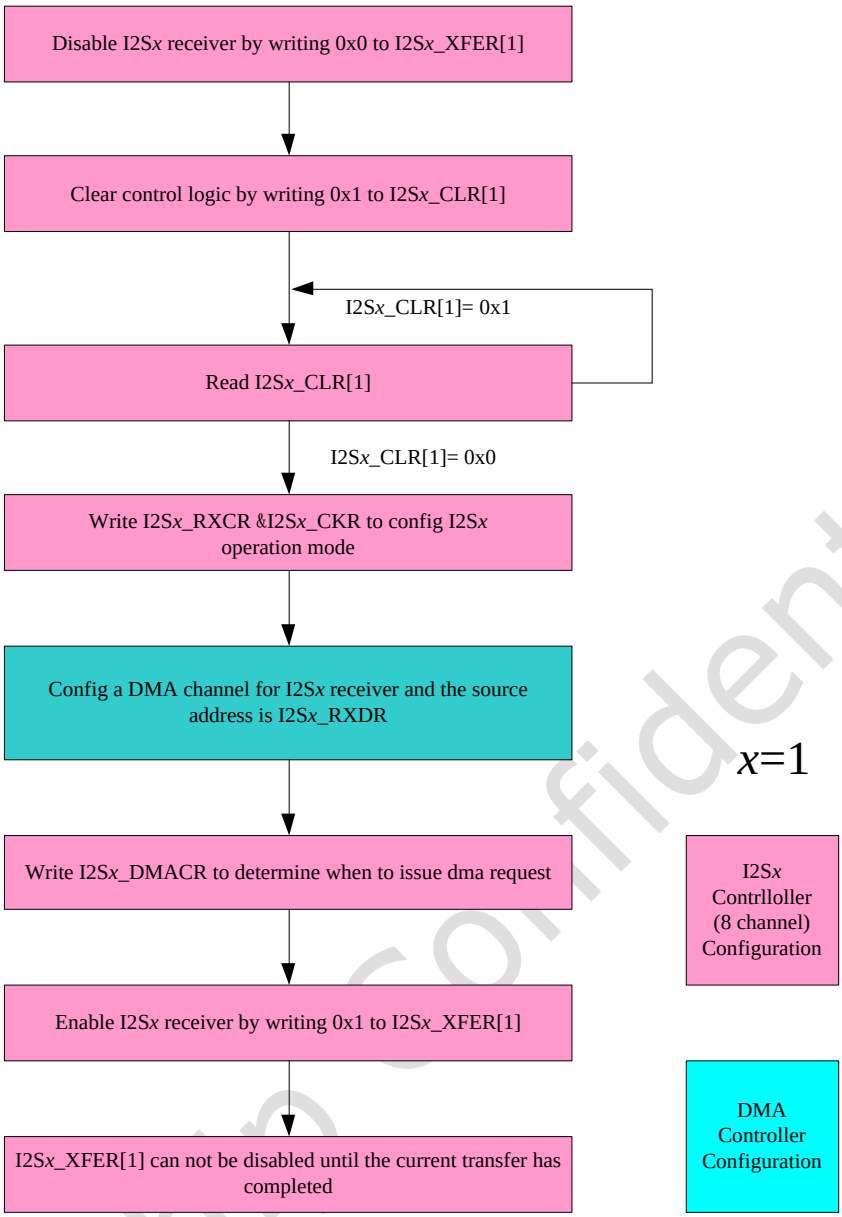


Fig. 20-12 I2S/PCM controller receive operation flow chart

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Chapter 21 I2S 2-channel

21.1 Overview

The I2S/PCM controller is designed for interfacing between the AHB bus and the I2S bus. The I2S bus (Inter-IC sound bus) is a serial link for digital audio data transfer between devices in the system and is invented by Philips Semiconductor. Now it is widely used by many semiconductor manufacturers.
I2S bus is widely used in the devices such as ADC, DAC, DSP, CPU, etc. With the I2S interface, we can connect audio devices and the embedded SoC platform together and provide an audio interface solution for the system.

21.1.1 Features

Not only I2S but also PCM mode stereo audio output and input are supported in I2S/PCM controller.

- Support two internal 32-bit wide and 32-location deep FIFOs, one for transmitting and the other for receiving audio data
- Support AHB bus interface
- Support 16 ~ 32 bits audio data transfer
- Support master and slave mode
- Support DMA handshaking interface and configurable DMA water level
- Support transmit FIFO empty, underflow, receive FIFO full, overflow interrupt and all interrupts can be masked
- Support configurable water level of transmit FIFO empty and receive FIFO full interrupt
- Support combined interrupt output
- Support 2-channel audio transmitting in I2S mode and PCM mode
- Support 2-channel audio receiving in I2S and PCM mode
- Support up to 192kHz sample rate
- Support I2S normal, left and right justified mode serial audio data transfer
- Support PCM early, late1, late2, late3 mode serial audio data transfer
- Support MSB or LSB first serial audio data transfer
- Support 16 to 31 bit audio data left or right justified in 32-bit wide FIFO
- Support two 16-bit audio data store together in one 32-bit wide location
- Support 2 independent LRCK signals, one for receiving and the other for transmitting audio data
- Support configurable SCLK and LRCK polarity

21.2 Block Diagram

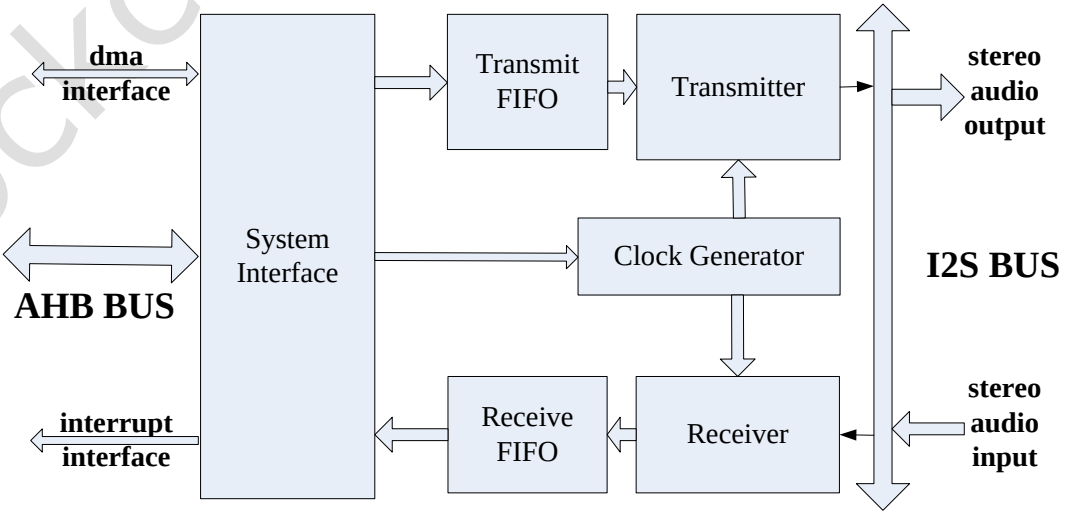


Fig. 21-1 I2S/PCM controller (2 channel) Block Diagram

System Interface

The system interface implements the AHB slave operation. It contains not only control registers of transmitters and receiver inside but also interrupt and DMA handshaking

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interface.

Clock Generator

The Clock Generator implements clock generation function. The input source clock to the module is MCLK_I2S, and by the divider of the module, the clock generator generates SCLK and LRCK to transmitter and receiver.

Transmitters

The Transmitters implement transmission operation. The transmitters can act as either a master or a slave, with I2S or PCM mode stereo serial audio interface.

Receiver

The Receiver implements receive operation. The receiver can act as either a master or a slave, with I2S or PCM mode stereo serial audio interface.

Transmit FIFO

The Transmit FIFO is the buffer to store transmitted audio data. The size of the FIFO is 32bits x 32.

Receive FIFO

The Receive FIFO is the buffer to store received audio data. The size of the FIFO is 32bits x 32.Function Description

21.3 Function description

In the I2S/PCM controller, there are four types: transmitter-master &receiver-master; transmitter-master & receiver-slave; transmitter-slave & receiver-master; transmitter-slave & receiver-slave.

In broadcasting application, the I2S/PCM controller is used as a transmitter and external or internal audio CODEC is used as a receiver. In recording application, the I2S/PCM controller is used as a receiver and external or internal audio CODEC is used as a transmitter. Either the I2S/PCM controller or the audio CODEC can act as a master or a slave, but if one is master, the other must be slave.

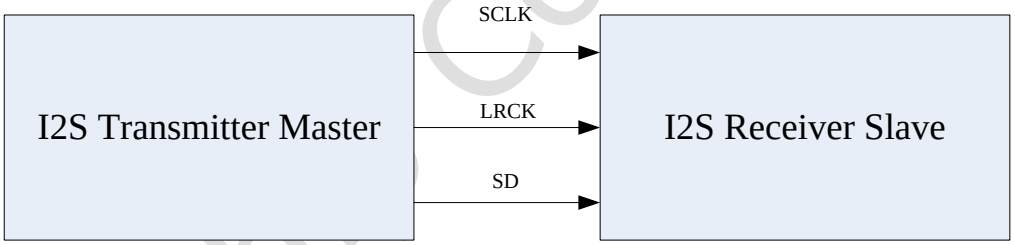


Fig. 21-2 I2S transmitter-master & receiver-slave condition

When the transmitter acts as a master, it sends all signals to the receiver (the slave), and CPU controls when to send clock and data to the receiver. When acts as a slave, SD signal still goes from transmitter to receiver, but SCLK and LRCK signals are from the receiver (the master) to the transmitter. Based on three interface specifications, transmitting data should be ready before transmitter receives SCLK and LRCK signals. CPU should know when the receiver to initialize a transaction and when the transmitter to send data.

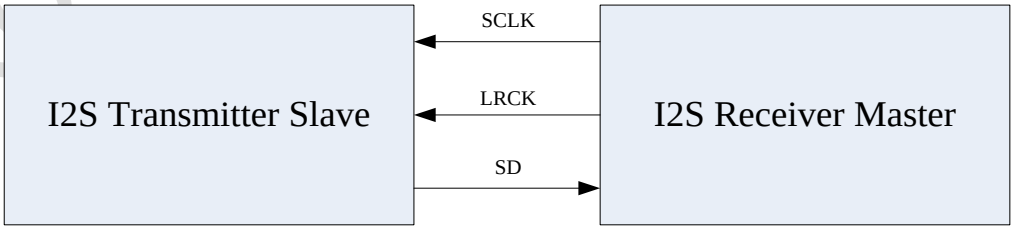


Fig. 21-3 I2S transmitter-slave & receiver-master condition

When the receiver acts as a master, it sends SCLK and LRCK signals to the transmitter (the slave) and receives serial data. So CPU must tell the transmitter when to start a transaction for it to prepare transmitting data then start a transfer and send clock and channel-select signals. When the receiver acts as a slave, CPU should only do initial setting and wait for all signals and then start reading data.

Before transmitting or receiving data, CPU need do initial setting to the I2S register. These

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includes CPU settings, I2S interface registers settings, and maybe the embedded SoC platform settings. These registers must be set before starting data transfer.

21.3.1 I2S normal mode

This is the waveform of I2S normal mode. For LRCK (i2s1_lrck_rx/i2s1_lrck_tx) signal, it goes low to indicate left channel and high to right channel. For SD (i2s1_sdo, i2s1_sdi) signal, it starts sending the first bit (MSB or LSB) one SCLK clock cycle after LRCK changes. The range of SD signal width is from 16 to 32bits.

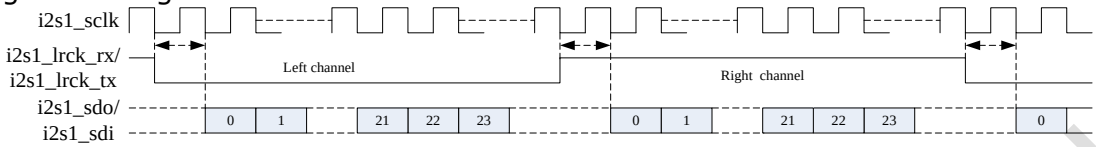


Fig. 21-4 I2S normal mode timing format

21.3.2 I2S left justified mode

This is the waveform of I2S left justified mode. For LRCK (i2s1_lrck_rx / i2s1_lrck_tx) signal, it goes high to indicate left channel and low to right channel. For SD (i2s1_sdo, i2s1_sdi) signal, it starts sending the first bit (MSB or LSB) at the same time when LRCK changes. The range of SD signal width is from 16 to 32bits.

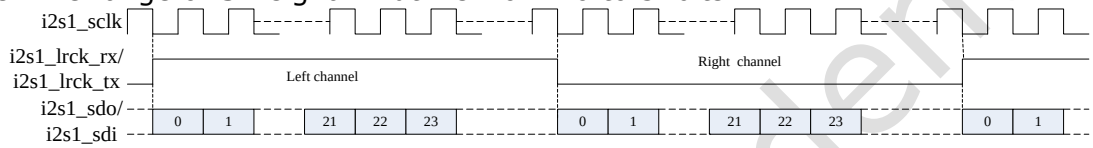


Fig. 21-5 I2S left justified mode timing format

21.3.3 I2S right justified mode

This is the waveform of I2S right justified mode. For LRCK (i2s1_lrck_rx/ i2s1_lrck_tx) signal, it goes high to indicate left channel and low to right channel. For SD (i2s1_sdo, i2s1_sdi) signal, it transfers MSB or LSB first; but what is different from I2S normal or left justified mode, the last bit of the transferred data is aligned to the transition edge of the LRCK signal while one bit is transferred at one SCLK cycle. The range of SD signal width is from 16 to 32bits.

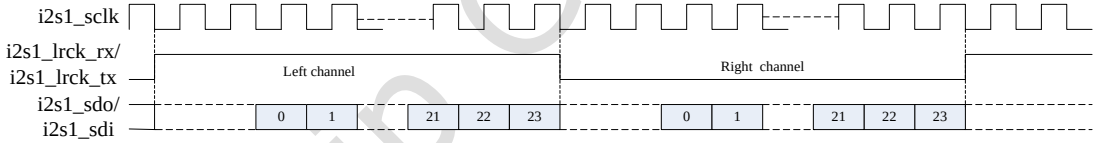


Fig. 21-6 I2S right justified mode timing format

21.3.4 PCM early mode

This is the waveform of PCM early mode. For LRCK (i2s1_lrck_rx/i2s1_lrck_tx) signal, it goes high to indicate the start of a group of audio channels. For SD (i2s1_sdo, i2s1_sdi) signal, it sends the first bit (MSB or LSB) at the same time when LRCK goes high. The range of SD signal width is from 16 to 32bits.

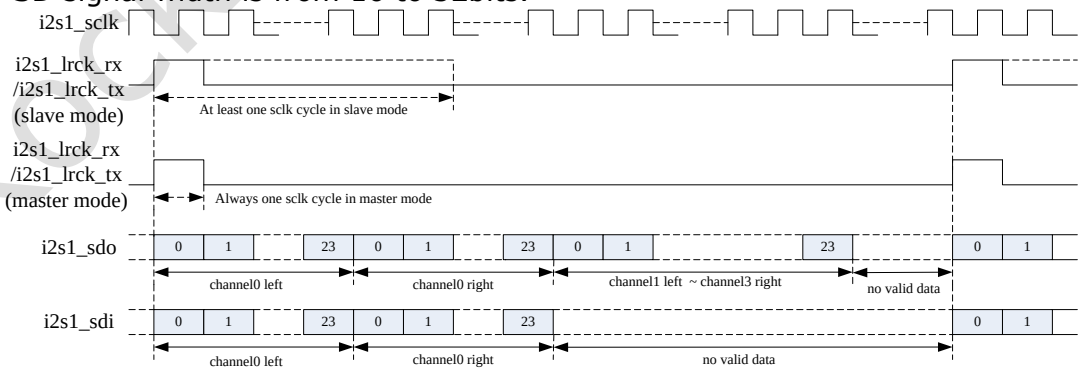


Fig. 21-7 PCM early mode timing format

21.3.5 PCM late1 mode

This is the waveform of PCM early mode. For LRCK (i2s1_lrck_rx/i2s1_lrck_tx) signal, it goes high to indicate the start of a group of audio channels. For SD (i2s1_sdo, i2s1_sdi) signal, it sends the first bit (MSB or LSB) one SCLK clock cycle after LRCK goes high. The range of SD signal width is from 16 to 32bits.

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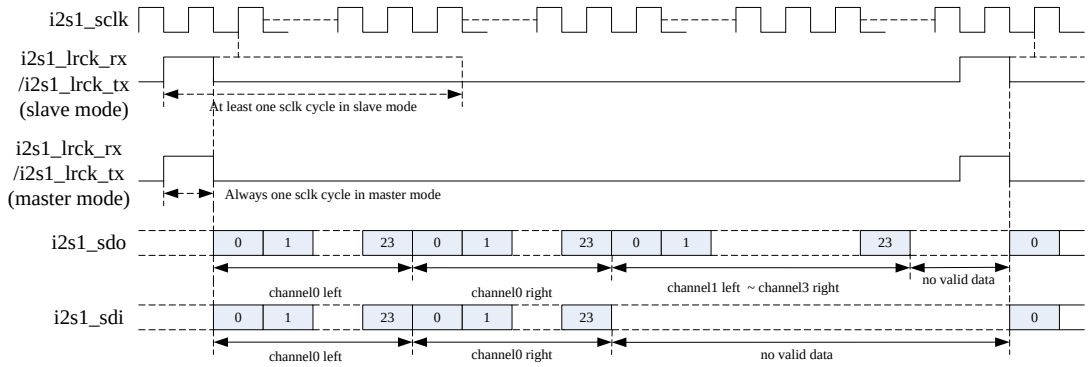


Fig. 21-8 PCM late1 mode timing format

21.3.6 PCM late2 mode

This is the waveform of PCM early mode. For LRCK (i2s1_lrck_rx/i2s1_lrck_tx) signal, it goes high to indicate the start of a group of audio channels. For SD (i2s1_sdo, i2s1_sdi) signal, it sends the first bit (MSB or LSB)two SCLK clock cycles after LRCK goes high. The range of SD signal width is from 16 to 32bits.

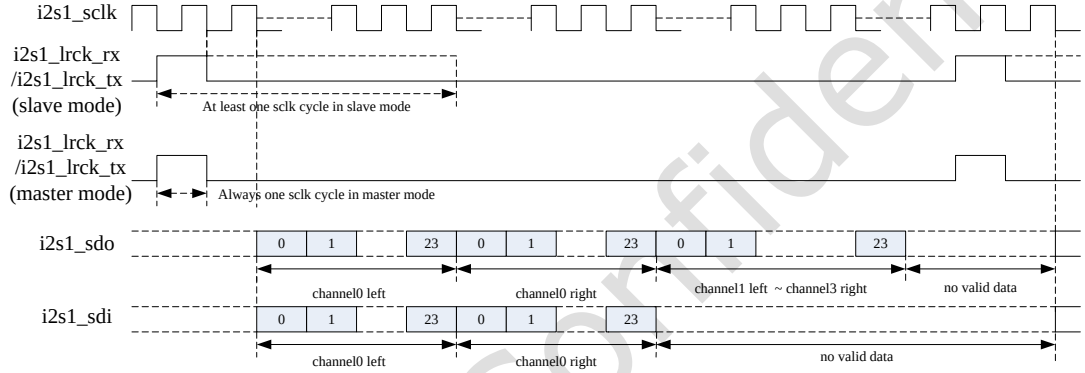


Fig. 21-9 PCM late2 mode timing format

21.3.7 PCM late3 mode

This is the waveform of PCM early mode. For LRCK (i2s1_lrck_rx/i2s1_lrck_tx) signal, it goes high to indicate the start of a group of audio channels. For SD (i2s1_sdo, i2s1_sdi) signal, it sends the first bit (MSB or LSB) three SCLK clock cycles after LRCK goes high. The range of SD signal width is from 16 to 32bits.

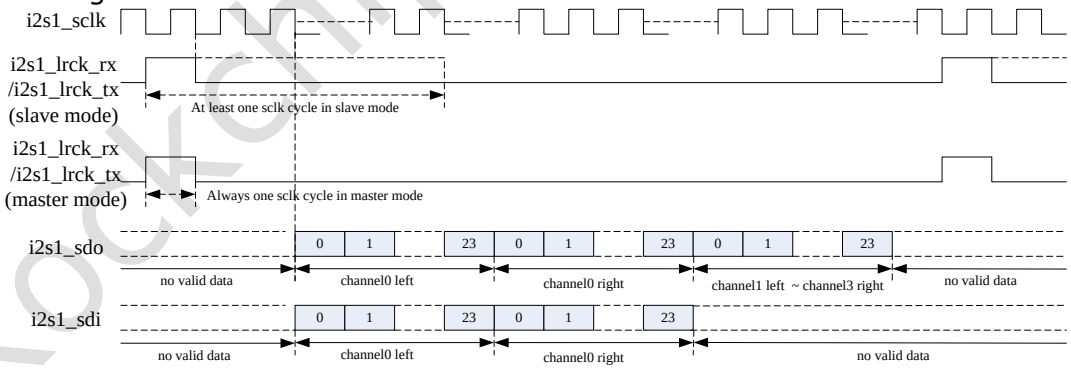


Fig. 21-10 PCM late3 mode timing format

21.4 Register Description

21.4.1 Registers Summary

Name	Offset	Size	Reset Value	Description
I2S_TXCR	0x0000	W	0x0000000f	transmit operation control register
I2S_RXCR	0x0004	W	0x0000000f	receive operation control register
I2S_CKR	0x0008	W	0x00071f1f	clock generation register

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Name	Offset	Size	Reset Value	Description
I2S_FIFOLR	0x000c	W	0x00000000	FIFO level register
I2S_DMACR	0x0010	W	0x001f0000	DMA control register
I2S_INTCR	0x0014	W	0x00000000	interrupt control register
I2S_INTSR	0x0018	W	0x00000000	interrupt status register
I2S_XFER	0x001c	W	0x00000000	Transfer Start Register
I2S_CLR	0x0020	W	0x00000000	SCLK domain logic clear Register
I2S_TXDR	0x0024	W	0x00000000	Transmit FIFO Data Register
I2S_RXDR	0x0028	W	0x00000000	Receive FIFO Data Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

21.4.2 Detail Register Description

I2S_TXCR

Address: Operational Base + offset (0x0000)
transmit operation control register

Bit	Attr	Reset Value	Description
31:23	RO	0x0	reserved
22:17	RW	0x00	RCNT right justified counter (Can be written only when XFER[0] bit is 0.) Only valid in I2S Right justified format and slave tx mode is selected. Start to transmit data RCNT sclk cycles after left channel valid.
16:15	RW	0x0	CSR Channel select register 2'b00:2 channel 2'b01:4 channel 2'b10:6 channel 2'b11:8 channel
14	RW	0x0	HWT Halfword word transform (Can be written only when XFER[0] bit is 0.) Only valid when VDW select 16bit data. 0:32 bit data valid from AHB/APB bus. Low 16 bit for left channel and high 16 bit for right channel. 1:low 16bit data valid from AHB/APB bus, high 16 bit data invalid.
13	RO	0x0	reserved
12	RW	0x0	SJM Store justified mode (Can be written only when XFER[0] bit is 0.) 16bit~31bit DATA stored in 32 bits width fifo. If VDW select 16bit data, this bit is valid only when HWT select 0.Because if HWT is 1, every fifo unit contain two 16bit data and 32 bit space is full, it is impossible to choose justified mode. 0:right justified 1:left justified

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Bit	Attr	Reset Value	Description
11	RW	0x0	FBM First Bit Mode (Can be written only when XFER[0] bit is 0.) 0:MSB 1:LSB
10:9	RW	0x0	IBM I2S bus mode (Can be written only when XFER[0] bit is 0.) 0:I2S normal 1:I2S Left justified 2:I2S Right justified 3:reserved
8:7	RW	0x0	PBM PCM bus mode (Can be written only when XFER[0] bit is 0.) 0:PCM no delay mode 1:PCM delay 1 mode 2:PCM delay 2 mode 3:PCM delay 3 mode
6	RO	0x0	reserved
5	RW	0x0	TFS Transfer format select (Can be written only when XFER[0] bit is 0.) 0: I2S format 1: PCM format
4:0	RW	0x0f	VDW Valid Data width (Can be written only when XFER[0] bit is 0.) 0~14:reserved 15:16bit 16:17bit 17:18bit 18:19bit …… 28:29bit 29:30bit 30:31bit 31:32bit

I2S_RXCR

Address: Operational Base + offset (0x0004)

receive operation control register

Bit	Attr	Reset Value	Description
31:15	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
14	RW	0x0	HWT Halfword word transform (Can be written only when XFER[1] bit is 0.) Only valid when VDW select 16bit data. 0:32 bit data valid to AHB/APB bus. Low 16 bit for left channel and high 16 bit for right channel. 1:low 16bit data valid to AHB/APB bus, high 16 bit data invalid.
13	RO	0x0	reserved
12	RW	0x0	SJM Store justified mode (Can be written only when XFER[1] bit is 0.) 16bit~31bit DATA stored in 32 bits width fifo. If VDW select 16bit data, this bit is valid only when HWT select 0.Because if HWT is 1, every fifo unit contain two 16bit data and 32 bit space is full, it is impossible to choose justified mode. 0:right justified 1:left justified
11	RW	0x0	FBM First Bit Mode (Can be written only when XFER[1] bit is 0.) 0:MSB 1:LSB
10:9	RW	0x0	IBM I2S bus mode (Can be written only when XFER[1] bit is 0.) 0:I2S normal 1:I2S Left justified 2:I2S Right justified 3:reserved
8:7	RW	0x0	PBM PCM bus mode (Can be written only when XFER[1] bit is 0.) 0:PCM no delay mode 1:PCM delay 1 mode 2:PCM delay 2 mode 3:PCM delay 3 mode
6	RO	0x0	reserved
5	RW	0x0	TFS Transfer format select (Can be written only when XFER[1] bit is 0.) 0:i2s 1:pcm

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Bit	Attr	Reset Value	Description
4:0	RW	0x0f	VDW Valid Data width (Can be written only when XFER[1] bit is 0.) 0~14:reserved 15:16bit 16:17bit 17:18bit 18:19bit …… 28:29bit 29:30bit 30:31bit 31:32bit

I2S_CKR

Address: Operational Base + offset (0x0008)

clock generation register

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27	RW	0x0	MSS Master/slave mode select (Can be written only when XFER[1] or XFER[0] bit is 0.) 0:master mode(sclk output) 1:slave mode(sclk input)
26	RW	0x0	CKP Sclk polarity (Can be written only when XFER[1] or XFER[0] bit is 0.) 0: sample data at posedge sclk and drive data at negedge sclk 1: sample data at negedge sclk and drive data at posedge sclk
25	RW	0x0	RLP Receive lrck polarity (Can be written only when XFER[1] or XFER[0] bit is 0.) 0:normal polarity (I2S normal: low for left channel, high for right channel I2S left/right just: high for left channel, low for right channel PCM start signal:high valid) 1:oppsite polarity (I2S normal: high for left channel, low for right channel I2S left/right just: low for left channel, high for right channel PCM start signal:low valid)

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Bit	Attr	Reset Value	Description
24	RW	0x0	TLP Transmit lrck polarity (Can be written only when XFER[1] or XFER[0] bit is 0.) 0:normal polarity (I2S normal: low for left channel, high for right channel I2S left/right just: high for left channel, low for right channel PCM start signal:high valid) 1:oppsite polarity (I2S normal: high for left channel, low for right channel I2S left/right just: low for left channel, high for right channel PCM start signal:low valid)
23:16	RW	0x07	MDIV mclk divider (Can be written only when XFER[1] or XFER[0] bit is 0.) mclk divider = mclk / (sclk-1). For example, if mclk divider is 5, then the frequency of sclk is mclk/6
15:8	RW	0x1f	RSD Receive sclk divider (Can be written only when XFER[1] or XFER[0] bit is 0.) 0~30:reserved 31~255:frequency of rx_lrck= (Receive sclk divider[7:1]+1)*2*frequency of sclk
7:0	RW	0x1f	TSD Transmit sclk divider (Can be written only when XFER[1] or XFER[0] bit is 0.) 0~30:reserved 31~255:frequency of tx_lrck= (Transmit sclk divider[7:1]+1)*2*frequency of sclk

I2S_FIFOLR
Address: Operational Base + offset (0x000c)
FIFO level register

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RO	0x00	RFL Receive FIFO Level Contains the number of valid data entries in the receive FIFO.
23:6	RO	0x00	reserved
5:0	RO	0x00	TFL Transmit FIFO Level Contains the number of valid data entries in the transmit FIFO.

I2S_DMACR
Address: Operational Base + offset (0x0010)

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DMA control register

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24	RW	0x0	RDE Receive DMA Enable 0 : Receive DMA disabled 1 : Receive DMA enabled
23:21	RO	0x0	reserved
20:16	RW	0x1f	RDL Receive Data Level This bit field controls the level at which a DMA request is made by the receive logic. The watermark level = DMARDL+1; that is, dma_rx_req is generated when the number of valid data entries in the receive FIFO is equal to or above this field value + 1.
15:9	RO	0x0	reserved
8	RW	0x0	TDE Transmit DMA Enable 0 : Transmit DMA disabled 1 : Transmit DMA enabled
7:5	RO	0x0	reserved
4:0	RW	0x00	TDL Transmit Data Level This bit field controls the level at which a DMA request is made by the transmit logic. It is equal to the watermark level; that is, the dma_tx_req signal is generated when the number of valid data entries in the TXFIFOis equal to or below this field value.

I2S_INTCR

Address: Operational Base + offset (0x0014)

interrupt control register

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24:20	RW	0x00	RFT Receive FIFO Threshold When the number of receive FIFO entries is more than or equal to this threshold plus 1, the receive FIFO full interrupt is triggered.
19	RO	0x0	reserved
18	WO	0x0	RXOIC RX overrun interrupt clear Write 1 to clear RX overrun interrupt.
17	RW	0x0	RXOIE RX overrun interrupt enable 0:disable 1:enable

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Bit	Attr	Reset Value	Description
16	RW	0x0	RXFIE RX full interrupt enable 0:disable 1:enable
15:9	RO	0x0	reserved
8:4	RW	0x00	TFT Transmit FIFO Threshold When the number of transmit FIFO entries is less than or equal to this threshold, the transmit FIFO empty interrupt is triggered.
3	RO	0x0	reserved
2	WO	0x0	TXUIC TX underrun interrupt clear Write 1 to clear TX underrun interrupt.
1	RW	0x0	TXUIE TX underrun interrupt enable 0:disable 1:enable
0	RW	0x0	TXEIE TX empty interrupt enable 0:disable 1:enable

I2S_INTSR
Address: Operational Base + offset (0x0018)
interrupt status register

Bit	Attr	Reset Value	Description
31:18	RO	0x0	reserved
17	RO	0x0	RXOI RX overrun interrupt 0:inactive 1:active
16	RO	0x0	RXFI RX full interrupt 0:inactive 1:active
15:2	RO	0x0	reserved
1	RO	0x0	TXUI TX underrun interrupt 0:inactive 1:active
0	RO	0x0	TXEI TX empty interrupt 0:inactive 1:active

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I2S_XFER
Address: Operational Base + offset (0x001c)
Transfer Start Register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x0	RXS RX Transfer start bit 0:stop RX transfer. 1:start RX transfer
0	RW	0x0	TXS TX Transfer start bit 0:stop TX transfer. 1:start TX transfer

I2S_CLR
Address: Operational Base + offset (0x0020)
SCLK domain logic clear Register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x0	RXC RX logic clear This is a self cleared bit. Write 1 to clear all receive logic.
0	RW	0x0	TXC TX logic clear This is a self cleared bit. Write 1 to clear all transmit logic.

I2S_TXDR
Address: Operational Base + offset (0x0024)
Transimt FIFO Data Register

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	TXDR Transmit FIFO Data Register When it is written to, data are moved into the transmit FIFO.

I2S_RXDR
Address: Operational Base + offset (0x0028)
Receive FIFO Data Register

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	RXDR Receive FIFO Data Register When the register is read, data in the receive FIFO is accessed.

21.5 Interface Description

I2S has 2 IOMUX, which controlled by GRF_SOC_CON1[5].
When GRF_SOC_CON1[5] is 1'b0, the IOMUX for I2S is as follow.

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Table 21-1 I2S Interface Description

Module Pin	Direction	Pad Name	IOMUX Setting
i2s_clk	O	IO_I2Smclk_MMC1clkout_XIN32k _GPIO1a0	GRF_GPIO1A_IOMUX[1: 0]=2'b1
i2s_sclk	I/O	IO_I2Ssclk_MMC1d0_PMICsleep1 _GPIO1a1	GRF_GPIO1A_IOMUX[3:2]= 2'b1
i2s_lrck_ rx	I/O	IO_I2Slrckrx_MMC1d1_GPIO1a2	GRF_GPIO1A_IOMUX[5:4]= 2'b1
i2s_lrck_ tx	I/O	IO_I2Slrcktx_GPIO1a3	GRF_GPIO1A_IOMUX[6]=1' b1
i2s_sdo	O	IO_I2Ssdo_MMC1d2_GPIO1a4	GRF_GPIO1A_IOMUX[9:8]=2 'b1
i2s_sdi	I	IO_I2Ssdi_MMC1d3_GPIO1a5	GRF_GPIO1A_IOMUX[11:10] =2'b1

When GRF_SOC_CON1[5] is 1'b1, the IOMUX for I2S1 is as follow.

Table 21-2 I2S1 Interface Description

Module Pin	Direction	Pad Name	IOMUX Setting
i2s_clk	O	IO_I2S1mclk_GPIO0b0	GRF_GPIO0B_IOMUX[0]=1' b1
i2s_sclk	I/O	IO_I2S1sclk_SPIclkm_GPIO0b1	GRF_GPIO0B_IOMUX[3:2]= 2'b01
i2s_lrck_ rx	I/O	IO_I2S1lrckrx_SPItxdm_GPIO0b3	GRF_GPIO0B _IOMUX[7:6]=2'b01
i2s_lrck_ tx	I/O	IO_I2S1lrcktx_GPIO0b4	GRF_GPIO0B _IOMUX[8]=1'b1
i2s_sdo	O	IO_I2S1sdo_SPIrxdm_GPIO0b5	GRF_GPIO0B _IOMUX[11:10]=2'b1
i2s_sdi	I	IO_I2S1sdi_SPIcsn0m_GPIO0b6	GRF_GPIO0B _IOMUX[13:12]=1'b1

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21.6 Application Notes

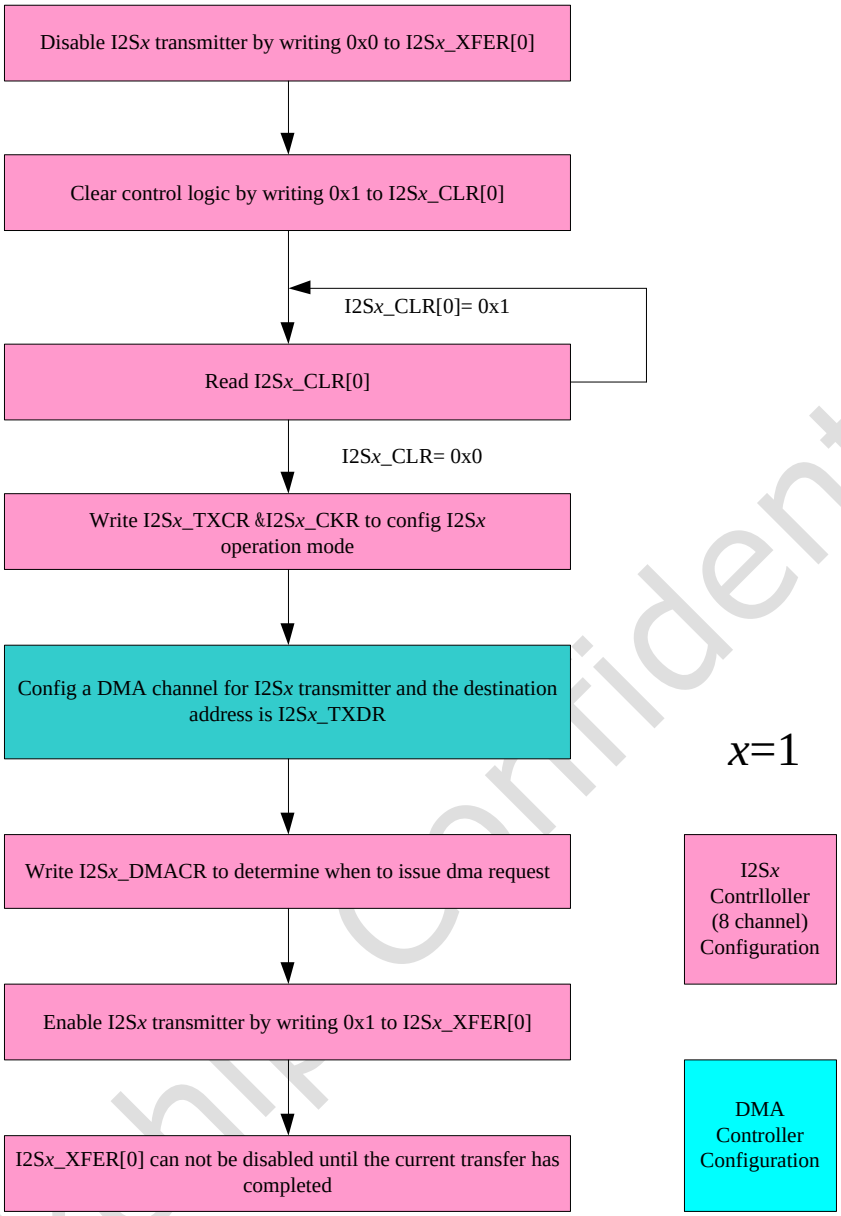


Fig. 21-11 I2S/PCM controller transmit operation flow chart

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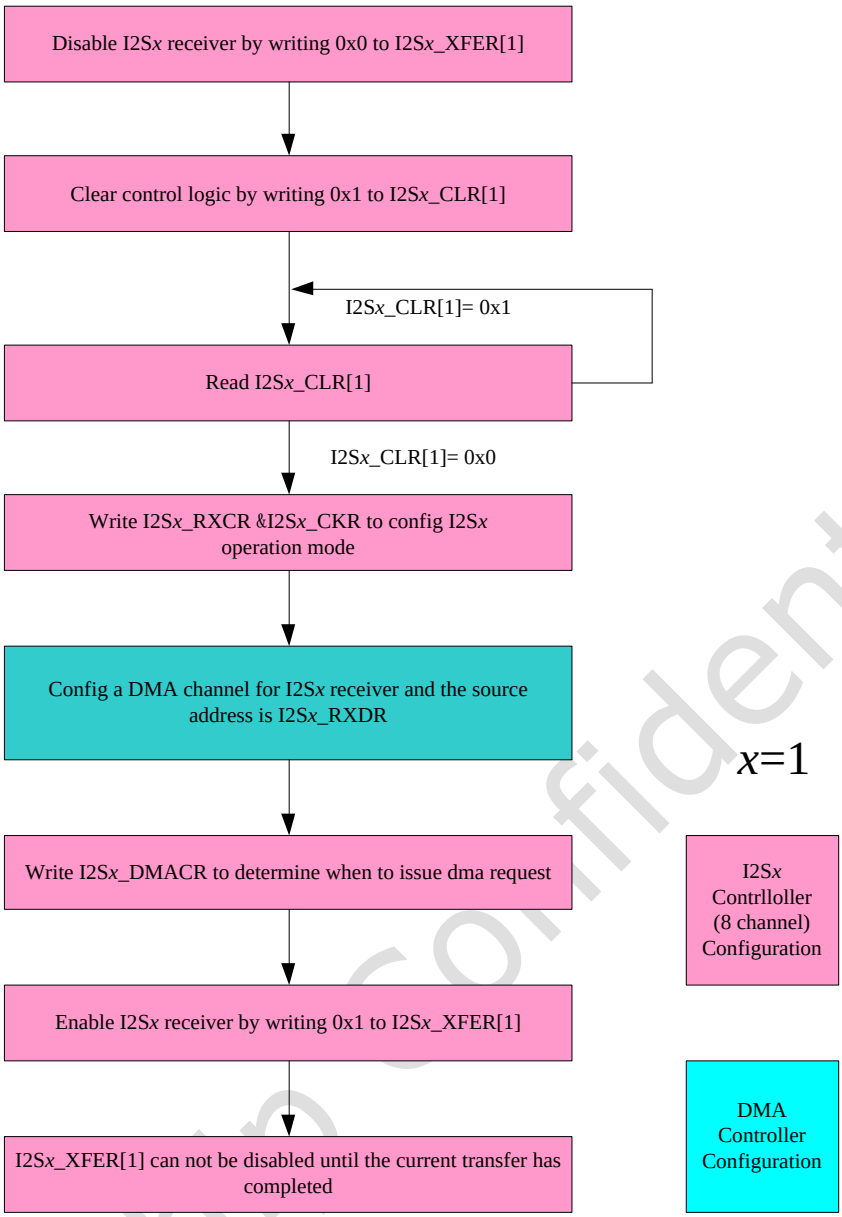


Fig. 21-12 I2S/PCM controller receive operation flow chart

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Chapter 22 SPDIF Transmitter

22.1 Overview

The SPDIF transmitter is a self-clocking, serial, unidirectional interface for the interconnection of digital audio equipment for consumer and professional applications, using linear PCM coded audio samples.
It provides the basic structure of the interface. Separate documents define items specific to particular applications.
When used in a professional application, the interface is primarily intended to carry monophonic or stereophonic programmes, at a 48 kHz sampling frequency and with a resolution of up to 24bits per sample; it may alternatively be used to carry signals sampled at 32 kHz or 44.1 kHz.
When used in a consumer application, the interface is primarily intended to carry stereophonic programmes, with a resolution of up to 20 bits per sample, an extension to 24 bits per sample being possible.
When used for other purposes, the interface is primarily intended to carry audio data coded other than as linear PCM coded audio samples. Provision is also made to allow the interface to carry data related to computer software or signals coded using non-linear PCM. The format specification for these applications is not part of this standard.
In all cases, the clock references and auxiliary information are transmitted along with the programme.
It supports following features:

- Support one internal 32-bit wide and 32-location deep sample data buffer
- Support two 16-bit audio data store together in one 32-bit wide location
- Support AHB bus interface
- Support biphase format stereo audio data output
- Support DMA handshake interface and configurable DMA water level
- Support sample data buffer empty and block terminate interrupt
- Support combine interrupt output
- Support 16 to 31 bit audio data left or right justified in 32-bit wide sample data buffer
- Support 48, 44.1, 32kHz sample rate
- Support 16, 20, 24 bits audio data transfer

22.2 Block Diagram

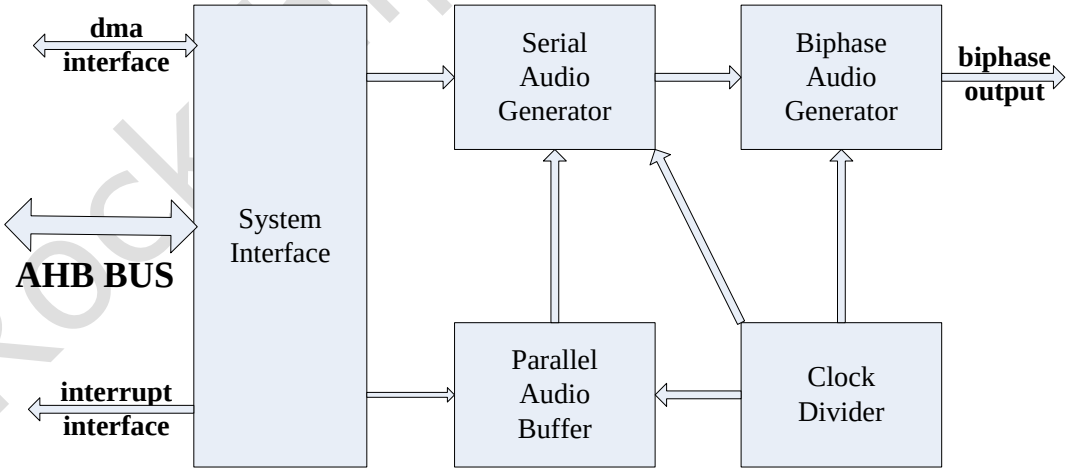


Fig. 22-1 SPDIF transmitter Block Diagram

The SPDIF is composed by:

System Interface

The system interface implements the AHB slave operation. It contains not only control registers of transmitters and receiver inside but also interrupt and DMA handshaking interface.

Clock Divider

The clock divider implements clock generation function. It divides the the source clock MCLK to generate the working clock used for the digital audio data transformation and

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transmission.

Parallel Audio Buffer

The parallel audio buffer stores the audio data to be transmitted. The size of the FIFO is 32bits x 32.

Serial Audio Converter

The serial audio converter converts the parallel audio data from the parallel audio buffer to the serial audio data.

Biphase Audio Generator

The biphase audio generator reads serial audio data from the serial audio converter and generates biphase audio data based on IEC-60958 standard.

22.3 Function description

22.3.1 Frame Format

A frame is uniquely composed of two sub-frames. For linear coded audio applications, the rate of transmission of frames corresponds exactly to the source sampling frequency.
In the 2-channel operation mode, the samples taken from both channels are transmitted by time multiplexing in consecutive sub-frames. The first sub-frame(left channel in stereophonic operation and primary channel in monophonic operation) normally use preamble M. However, the preamble is changed to preamble B once every 192 frame to identify the start of the block structure used to organize the channel status information.
The second sub-frame (right in stereophonic operation and secondary channel in monophonic operation) always use preamble W.

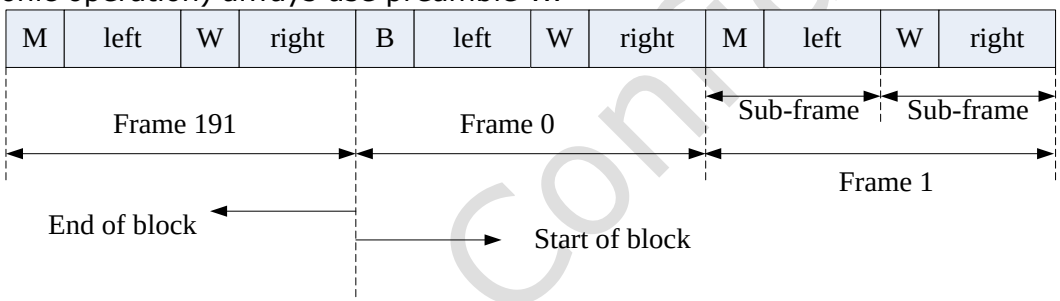


Fig. 22-2 SPDIF Frame Format

In the single channel operation mode in a professional application, the frame format is the same as in the 2-channel mode. Data is carried only in the first sub-frame and may be duplicated in the second sub-frame. If the second sub-frame is not carrying duplicate data, then time slot 28 (validity flag) shall be set to logical '1' (not valid).

22.3.2 Sub-frame Format

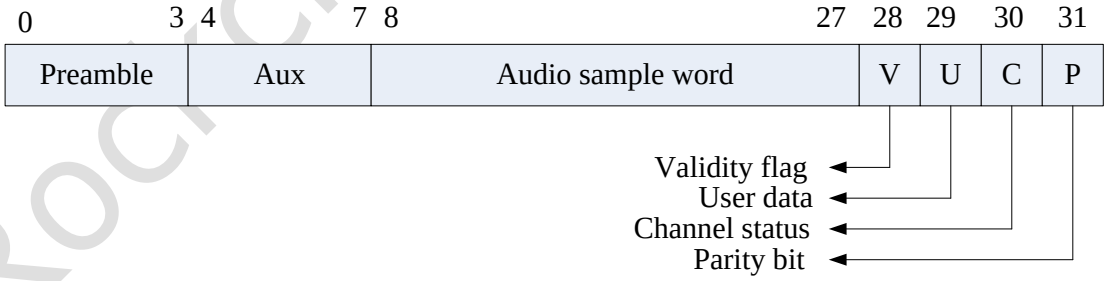


Fig. 22-3 SPDIF Sub-frame Format

Each sub-frame is divided into 32 time slots, numbered from 0 to 31. Time slot 0 to 3 carries one of the three permitted preambles. Time slot 4 to 27 carry the audio sample word in linear 2's complement representation. The MSB is carried by time slot 27. When a 24-bit coding range is used, the LSB is in time slot 4. When a 20-bit coding range is used, time slot 8 to 27 carry the audio sample word with the LSB in time slot 8.Time slot 4 to 7 may be used for other application. Under these circumstances, the bits in the time slot 4 to 7 are designated auxiliary sample bits.
If the source provides fewer bits than the interface allows (either 24 or 20),the unused LSBs are set to a logical '0'. For a non-linear PCM audio application or a data application the main data field may carry any other information. Time slot 28 carries the validity flag

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associated with the main data field. Time slot 29 carries 1 bit of the user data associated with the audio channel transmitted in the same sub-frame. Time slot 30 carries one bit of the channel status words associated with the main data field channel transmitted in the same sub-frame. Time slot 31 carries a parity bit such that time slots 4 to 31 inclusive carries an even number of ones and an even number of zeros.

22.3.3 Channel Coding

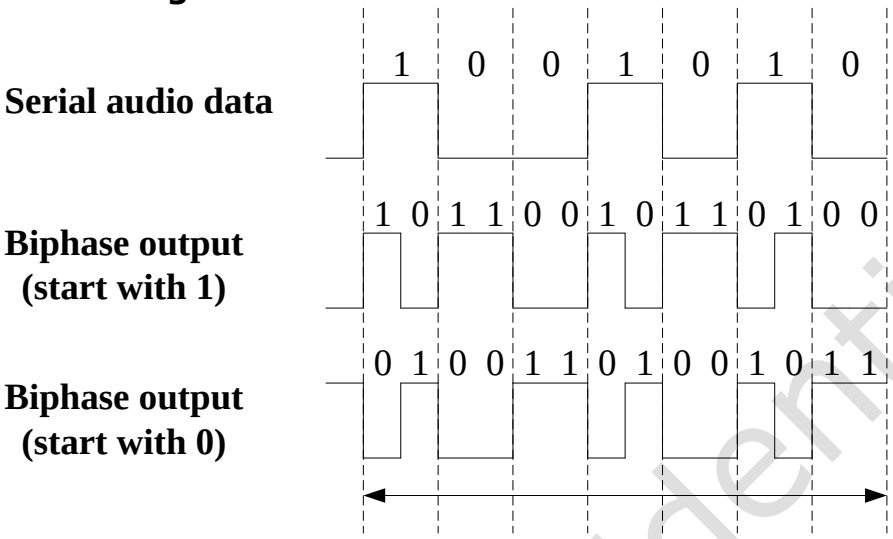


Fig. 22-4 SPDIF Channel Coding

To minimize the direct current component on the transmission line, to facilitate clock recovery from the data stream and to make the interface insensitive to the polarity of connections, time slots 4 to 31 are encoded in biphase-mark.

Each bit to be transmitted is represented by a symbol comprising two consecutive binary states. The first state of a symbol is always different from the second state of the previous symbol. The second state of the symbol is identical to the first if the bit to be transmitted is logical '0'.However, it is different from the first if the bit is logical '1'.

22.3.4 Preamble

Preambles are specific patterns providing synchronization and identification of the sub-frames and blocks.

To achieve synchronization within one sampling period and to make this process completely reliable, these patterns violate the biphase-mark code rules, thereby avoiding the possibility of data imitating the preambles.

A set of three preambles is used. These preambles are transmitted in the time allocated to four time slots (time slots 0 to 3) and are represented by eight successive states. The first state of the preamble is always different from the second state of the previous symbol.

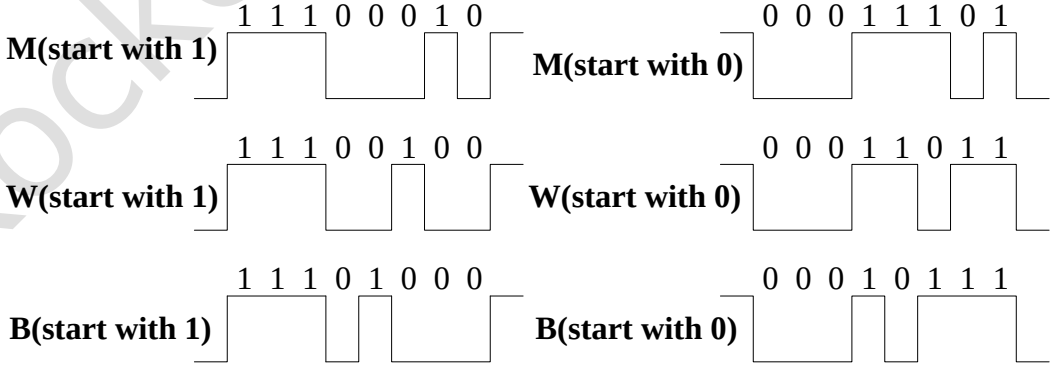


Fig. 22-5 SPDIF Preamble

Like biphase code, these preambles are dc free and provide clock recovery. They differ in at least two states from any valid biphase sequence.

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22.4 Register Description

22.4.1 Registers Summary

Name	Offset	Size	Reset Value	Description
SPDIF_CFGR	0x0000	W	0x00000000	Transfer Configuration Register
SPDIF_SDBLR	0x0004	W	0x00000000	Sample Date Buffer Level Register
SPDIF_DMACR	0x0008	W	0x00000000	DMA Control Register
SPDIF_INTCR	0x000c	W	0x00000000	Interrupt Control Register
SPDIF_INTSR	0x0010	W	0x00000000	Interrupt Status Register
SPDIF_XFER	0x0018	W	0x00000000	Transfer Start Register
SPDIF_SMPDR	0x0020	W	0x00000000	Sample Data Register
SPDIF_VLDFRn	0x0060	W	0x00000000	Validity Flag Register n
SPDIF_USRDRn	0x0090	W	0x00000000	User Data Register n
SPDIF_CHNSRn	0x00c0	W	0x00000000	Channel Status Register n
SPDIF_BURTSINFO	0x00d0	W	0x00000000	Channel Burst Info Register
SPDIF_REPETTION	0x0104	W	0x00000000	Channel Repetition Register
SPDIF_BURTSINFO_SHD	0x0108	W	0x00000000	Shadow Channel Burst Info Register
SPDIF_REPETTION_SHD	0x010c	W	0x00000000	Shadow Channel Repetition Register
SPDIF_USRDR_SHDn	0x0190	W	0x00000000	Shadow User Data Register n

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

22.4.2 Detail Register Description

SPDIF_CFGR

Address: Operational Base + offset (0x0000)

Transfer Configuration Register

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:16	RW	0x00	MCD mclk divider Fmclk/Fsdo This parameter can be calculated by Fmclk/(Fs*128). Fs=the sample frequency be wanted
15:9	RO	0x0	reserved
8	RW	0x0	PCMTYPE PCM type 0: linear PCM 1: non-linear PCM
7	WO	0x0	CLR mclk domain logic clear Write 1 to clear mclk domain logic. Read return zero.

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Bit	Attr	Reset Value	Description
6	RW	0x0	CSE Channel status enable 0: disable 1: enable The bit should be set to 1 when the channel conveys non-linear PCM
5	RW	0x0	UDE User data enable 0: disable 1: enable
4	RW	0x0	VFE Validity flag enable 0: disable 1: enable
3	RW	0x0	ADJ audio data justified 0: Right justified 1: Left justified
2	RW	0x0	HWT Halfword word transform enable 0: disable 1: enable It is valid only when the valid data width is 16bit.
1:0	RW	0x0	VDW Valid data width 00: 16bit 01: 20bit 10: 24bit 11: reserved The valid data width is 16bit only for non-linear PCM

SPDIF_SDBLR
Address: Operational Base + offset (0x0004)
Sample Date Buffer Level Register

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5:0	RW	0x00	SDBLR Sample Date Buffer Level Register Contains the number of valid data entries in the sample data buffer.

SPDIF_DMACR
Address: Operational Base + offset (0x0008)
DMA Control Register

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Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5	RW	0x0	TDE Transmit DMA Enable 0: Transmit DMA disabled 1: Transmit DMA enabled
4:0	RW	0x00	TDL Transmit Data Level This bit field controls the level at which a DMA request is made by the transmit logic. It is equal to the watermark level; that is, the dma_tx_req signal is generated when the number of valid data entries in the Sample Date Buffer is equal to or below this field value

SPDIF_INTCR

Address: Operational Base + offset (0x000c)

Interrupt Control Register

Bit	Attr	Reset Value	Description
31:18	RO	0x0	reserved
17	W1C	0x0	UDTIC User Data Interrupt Clear Write '1' to clear the user data interrupt.
16	W1C	0x0	BTTIC Block/Data burst transfer finish interrupt clear Write 1 to clear the interrupt.
15:10	RO	0x0	reserved
9:5	RW	0x00	SDBT Sample Date Buffer Threshold Sample Date Buffer Threshold for empty interrupt
4	RW	0x0	SDBEIE Sample Date Buffer empty interrupt enable 0: disable 1: enable
3	RW	0x0	BTTIE Block transfer/repetition period end interrupt enable When enabled, an interrupt will be asserted when the block transfer is finished if the channel conveys linear PCM or when the repetition period is reached if the channel conveys non-linear PCM. 0: disable 1: enable

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Bit	Attr	Reset Value	Description
2	RW	0x0	UDTIE User Data Interrupt 0: disable 1: enable If enabled, an interrupt will be asserted when the content of the user data register is fed into the corresponding shadow register
1:0	RO	0x0	reserved

SPDIF_INTSR
Address: Operational Base + offset (0x0010)
Interrupt Status Register

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4	RW	0x0	SDBEIS Sample Date Buffer empty interrupt status 0: inactive 1: active
3	RW	0x0	BTTIS Block/Data burst transfer interrupt status 0: inactive 1: active
2	RW	0x0	UDTIS User Data Interrupt Status 0: inactive 1: active
1:0	RO	0x0	reserved

SPDIF_XFER
Address: Operational Base + offset (0x0018)
Transfer Start Register

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	XFER Transfer Start Register Transfer Start Register

SPDIF_SMPDR
Address: Operational Base + offset (0x0020)
Sample Data Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	SMPDR Sample Data Register Sample Data Register

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SPDIF_VLDFRn
Address: Operational Base + offset (0x0060)
Validity Flag Register n

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	VLDFR_SUB_1 Validity Flag Subframe 1 Validity Flag Register 0
15:0	RW	0x0000	VLDFR_SUB_0 Validity Flag Subframe 0 Validity Flag for Subframe 0

SPDIF_USRDRn
Address: Operational Base + offset (0x0090)
User Data Register n

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	USR_SUB_1 User Data Subframe 1 User Data Bit for Subframe 1
15:0	RW	0x0000	USR_SUB_0 User Data Subframe 0 User Data Bit for Subframe 0

SPDIF_CHNSRn
Address: Operational Base + offset (0x00c0)
Channel Status Register n

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	CHNSR_SUB_1 Channel Status Subframe 1 Channel Status Bit for Subframe 1
15:0	RW	0x0000	CHNSR_SUB_0 Channel Status Subframe 0 Channel Status Bit for Subframe 0

SPDIF_BURTSINFO
Address: Operational Base + offset (0x00d0)
Channel Burst Info Register

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	PD pd Preamble Pd for non-linear pcm, indicating the length of burst payload in unit of bytes or bits.
15:13	RW	0x0	BSNUM Bitstream Number This field indicates the bitstream number. Usually the bitstream number is 0.

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Bit	Attr	Reset Value	Description
12:8	RW	0x00	DATAINFO Data-type-dependent info This field gives the data-type-dependent info
7	RW	0x0	ERRFLAG Error Flag 0: indicates a valid burst-payload 1: indicates that the burst-payload may contain errors
6:0	RW	0x00	DATATYPE Data type 0000000: null data 0000001: AC-3 data 0000011: Pause data 0000100: MPEG-1 layer 1 data 0000101: MPEG-1 layer 2 or 3 data or MPEG-2 without extension 0000110: MPEG-2 data with extension 0000111: MPEG-2 AAC 0001000: MPEG-2, layer-1 low sampling frequency 0001001: MPEG-2, layer-2 low sampling frequency 0001010: MPEG-2, layer-3 low sampling frequency 0001011: DTS type I 0001100: DTS type II 0001101: DTS type III 0001110: ATRAC 0001111: ATRAC 2/3 0010000: ATRAC-X 0010001: DTS type IV 0010010: WMA professional type I 0110010: WMA professional type II 1010010: WMA professional type III 1110010: WMA professional type IV 0010011: MPEG-2 AAC low sampling frequency 0110011: MPEG-2 AAC low sampling frequency 1010011: MPEG-2 AAC low sampling frequency 1110011: MPEG-2 AAC low sampling frequency 0010100: MPEG-4 AAC 0110100: MPEG-4 AAC 1010100: MPEG-4 AAC 1110100: MPEG-4 AAC 0010101: Enhanced AC-3 0010110: MAT others: reserved

SPDIF_REPETTION
Address: Operational Base + offset (0x0104)
Channel Repetition Register

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Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0000	REPETTION Repetition This define the repetition period when the channel conveys non-linear PCM

SPDIF_BURTSINFO_SHD

Address: Operational Base + offset (0x0108)

Shadow Channel Burst Info Register

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	PD pd Preamble Pd for non-linear pcm, indicating the length of burst payload in unit of bytes or bits.
15:13	RO	0x0	BSNUM Bitstream Number This field indicates the bitstream number. Usually the bitstream number is 0.
12:8	RO	0x00	DATAINFO Data-type-dependent info This field gives the data-type-dependent info
7	RO	0x0	ERRFLAG Error Flag 0: indicates a valid burst-payload 1: indicates that the burst-payload may contain errors

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Bit	Attr	Reset Value	Description
6:0	RO	0x00	DATATYPE Data type 0000000: null data 0000001: AC-3 data 0000011: Pause data 0000100: MPEG-1 layer 1 data 0000101: MPEG-1 layer 2 or 3 data or MPEG-2 without extension 0000110: MPEG-2 data with extension 0000111: MPEG-2 AAC 0001000: MPEG-2, layer-1 low sampling frequency 0001001: MPEG-2, layer-2 low sampling frequency 0001010: MPEG-2, layer-3 low sampling frequency 0001011: DTS type I 0001100: DTS type II 0001101: DTS type III 0001110: ATRAC 0001111: ATRAC 2/3 0010000: ATRAC-X 0010001: DTS type IV 0010010: WMA professional type I 0110010: WMA professional type II 1010010: WMA professional type III 1110010: WMA professional type IV 0010011: MPEG-2 AAC low sampling frequency 0110011: MPEG-2 AAC low sampling frequency 1010011: MPEG-2 AAC low sampling frequency 1110011: MPEG-2 AAC low sampling frequency 0010100: MPEG-4 AAC 0110100: MPEG-4 AAC 1010100: MPEG-4 AAC 1110100: MPEG-4 AAC 0010101: Enhanced AC-3 0010110: MAT others: reserved

SPDIF_REPETTION_SHD
Address: Operational Base + offset (0x010c)
Shadow Channel Repetition Register

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
15:0	RO	0x0000	REPETTION Repetition This register provides the repetition of the bitstream when channel conveys non-linear PCM. In the design, it is define the length between Pa of the two consecutive data-burst. For the same audio format, the definition is different. Please convert the actual repetition in order to comply with the design.

SPDIF_USRDR_SHDn
Address: Operational Base + offset (0x0190)
Shadow User Data Register n

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	USR_SUB_1 User Data Subframe 1 User Data Bit for Subframe 1
15:0	RO	0x0000	USR_SUB_0 User Data Subframe 0 User Data Bit for Subframe 0

22.5 Interface Description

Table 22-1 Input clock description in clock architecture diagram

Module Pin	Dir.	Pad Name	IOMUX Setting
spdif_tx	O	SPDIFtx_GPIO3d3	GRF_GPIO3D_IOMUX[6]=1'b11

Notes: I=input, O=output, I/O=input/output, bidirectional

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22.6 Application Notes

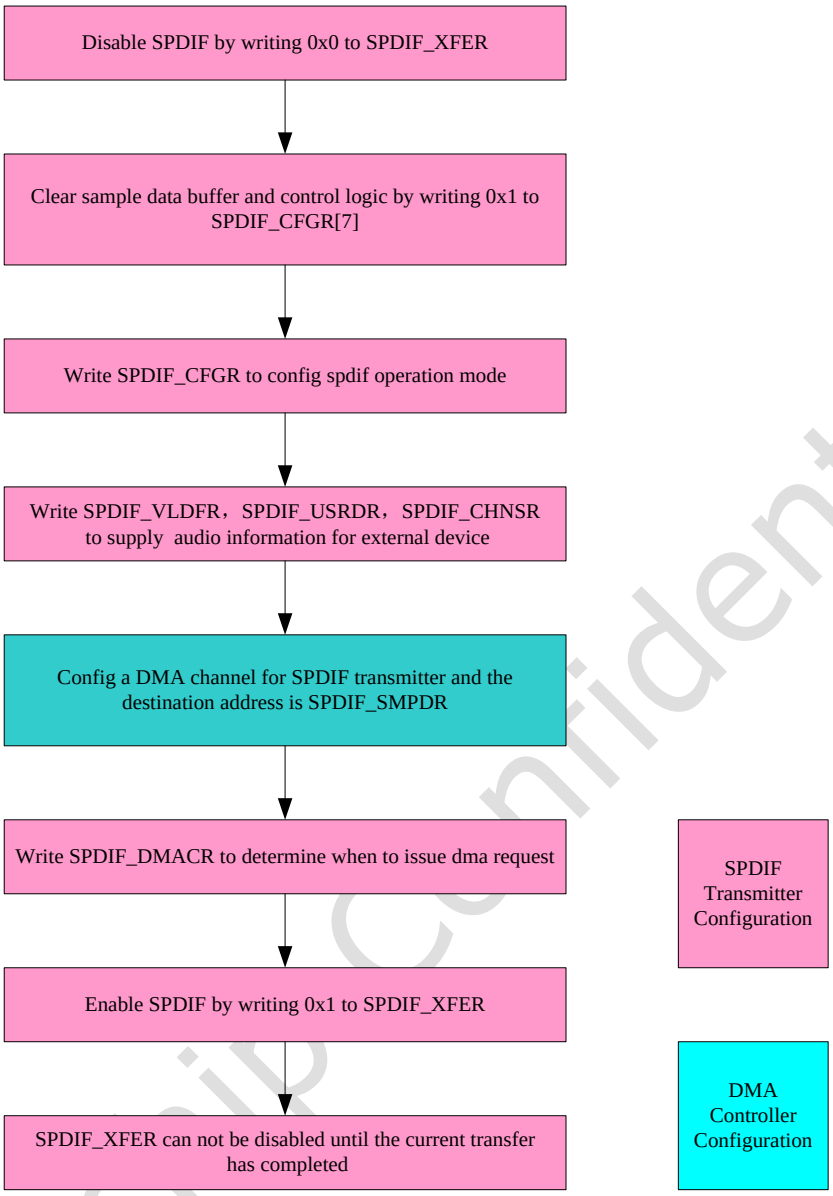


Fig. 22-6 SPDIF transmitter operation flow chart

The above figure shows the operation flow of SPDIF operation. Note that the configuration register can be written only when the transfer is stopped.

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Chapter 23 Smart Card Reader

23.1 Overview

The Smart Card Reader (SCR) is a communication controller that transmits data between the superior system and the Smart Card. The controller can perform a complete smart card session, including card activation, card deactivation, cold/warm reset, Answer to Reset (ATR) response reception, data transfers, etc.
The SCR support the following main features:

- Supports the ISO/IEC 7816-3:1997(E) and EMV2000 (4.0) specifications
- Performs functions needed for complete smart card sessions, including:
  - Card activation and deactivation
  - Cold/warm reset
  - Answer to Reset (ATR) response reception
  - Data transfers to and from the card
- Extensive interrupt support system
- Adjustable clock rate and bit (baud) rate
- Configurable automatic byte repetition
- Handles commonly used communication protocols:
  - T=0 for asynchronous half-duplex character transmission
  - T=1 for asynchronous half-duplex block transmission
- Automatic convention detection
- Configurable timing functions:
  - Smart card activation time
  - Smart card reset time
  - Guard time
  - Timeout timers
- Automatic operating voltage class selection
- Supports synchronous and any other non-ISO 7816 and non-EMV cards
- Advanced Peripheral Bus (APB) slave interface for easy integration with AMBA-based host systemsBlock Diagram

23.2 Block Diagram

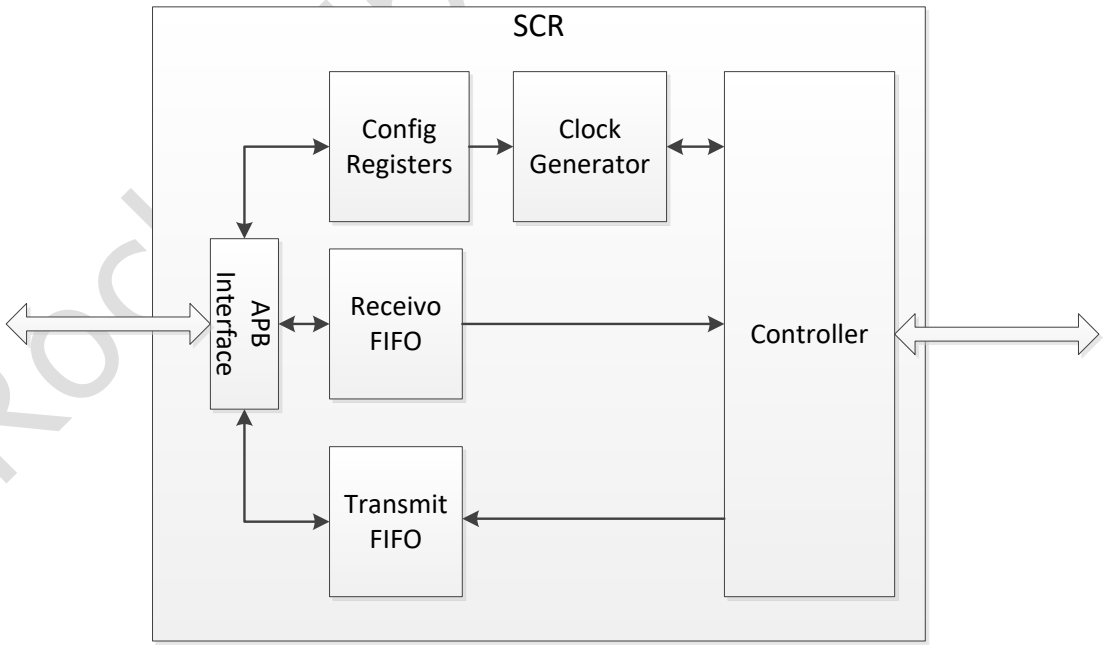


Fig. 23-1 SCR Block Diagram

The host processor gets access to PWM Register Block through the APB slave interface.

23.2.1 APB Interface

The host processor gets access to PWM Register Block through the APB slave interface.

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23.2.2 Configuration Registers
The Configuration Registers block provides control over all functions of the Smart Card Reader

23.2.3 Controller
The Controller is the main block in the SCR core. This block controls receiving characters transmitted by the Smart Card, storing them in the RX FIFO, and transmitting them to the Smart Card. This block also performs card activation, deactivation, and cold and warm reset. After the card is reset, the Answer To Reset (ATR) sequence is received by the controller and stored in RX FIFO.
The parallel to serial conversion needed to transmit data from a Smart Card Reader to a Smart Card and the serial to parallel conversion needed to transmit data in the opposite direction is performed by the UART. The UART also performs the guardtime, parity checking and character repeating functions.

23.2.4 Receive FIFO
The Receive FIFO is used to store the data received from the Smart Card until the data is read out by the superior system.

23.2.5 Transmit FIFO
The Transmit FIFO is used to store the data to be transmitted to the Smart Card.

23.2.6 Clock Generator
The Clock Generator generates the Smart Card Clock signal and the Baud Clock Impulse signal, used in timing the Smart Card Reader.)

23.3 Function Description

A Smart Card session consists of following stages:
1. Smart Card insertion
2. Activation of contacts and cold reset sequence
3. Answer To Reset sequence (ATR)
4. Execution of transaction
5. Deactivation of contacts
6. Smart Card removal

23.3.1 Smart Card Insertion
A Smart Card session starts with the insertion of the Smart Card. This event is signaled to the SCR using the SCDETECT input. The SCPRESENT bit is set and also the SCINS interrupt is asserted (if enabled).
When the external card detect switch is not used, the input pin SCDETECT mustbe tied to inactive state.

23.3.2 Automatic operating voltage class selection
There are three operating classes (1.8V - class C, 3V - class B and 5V - class A) defined in ISO/IEC 7816-3(2006) specification. Only 1.8V and 3.3V are supported by the SCR.
Before the activation of contacts, operating classes have to be enabled via bits VCC18, VCC33 in CTRL2 register. In case that no operating class is enabled, the controller performs activation for all two voltage classes (1.8V, 3V) in sequence.
When Smart Card Reader performs activation of contacts the lowest enabled voltage class is automatically applied first. When the first character start bit of ATR sequence is received, the selected voltage class is correct (even if the ATR is then received with errors). When the ATR sequence reception does not start, ATRFAIL interrupt is not activated, deactivation is performed and next higher enabled voltage class is applied. If the ATR sequence reception does not start and no other higher class is enabled was already applied the ATRFAIL interrupt is activated and the last applied voltage class remains active.
After the automatic voltage class selection is finished the selected class can be read from bits VCC18, VCC33 in CTRL2 register. If the automatic voltage class selection fails, these bits remain untouched.
There is a delay applied between deactivation of contacts with lower voltage class and activation of contacts with higher voltage class. This delay should be at least 10 ms according to the ISO/IEC 7816-3 specification.

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23.3.3 Activation of Contacts and Cold Reset Sequence

When the Smart Card is properly inserted and the ACT bit in CTRL2 register is asserted, the activation of contacts can be started. The duration of each part of the activation is the time Ta, which is equal to the ADEATIME register value. If no Vpp is necessary, the activation and deactivation part of Vpp can be omitted by clearing the AUTOADEAVPP bit in SCPADS register.

The Cold Reset sequence follows immediately after the activation. Time (Tc) is the duration of the Reset. The EMV specification recommends that this value should be between 40000 and 45000. The activation of contacts and cold reset sequence is shown in Fig.1-2.

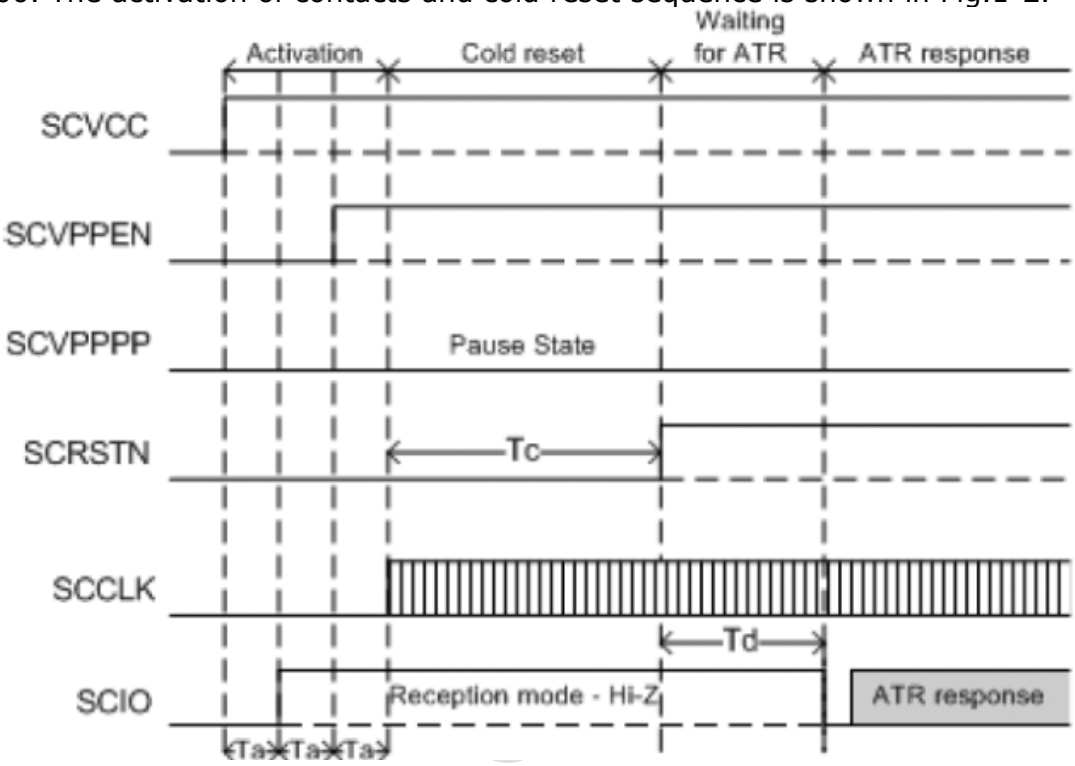


Fig. 23-2 Activation, Cold Reset and ATR

23.3.4 Execution of Transaction

All transfers between the Smart Card Reader and a Smart Card are under the control of the superior system. It controls the number of characters sent to the Smart Card and it knows the number of characters expected to be returned from the Smart Card.

23.3.5 Warm Reset

The Warm Reset sequence is initialized by setting the WRST bit in the CTRL2 register to '1'.Smart Card Reader drives the SCRSTN signal to '0' to perform the Warm Reset as shown in Fig. 1 3. After the SCRSTN assertion, the Warm Reset sequence then continues the same way as the Cold Reset sequence.

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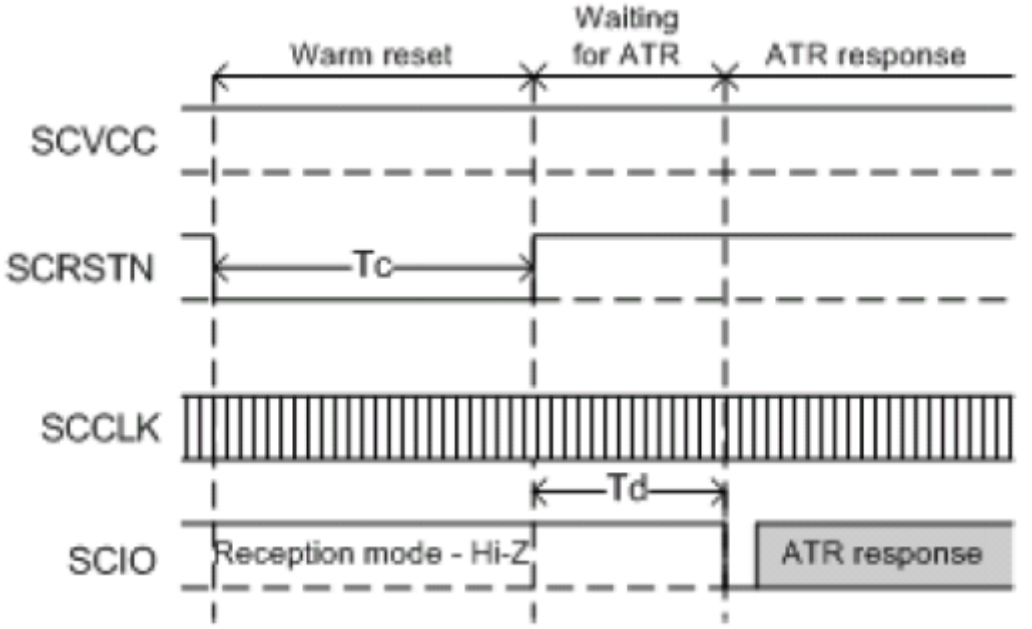


Fig. 23-3 Warm Reset and ATR

23.3.6 Deactivation of Contacts

After the smart card reader detects the removal of the smart card (SCREM interrupt) or the superior system initiates deactivation by setting the DEACT bit in the CTRL2 register to '1', the deactivation is performed immediately as shown in . The duration time (Ta), of each part of the deactivation sequence time is defined in the ADEATIME register.

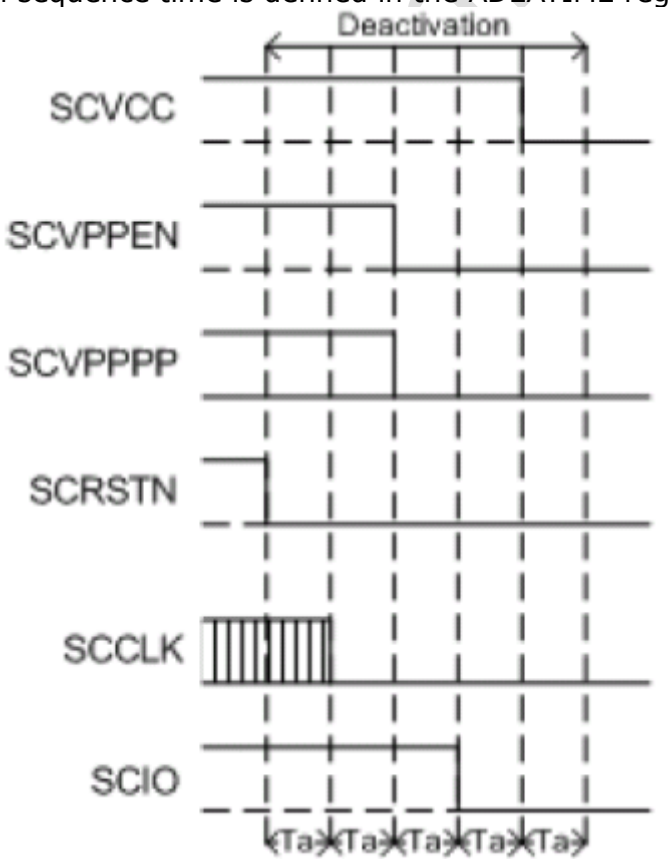


Fig. 23-4 Deactivation Sequence

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23.4 Register Description

23.4.1 Registers Summary

Name	Offset	Size	Reset Value	Description
SCR_CTRL1	0x0000	HW	0x0000	Control Register 1
SCR_CTRL2	0x0004	HW	0x0000	Control Register 2
SCR_SCPADS	0x0008	HW	0x0000	Smart Card Pads Register
SCR_INTEN1	0x000c	HW	0x0000	Interrupt Enable Register 1
SCR_INTSTAT1	0x0010	HW	0x0000	Interrupt Status Register 1
SCR_FIFOCTRL	0x0014	HW	0x0000	FIFO Control Register
SCR_LEGTXFICNT	0x0018	B	0x00	Legacy TX FIFO Counter
SCR_LEGRXFICNT	0x0019	B	0x00	Legacy RX FIFO Counter
SCR_RXFITH	0x001c	HW	0x0000	RX FIFO Threshold
SCR_REP	0x0020	B	0x00	Repeat
SCR_SCCDDIV	0x0024	HW	0x0000	Smart Card Clock Divisor
SCR_BAUDDIV	0x0028	HW	0x0000	Baud Clock Divisor
SCR_SCGUTIME	0x002c	B	0x00	Smart Card Guardtime
SCR_ADEATIME	0x0030	HW	0x0000	Activation / Deactivation Time
SCR_LOWRSTTIME	0x0034	HW	0x0000	Reset Duration
SCR_ATRSTARTLIMIT	0x0038	HW	0x0000	ATR Start Limit
SCR_C2CLIM	0x003c	HW	0x0000	Two Characters Delay Limit
SCR_INTEN2	0x0040	HW	0x0000	Interrupt Enable Register 2
SCR_INTSTAT2	0x0044	HW	0x0000	Interrupt Status Register 2
SCR_TXFITH	0x0048	HW	0x0000	TX FIFO Threshold
SCR_TXFIFOCNT	0x004c	HW	0x0000	TX FIFO Counter
SCR_RXFIFOCNT	0x0050	HW	0x0000	RX FIFO Counter
SCR_BAUDTUNE	0x0054	B	0x00	Baud Tune Register
SCR_FIFO	0x0200	B	0x00	FIFO

*Notes: Size: **B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

23.4.2 Detail Register Description

SCR_CTRL1

Address: Operational Base + offset (0x0000)

Control Register 1

Bit	Attr	Reset Value	Description
15	RW	0x0	GINTEN Global Interrupt Enable When high, INTERRUPT output assertion is enabled.
14	RO	0x0	reserved
13	RW	0x0	TCKEN TCK enable When enabled all ATR bytes beginning from T0 are being XOR-ed. The result must be equal to TCK byte (when present). If the TCK byte does not match the computed value the ATR is considered to be malformed.

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Bit	Attr	Reset Value	Description
12	RW	0x0	ATRSTFLUSH ATR Start Flush FIFO When enabled, both FIFOs are flushed before the ATR is started.
11	RW	0x0	T0T1 T0/T1 Protocol Controls the using of T=0 or T=1 protocol. No character repeating is used when T=1 protocol is selected. The Character Guardtime (minimum delay between the leading edges of two consecutive characters) is reduced to 11 ETU when T=1 protocol is used and Guardtime value N = 255. The delay between the leading edge of the last received character and the leading edge of the first character transmitted is 16 ETU when T=0 protocol is used and 22 ETU when T=1 protocol is used.
10	RW	0x0	TS2FIFO TS to FIFO Enables to store the first ATR character TS in RX FIFO. During ideal card session there is no necessity to store TS character, so it can be disabled
9	RW	0x0	RXEN Receiving enable When enabled the characters sent by the Smart Card are received by the UART and stored in RX FIFO. Receiving is internally disabled while a transmission is in progress.
8	RW	0x0	TXEN Transmission enable When enabled the characters are read from TX FIFO and transmitted through UART to the Smart Card
7	RW	0x0	CLKSTOPVAL Clock Stop Value The value of the scclk output during the clock stop state.
6	RW	0x0	CLKSTOP Clock Stop Clock Stop. When this bit is asserted and the smart card I/O line is in ‘Z’ state, the SCR core stops driving of the smart card clock signal after the CLKSTOPDELAY time expires. The smart card clock is restarted immediately after the CLKSTOP signal is deserted. New character transmission can be started by superior system after the CLKSTARTDELAY time expires. The expiration of both times is signaled by the CLKSTOPRUN bit in the Interrupt registers. Reading '1' from this bit signals that the clock is stopped or CLKSTARTDELAY time not expired yet. Reading '0' from this bit signals that the clock is not stopped.
5:3	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
2	RW	0x0	PECH2FIFO Character With Wrong Parity to FIFO Enables storage of the characters received with wrong parity in RX FIFO.
1	RW	0x0	INVORD Inverse Bit Ordering When High, inverse bit ordering convention(MSB-LSB) is used.
0	RW	0x0	INVLEV Inverse Bit Level When high, inverse level convention is used(A= '1', Z='0');

SCR_CTRL2

Address: Operational Base + offset (0x0004)

Control Register 2

Bit	Attr	Reset Value	Description
15:8	RO	0x00	Reserved3 Reserved Reserved bits are hard-wired to zero
7	RW	0x0	VCC50 Control 5V Smart Card Vcc Control 5V Smart Card Vcc. Setting of this bit allows selection of 5V Vcc for Smart Card session (Class A). After the selection of operating class is completed, this bit is in '1'.if this class was selected. Default value after reset is '0'..
6	RW	0x0	VCC33 Control 3V Smart Card Vcc Setting of this bit allows selection of 3V Vcc for Smart Card session (Class B). After the selection of operating class is completed, this bit is in '1'.if this class was selected. Default value after reset is '0'.
5	RW	0x0	VCC18 Control 1.8V Smart Card Vcc Control 1.8V Smart Card Vcc. Setting of this bit allows selection of 1.8V Vcc for Smart Card session (Class C). After the selection of operating class is completed, this bit is in '1'.if this class was selected. Default value after reset is '0'.
4	RW	0x0	DEACT Deactivation Setting of this bit initializes the deactivation sequence. When the deactivation is finished, the DEACT bit is automatically cleared.
3	RW	0x0	ACT Activation Setting of this bit initializes the activation sequence. When the activation is finished, the ACT bit is automatically cleared.

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Bit	Attr	Reset Value	Description
2	WO	0x0	WARMRST Warm Reset Command Writing '1'.to this bit initializes Warm Reset of the Smart Card. This bit is always read as '0'.
1:0	RO	0x0	reserved

SCR_SCPADS
Address: Operational Base + offset (0x0008)
Smart Card Pads Register

Bit	Attr	Reset Value	Description
15:10	RO	0x0	reserved
9	RO	0x0	SCPRESENT Smart Card presented This bit is set to '1'.when the SCDETECT input is active at least for SCDETECTTIME
8	RW	0x0	DSCFCB Direct Smart Card Function Code Bit It provides direct access to SCFCB output
7	RW	0x0	DSCVPPPP Direct Smart Card Vpp Pause/Prog It provides direct access to SCVPPPP output
6	RW	0x0	DSCVPPEN Direct Smart Card Vpp Enable It provides direct access to SCVPPEN output
5	RW	0x0	AUTOADEAVPP Automatic Vpp Handling. When high, it enables automatic handling of DSCVPPEN and DSCVPPPP signals during activation and deactivation sequence.
4	RW	0x0	DSCVCC Direct Smart Card Vcc Direct Smart Card Vcc. When DIRACCPADS = '1', the DSCVCC bit provides direct access to SCVCCx outputs. The appropriate SCVCC18, SCVCC33 and SCVCC50 outputs are driven according to state of bits VCC18, VCC33 and VCC50 in CTRL2 register.
3	RW	0x0	DSCRST Direct Smart Card Reset When DIRACCPADS = '1'., the DSCRST bit provides direct access to SCRST output
2	RW	0x0	DSCCLK Direct Smart Card Clock When DIRACCPADS = '1'., the DSCCLK bit provides direct access to SCCLK output
1	RW	0x0	DSCIO Direct Smart Card Input/Output When DIRACCPADS = '1', the DSCIO bit provides direct access to SCIO pad.

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Bit	Attr	Reset Value	Description
0	RW	0x0	DIRACCPADS Direct Access To Smart Card Pads When high, it disables a serial interface functionality and enables direct control of the smart card pads using following 4 bits.

SCR_INTEN1
Address: Operational Base + offset (0x000c)
Interrupt Enable Register 1

Bit	Attr	Reset Value	Description
15	RW	0x0	SCDEACT Smart Card Deactivation Interrupt When enabled, this interrupt is asserted after the Smart Card deactivation sequence is complete.
14	RW	0x0	SCACT Smart Card Activation Interrupt. When enabled, this interrupt is asserted after the Smart Card activation sequence is complete.
13	RW	0x0	SCINS Smart Card Inserted Interrupt When enabled, this interrupt is asserted after the smart card insertion
12	RW	0x0	SCREM Smart Card Removed Interrupt. When enabled, this interrupt is asserted after the smart card removal.
11	RW	0x0	ATRDONE ATR Done Interrupt When enabled, this interrupt is asserted after the ATR sequence is successfully completed.
10	RW	0x0	ATRFAIL ATR Fail Interrupt When enabled, this interrupt is asserted if the ATR sequence fails.
9	RW	0x0	RXTHRESHOLD RX FIFO Threshold Interrupt When enabled, this interrupt is asserted if the number of bytes in RX FIFO is equal or exceeds the RX FIFO threshold.
8	RW	0x0	C2CFULL Two Consecutive Characters Limit Interrupt When enabled, this interrupt is asserted if the time between two consecutive characters, transmitted between the Smart Card and the Reader in both directions, is equal the Two Characters Delay Limit described below. The C2CFULL interrupt is internally enabled from the ATR start to the deactivation or ATR restart initialization. It is recommended to use this counter to detect unresponsive Smart Cards.

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Bit	Attr	Reset Value	Description
7	RW	0x0	RXPERR Reception Parity Error Interrupt When enabled, this interrupt is asserted after the character with wrong parity was received when the number of repeated receptions exceeds RXREPEAT value or T=1 protocol is used
6	RW	0x0	TXPERR Transmission Parity Error Interrupt. When enabled, this interrupt is asserted if the Smart Card signals wrong character parity during the guardtime after the character transmission was repeated TXREPEAT-times
5	RW	0x0	RXDONE Reception Done Interrupt When enabled, this interrupt is asserted after a character was received from the Smart Card.
4	RW	0x0	TXDONE Transmission Done Interrupt When enabled, this interrupt is asserted after one character was transmitted to the Smart Card.
3	RW	0x0	CLKSTOPRUN Smart Card Clock Stop Interrupt When enabled, this interrupt is asserted in two cases: 1. When the smart card clock is stopped (after CLOCKSTOP assertion). 2. When the new character transfer can be started (the smart card clock is fully running after CLOCKSTOP de-assertion).
2	RW	0x0	RXFIFULL RX FIFO Full Interrupt When enabled, this interrupt is asserted if the RX FIFO is filled up.
1	RW	0x0	TXFIEMPTY TX FIFO Empty Interrupt. When enabled, this interrupt is asserted if the TX FIFO is emptied out.
0	RW	0x0	TXFIDONE TX FIFO Done Interrupt When enabled, this interrupt is asserted after all bytes from TX FIFO were transferred to the Smart Card

SCR_INTSTAT1
Address: Operational Base + offset (0x0010)
Interrupt Status Register 1

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Bit	Attr	Reset Value	Description
15	RW	0x0	SCDEACT Smart Card Deactivation Interrupt When enabled, this interrupt is asserted after the Smart Card deactivation sequence is complete.
14	RW	0x0	SCACT Smart Card Activation Interrupt. When enabled, this interrupt is asserted after the Smart Card activation sequence is complete.
13	RW	0x0	SCINS Smart Card Inserted Interrupt When enabled, this interrupt is asserted after the smart card insertion
12	RW	0x0	SCREM Smart Card Removed Interrupt. When enabled, this interrupt is asserted after the smart card removal.
11	RW	0x0	ATRDONE ATR Done Interrupt When enabled, this interrupt is asserted after the ATR sequence is successfully completed.
10	RW	0x0	ATRFAIL ATR Fail Interrupt When enabled, this interrupt is asserted if the ATR sequence fails.
9	RW	0x0	RXTHRESHOLD RX FIFO Threshold Interrupt When enabled, this interrupt is asserted if the number of bytes in RX FIFO is equal or exceeds the RX FIFO threshold.
8	RW	0x0	C2CFULL Two Consecutive Characters Limit Interrupt When enabled, this interrupt is asserted if the time between two consecutive characters, transmitted between the Smart Card and the Reader in both directions, is equal the Two Characters Delay Limit described below. The C2CFULL interrupt is internally enabled from the ATR start to the deactivation or ATR restart initialization. It is recommended to use this counter to detect unresponsive Smart Cards.
7	RW	0x0	RXPERR Reception Parity Error Interrupt When enabled, this interrupt is asserted after the character with wrong parity was received when the number of repeated receptions exceeds RXREPEAT value or T=1 protocol is used

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Bit	Attr	Reset Value	Description
6	RW	0x0	TXPERR Transmission Parity Error Interrupt. When enabled, this interrupt is asserted if the Smart Card signals wrong character parity during the guardtime after the character transmission was repeated TXREPEAT-times
5	RW	0x0	RXDONE Reception Done Interrupt When enabled, this interrupt is asserted after a character was received from the Smart Card.
4	RW	0x0	TXDONE Transmission Done Interrupt When enabled, this interrupt is asserted after one character was transmitted to the Smart Card.
3	RW	0x0	CLKSTOPRUN Smart Card Clock Stop Interrupt When enabled, this interrupt is asserted in two cases: 1. When the smart card clock is stopped (after CLOCKSTOP assertion). 2. When the new character transfer can be started (the smart card clock is fully running after CLOCKSTOP de-assertion).
2	RW	0x0	RXFIFULL RX FIFO Full Interrupt When enabled, this interrupt is asserted if the RX FIFO is filled up.
1	RW	0x0	TXFIEMPTY TX FIFO Empty Interrupt. When enabled, this interrupt is asserted if the TX FIFO is emptied out.
0	RW	0x0	TXFIDONE TX FIFO Done Interrupt When enabled, this interrupt is asserted after all bytes from TX FIFO were transferred to the Smart Card

SCR_FIFOCTRL
Address: Operational Base + offset (0x0014)
FIFO Control Register

Bit	Attr	Reset Value	Description
15:11	RO	0x0	reserved
10	WO	0x0	RXFIFLUSH Flush RX FIFO RX FIFO is flushed, when '1'.is written to this bit.
9	RO	0x0	RXFIFULL RX FIFO Full RX FIFO Full

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Bit	Attr	Reset Value	Description
8	RO	0x0	RXFIEMPTY RX FIFO Empty Field0000 Description
7:3	RO	0x0	reserved
2	WO	0x0	TXFIFLUSH Flush TX FIFO. TX FIFO is flushed, when '1'.is written to this bit.
1	RO	0x0	TXFIFULL TX FIFO Full TX FIFO Full
0	RO	0x0	TXFIEMPTY TX FIFO Empty. TX FIFO Empty.

SCR_LEGTXFICNT
Address: Operational Base + offset (0x0018)
Legacy TX FIFO Counter

Bit	Attr	Reset Value	Description
7:0	RO	0x00	LEGTXFICNT Legacy TX FIFO Counter It is equal to TX FIFO Counter up to value 255. All values above 255 are read as 255. It is recommended to use the 16-bit TX FIFO Counter instead of this register.

SCR_LEGRXFICNT
Address: Operational Base + offset (0x0019)
Legacy RX FIFO Counter

Bit	Attr	Reset Value	Description
7:0	RO	0x00	LEGRXFICNT Legacy RX FIFO Counter It is equal to RX FIFO Counter up to value 255. All values above 255 are read as 255. It is recommended to use the 16-bit RX FIFO Counter instead of this register.

SCR_RXFITH
Address: Operational Base + offset (0x001c)
RX FIFO Threshold

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	RXFITH RX FIFO Threshold The interrupt is asserted when the number of bytes it receives is equal to, or exceeds the threshold

SCR_REP
Address: Operational Base + offset (0x0020)

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Repeat

Bit	Attr	Reset Value	Description
7:4	RW	0x0	RXREP RX Repeat This is a 4-bit, read/write register that specifies the number of attempts to request character re-transmission after wrong parity was detected. The re-transmission of the character is requested using the 1 ETU long error signal during the guardtime
3:0	RW	0x0	TXREP TX Repeat This is a 4-bit, read/write register that specifies the number of attempts to re-transmit the character after the Smart Card signals the wrong parity during the guardtime.

SCR_SCCDDIV
Address: Operational Base + offset (0x0024)
Smart Card Clock Divisor

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	SCCDDIV Smart Card Clock Divisor This is a 16-bit, read/write register that defines the divisor value used to generate the Smart Card Clock from the system clock.

SCR_BAUDDIV
Address: Operational Base + offset (0x0028)
Baud Clock Divisor

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	BAUDDIV Baud Clock Divisor This is a 16-bit, read/write register that defines a divisor value used to generate the Baud Clock impulses from the system clock

SCR_SCGUTIME
Address: Operational Base + offset (0x002c)
Smart Card Guardtime

Bit	Attr	Reset Value	Description
7:0	RW	0x00	SCGUTI Smart Card Guardtime This is an 8-bit, read/write register that sets a delay at the end of each character transmitted from the Smart Card Reader to the Smart Card. The value is in Elementary Time Units (ETU). The parity error is besides signaled during the guardtime

SCR_ADEATIME
Address: Operational Base + offset (0x0030)
Activation / Deactivation Time

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Bit	Attr	Reset Value	Description
15:8	RW	0x00	ADEATIME Activation / Deactivation Time Sets the duration of each part of the activation and deactivation sequence. The value is in Smart Card Clock Cycles.
7:0	RW	0x00	Reserved Reserved Reserved bits are hard-wired to zero.

SCR_LOWRSTTIME
Address: Operational Base + offset (0x0034)
Reset Duration

Bit	Attr	Reset Value	Description
15:8	RW	0x00	LOWRSTTIME Reset Duration Sets the duration of the smart card reset sequence. This value is same for the cold and warm reset. The value is in terms of smart card clock cycles.
7:0	RW	0x00	Reserved Reserved Bits (7:0) of this register are hard-wired to zero.

SCR_ATRSTARTLIMIT
Address: Operational Base + offset (0x0038)
ATR Start Limit

Bit	Attr	Reset Value	Description
15:8	RW	0x00	ATRSTARTLIMIT ATR Start Limit Defines the maximum time between the rising edge of the SCRSTN signal and the start of ATR response. The value is in terms of smart card clock cycles
7:0	RW	0x00	Reserved Reserved Bits (7:0) of this register are hard-wired to zero

SCR_C2CLIM
Address: Operational Base + offset (0x003c)
Two Characters Delay Limit

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	C2CLIM Two Characters Delay Limit This is a 16-bit, read/write register that sets the maximum time between the leading edges of two, consecutive characters. The value is in ETUs.

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SCR_INTEN2
Address: Operational Base + offset (0x0040)
Interrupt Enable Register 2

Bit	Attr	Reset Value	Description
15:2	RO	0x0	reserved
1	RW	0x0	TCKERR TCK Error Interrupt. When enabled, this interrupt is asserted if the TCK byte does not match computed value.
0	RW	0x0	TXTHRESHOLD TX FIFO Threshold Interrupt When enabled, this interrupt is asserted if the number of bytes in TX FIFO is equal or less than the TX FIFO threshold.

SCR_INTSTAT2
Address: Operational Base + offset (0x0044)
Interrupt Status Register 2

Bit	Attr	Reset Value	Description
15:2	RO	0x0	reserved
1	RW	0x0	TCKERR TCK Error Interrupt When enabled, this interrupt is asserted if the TCK byte does not match computed value.
0	RW	0x0	TXTHRESHOLD TX FIFO Threshold Interrupt When enabled, this interrupt is asserted if the number of bytes in TX FIFO is equal or less than the TX FIFO threshold.

SCR_TXFITH
Address: Operational Base + offset (0x0048)
TX FIFO Threshold

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	TXFITH TX FIFO Threshold The interrupt is asserted when the number of bytes in TX FIFO is equal or less than the threshold

SCR_TXFIFOCNT
Address: Operational Base + offset (0x004c)
TX FIFO Counter

Bit	Attr	Reset Value	Description
15:0	RO	0x0000	TXFIFOCNT TX FIFO Counter This is a 16-bit, read-only register that provides the number of bytes stored in the RX FIFO

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SCR_RXFIFOCNT
Address: Operational Base + offset (0x0050)
RX FIFO Counter

Bit	Attr	Reset Value	Description
15:0	RO	0x0000	RXFIFOCNT RX FIFO Counter This is a 16-bit, read-only register that provides the number of bytes stored in the RX FIFO.

SCR_BAUDTUNE
Address: Operational Base + offset (0x0054)
Baud Tune Register

Bit	Attr	Reset Value	Description
7:4	RO	0x0	reserved
3:0	RW	0x0	BAUDTUNE Baud Tune Register This is a 3-bit, read/write register that defines an additional value used to increase the accuracy of the Baud Clock impulses

SCR_FIFO
Address: Operational Base + offset (0x0200)
FIFO

Bit	Attr	Reset Value	Description
7:0	RW	0x00	FIFO FIFO This is an 8-bit, read/write register that provides access to the receive and transmit FIFO buffers. The TX FIFO is accessed during the APB write transfer. The RX FIFO is accessed during the APB read transfer. All read/write accesses at address range 200h-3ffh are redirected to the FIFO.

23.5 Interface Description

Table 23-1 IOMUX Setting

Module Pin	IO	Pad Name	IOMUX Setting
SIM0			
sim_clk	O	SCclk_URT0sin_GPIO2d3	GPIO2D_IOMUX[7:6]= 2'b01
sim_rstn	O	SCrst_URT0sout_GPIO2d2	GPIO2D_IOMUX[5:4]= 2'b01
sim_data	I/O	SCio_URT0rtsn_GPIO0c1	GPIO0C_IOMUX[2]= 1'b1
sim_detect	O	SCdetect_URT0ctsn_GPIO2d5	GPIO2D_IOMUX[11:10]= 2'b01

Note:
- *I=input, O=output, I/O=input/output, bidirectional*
- *Pull up sim0/1 data pin when data transaction*

23.6 Application Notes

23.6.1 SCR Clock

The Smart Card Clock signal is used as the main clock for the smart card. Its frequency can

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be adjusted using the Smart Card Clock Divisor (SCCDIV). This value is used to divide the system clock.
The SCCLK frequency is given by the following equation:

$$\mathrm{SCCLK_{freq}} = \frac{CLK_freq}{2 * (SCCDIV + 1)}, \qquad SCCDIV \cong \frac{CLK_{freq}}{2 * SCCLK_{freq}} - 1$$

SCCLK_freq– Smart Card Clock Frequency
CLK_freq- System Clock Frequency
The Baud Clock Impulse signal is used to transmit and receive serial data between the Smart CardReader and the Smart Card. The baud rate can be modified using the Baud Clock Divisor (BAUDDIV) which is used to divide the system clock. The BAUDDIV value must be >= 4. The BAUD rate is given by the following equation:

$$\mathrm{BAUD_{rate}} = \frac{CLK_freq}{2 * (BAUDDIV + 1)}$$

The duration of one bit, Elementary Time Unit (ETU) and parameters F and D are defined in the ISO/IEC7816-3 specification.

$$\frac{1}{BAUD_rate} \cong ETU = \frac{F}{D} * \frac{1}{SCCLK_{freq}}, \frac{F}{D} \cong \frac{BAUDDIV + 1}{SCCDIV + 1}$$

BAUDDIV equation based on SCCDIV value and Smart Card parameters F and D is following:

$$\mathrm{BAUDDIV} \cong (\mathrm{SCCDIV} + 1) * \frac{F}{D} - 1$$

During the first answer to reset response after the cold reset, the initial ETU must be equal to 372 SmartCard Clock Cycles (given by parameters F=372 and D=1). In this case, the BAUDDIV should be:

$$\mathrm{BAUDDIV} \cong (\mathrm{SCCDIV} + 1) * \frac{372}{1} - 1$$

After the ATR is completed, the BAUDDIV register value can be changed according to Smart Card parameters F and D.
Baud Tune Register (BAUDTUNE) 3-bit value that can be used to increase the accuracy of the BaudClock impulses timing by using the BAUDTUNE Increment from Table listed below in combination with BAUDDIV register value.

Table 23-1 BAUDTUNE register

BAUDTUNE	000	001	010	011	100	101	110	111
$\mathrm{BAUDTUNE_{INCR}}$	+0	+0.125	0.25	+0.375	+0.5	+0.625	+0.75	+0.875

$$\mathrm{BAUDDIV} + \mathrm{BAUDTUNE}_{INCR} \cong (SCCDIV + 1) * \frac{F}{D} - 1$$

The BAUDDIV register value (nearest integer) can be computed using following equation:

$$\mathrm{BAUDDIV} \cong (\mathrm{SCCDIV} + 1) * \frac{F}{D} - 1 - BAUDTUNE_{INCR}$$

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Chapter 24 Serial Peripheral Interface (SPI)

24.1 Overview

The serial peripheral interface is an APB slave device. A four wire full duplex serial protocol from Motorola. There are four possible combinations for the serial clock phase and polarity. The clock phase (SCPH) determines whether the serial transfer begins with the falling edge of slave select signals or the first edge of the serial clock. The slave select line is held high when the SPI is idle or disabled. This SPI controller can work as either master or slave mode.

SPI Controller supports the following features:

- Support Motorola SPI,TI Synchronous Serial Protocol and National Semiconductor Micro wire interface
- Support 32-bit APB bus
- Support two internal 16-bit wide and 32-location deep FIFOs, one for transmitting and the other for receiving serial data
- Support two chip select signals in master mode
- Support 4,8,16 bit serial data transfer
- Support configurable interrupt polarity
- Support asynchronous APB bus and SPI clock
- Support master and slave mode
- Support DMA handshake interface and configurable DMA water level
- Support transmit FIFO empty, underflow, receive FIFO full, overflow, interrupt and all interrupts can be masked
- Support configurable water level of transmit FIFO empty and receive FIFO full interrupt
- Support combine interrupt output
- Support up to half of SPI clock frequency transfer in master mode and one sixth of SPI clock frequency transfer in slave mode
- Support full and half duplex mode transfer
- Stop transmitting SCLK if transmit FIFO is empty or receive FIFO is full in master mode
- Support configurable delay from chip select active to SCLK active in master mode
- Support configurable period of chip select inactive between two parallel data in master mode
- Support big and little endian, MSB and LSB first transfer
- Support two 8-bit audio data store together in one 16-bit wide location
- Support sample RXD 0~3 SPI clock cycles later
- Support configurable SCLK polarity and phase
- Support fix and incremental address access to transmit and receive FIFO

24.2 Block Diagram

The SPI Controller comprises with:

- AMBA APB interface and DMA Controller Interface
- Transmit and receive FIFO controllers and an FSM controller
- Register block
- Shift control and interrupt

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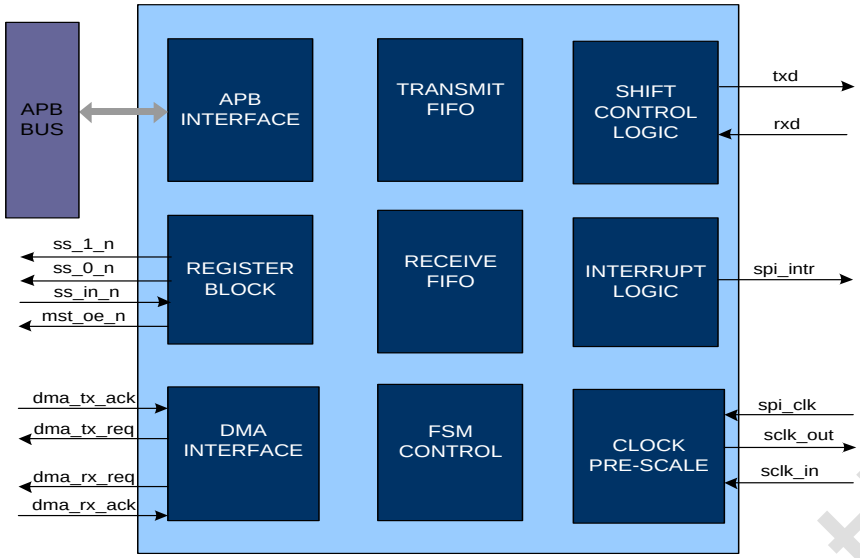


Fig. 24-1 SPI Controller Block Diagram

APB INTERFACE

The host processor accesses data, control, and status information on the SPI through the APB interface. The SPI supports APB data bus widths of 32 bits and 8 or 16 bits when reading or writing internal FIFO if data frame size(SPI_CTRL0[1:0]) is set to 8 bits.

DMA INTERFACE

This block has a handshaking interface to a DMA Controller to request and control transfers. The APB bus is used to perform the data transfer to or from the DMA Controller.

FIFO LOGIC

For transmit and receive transfers, data transmitted from the SPI to the external serial device is written into the transmit FIFO. Data received from the external serial device into the SPI is pushed into the receive FIFO. Both fifos are 32x16bits.

FSM CONTROL

Control the state's transformation of the design.

REGISTER BLOCK

All registers in the SPI are addressed at 32-bit boundaries to remain consistent with the APB bus. Where the physical size of any register is less than 32-bits wide, the upper unused bits of the 32-bit boundary are reserved. Writing to these bits has no effect; reading from these bits returns 0.

SHIFT CONTROL

Shift control logic shift the data from the transmit fifo or to the receive fifo. This logic automatically right-justifies receive data in the receive FIFO buffer.

INTERRUPT CONTROL

The SPI supports combined and individual interrupt requests, each of which can be masked. The combined interrupt request is the ORed result of all other SPI interrupts after masking.

24.3 Function Description

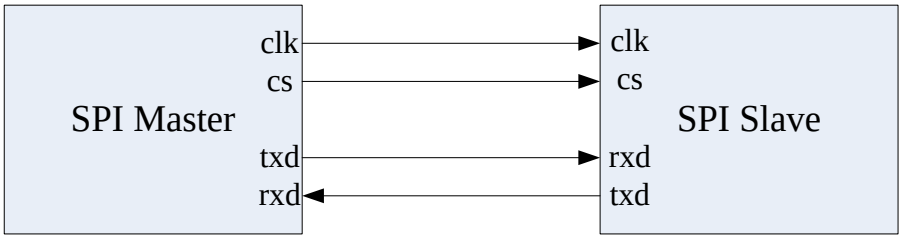


Fig. 24-2 SPI Master and Slave Interconnection

The SPI controller support dynamic switching between master and slave in a system. The diagram show how the SPI controller connects with other SPI devices.

Operation Modes

The SPI can be configured in the following two fundamental modes of operation: Master

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Mode when SPI_CTRLR0 [20] is 1'b0, Slave Mode when SPI_CTRLR0 [20] is 1'b1.

Transfer Modes

The SPI operates in the following three modes when transferring data on the serial bus.

1). Transmit and Receive

When SPI_CTRLR0 [19:18] == 2'b00, both transmit and receive logic are valid.

2). Transmit Only

When SPI_CTRLR0 [19:18] == 2'b01, the receive data are invalid and should not be stored in the receive FIFO.

3). Receive Only

When SPI_CTRLR0 [19:18] == 2'b10, the transmit data are invalid.

Clock Ratios

A summary of the frequency ratio restrictions between the bit-rate clock (sclk_out/sclk_in) and the SPI peripheral clock (spi_clk) are described as,

When SPI Controller works as master, the F_{spi_clk}>= 2 × (maximum F_{sclk_out})

When SPI Controller works as slave, the F_{spi_clk}>= 6 × (maximum F_{sclk_in})

With the SPI, the clock polarity (SCPOL) configuration parameter determines whether the inactive state of the serial clock is high or low. To transmit data, both SPI peripherals must have identical serial clock phase (SCPH) and clock polarity (SCPOL) values. The data frame can be 4/8/16 bits in length.

When the configuration parameter SCPH = 0, data transmission begins on the falling edge of the slave select signal. The first data bit is captured by the master and slave peripherals on the first edge of the serial clock; therefore, valid data must be present on the txd and rxd lines prior to the first serial clock edge. The following two figures show a timing diagram for a single SPI data transfer with SCPH = 0. The serial clock is shown for configuration parameters SCPOL = 0 and SCPOL = 1.

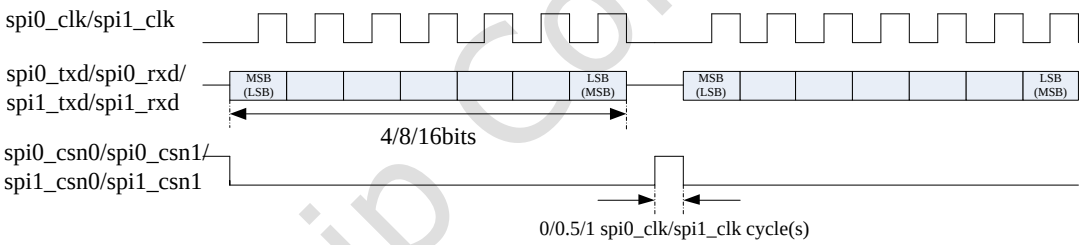


Fig. 24-3 SPI Format (SCPH=0 SCPOL=0)

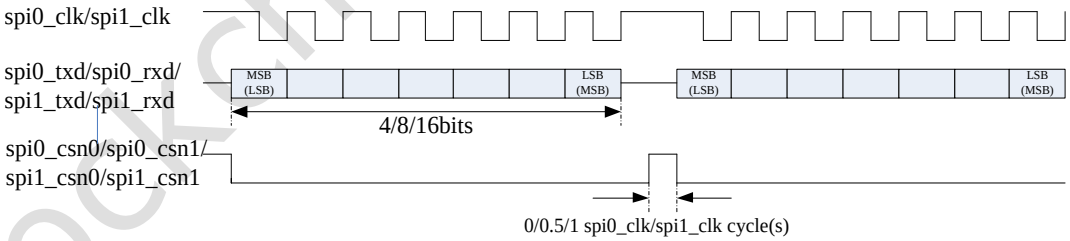


Fig. 24-4 SPI Format (SCPH=0 SCPOL=1)

When the configuration parameter SCPH = 1, both master and slave peripherals begin transmitting data on the first serial clock edge after the slave select line is activated. The first data bit is captured on the second (trailing) serial clock edge. Data are propagated by the master and slave peripherals on the leading edge of the serial clock. During continuous data frame transfers, the slave select line may be held active-low until the last bit of the last frame has been captured. The following two figures show the timing diagram for the SPI format when the configuration parameter SCPH = 1.

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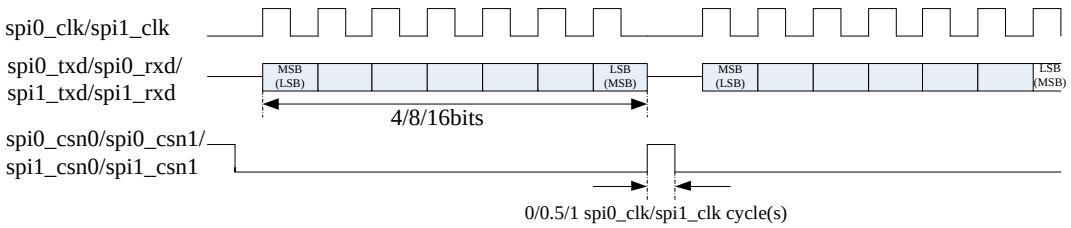


Fig. 24-5 SPI Format (SCPH=1 SCPOL=0)

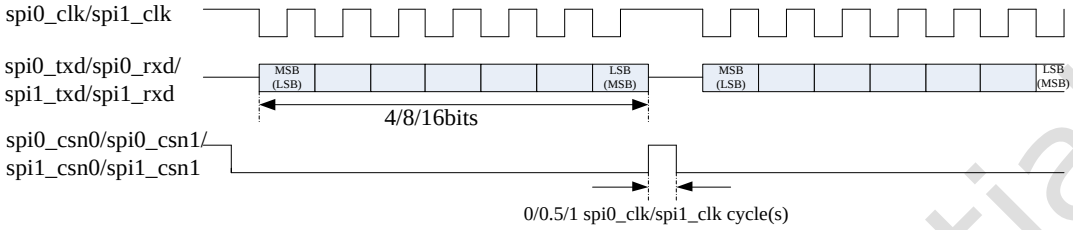


Fig. 24-6 SPI Format (SCPH=1 SCPOL=1)

24.4 Register Description

24.4.1 Registers Summary

Name	Offset	Size	Reset Value	Description
SPI_CTRLR0	0x0000	W	0x00000002	Control Register 0
SPI_CTRLR1	0x0004	W	0x00000000	Control Register 1
SPI_ENR	0x0008	W	0x00000000	SPI Enable
SPI_SER	0x000c	W	0x00000000	Slave Enable Register
SPI_BAUDR	0x0010	W	0x00000000	Baud Rate Select
SPI_TXFTLR	0x0014	W	0x00000000	Transmit FIFO Threshold Level
SPI_RXFTLR	0x0018	W	0x00000000	Receive FIFO Threshold Level
SPI_TXFLR	0x001c	W	0x00000000	Transmit FIFO Level
SPI_RXFLR	0x0020	W	0x00000000	Receive FIFO Level
SPI_SR	0x0024	W	0x0000000c	SPI Status
SPI_IPR	0x0028	W	0x00000000	Interrupt Polarity
SPI_IMR	0x002c	W	0x00000000	Interrupt Mask
SPI_ISR	0x0030	W	0x00000000	Interrupt Status
SPI_RISR	0x0034	W	0x00000001	Raw Interrupt Status
SPI_ICR	0x0038	W	0x00000000	Interrupt Clear
SPI_DMACR	0x003c	W	0x00000000	DMA Control
SPI_DMATDLR	0x0040	W	0x00000000	DMA Transmit Data Level
SPI_DMARDLR	0x0044	W	0x00000000	DMA Receive Data Level
SPI_TXDR	0x0400	W	0x00000000	Transmit FIFO Data
SPI_RXDR	0x0800	W	0x00000000	Receive FIFO Data

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

24.4.2 Detail Register Description

SPI_CTRLR0

Address: Operational Base + offset (0x0000)
Control Register 0

Bit	Attr	Reset Value	Description
31:22	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
21	RW	0x0	MTM Microwire Transfer Mode Valid when frame format is set to National Semiconductors Microwire. 1'b0: non-sequential transfer 1'b1: sequential transfer
20	RW	0x0	OPM Operation Mode 1'b0: Master Mode 1'b1: Slave Mode
19:18	RW	0x0	XFM Transfer Mode 2'b00: Transmit & Receive 2'b01: Transmit Only 2'b10: Receive Only 2'b11: reserved
17:16	RW	0x0	FRF Frame Format 2'b00: Motorola SPI 2'b01: Texas Instruments SSP 2'b10: National Semiconductors Microwire 2'b11: Reserved
15:14	RW	0x0	RSD Rxd Sample Delay When SPI is configured as a master, if the rxd data cannot be sampled by the sclk_out edge at the right time, this register should be configured to define the number of the spi_clk cycles after the active sclk_out edge to sample rxd data later when SPI works at high frequency. 2'b00: do not delay 2'b01: 1 cycle delay 2'b10: 2 cycles delay 2'b11: 3 cycles delay
13	RW	0x0	BHT Byte and Halfword Transform Valid when data frame size is 8bit. 1'b0: apb 16bit write/read, spi 8bit write/read 1'b1: apb 8bit write/read, spi 8bit write/read
12	RW	0x0	FBM First Bit Mode 1'b0: first bit is MSB 1'b1: first bit is LSB

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Bit	Attr	Reset Value	Description
11	RW	0x0	EM Endian Mode Serial endian mode can be configured by this bit. APB endian mode is always little endian. 1'b0: little endian 1'b1: big endian
10	RW	0x0	SSD ss_n to sclk_out delay Valid when the frame format is set to Motorola SPI and SPI used as a master. 1'b0: the period between ss_n active and sclk_out active is half sclk_out cycles. 1'b1: the period between ss_n active and sclk_out active is one sclk_out cycle.
9:8	RW	0x0	CSM Chip Select Mode Valid when the frame format is set to Motorola SPI and SPI used as a master. 2'b00: ss_n keep low after every frame data is transferred. 2'b01: ss_n be high for half sclk_out cycles after every frame data is transferred. 2'b10: ss_n be high for one sclk_out cycle after every frame data is transferred. 2'b11: reserved
7	RW	0x0	SCPOL Serial Clock Polarity Valid when the frame format is set to Motorola SPI. 1'b0: Inactive state of serial clock is low 1'b1: Inactive state of serial clock is high
6	RW	0x0	SCPH Serial Clock Phase Valid when the frame format is set to Motorola SPI. 1'b0: Serial clock toggles in middle of first data bit 1'b1: Serial clock toggles at start of first data bit

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Bit	Attr	Reset Value	Description
5:2	RW	0x0	CFS Control Frame Size Selects the length of the control word for the Microwire frame format. 4'b0000~0010:reserved 4'b0011: 4-bit serial data transfer 4'b0100: 5-bit serial data transfer 4'b0101: 6-bit serial data transfer 4'b0110: 7-bit serial data transfer 4'b0111: 8-bit serial data transfer 4'b1000: 9-bit serial data transfer 4'b1001: 10-bit serial data transfer 4'b1010: 11-bit serial data transfer 4'b1011: 12-bit serial data transfer 4'b1100: 13-bit serial data transfer 4'b1101: 14-bit serial data transfer 4'b1110: 15-bit serial data transfer 4'b1111: 16-bit serial data transfer
1:0	RW	0x2	DFS Data Frame Size Selects the data frame length. 2'b00: 4bit data 2'b01: 8bit data 2'b10: 16bit data 2'b11: reserved

SPI_CTRLR1
Address: Operational Base + offset (0x0004)
Control Register 1

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0000	NDM Number of Data Frames When Transfer Mode is receive only, this register field sets the number of data frames to be continuously received by the SPI. The SPI continues to receive serial data until the number of data frames received is equal to this register value plus 1, which enables you to receive up to 64 KB of data in a continuous transfer.

SPI_ENR
Address: Operational Base + offset (0x0008)
SPI Enable

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
0	RW	0x0	ENR SPI Enable 1'b1: Enable all SPI operations. 1'b0: Disable all SPI operations Transmit and receive FIFO buffers are cleared when the device is disabled.

SPI_SER
Address: Operational Base + offset (0x000c)
Slave Enable Register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x0	SER1 Slave 1 Select Enable 1'b1: Enable chip select 1 1'b0: Disable chip select 1 This register is valid only when SPI is configured as a master device.
0	RW	0x0	SER0 Slave Select Enable 1'b1: Enable chip select 0 1'b0: Disable chip select 0 This register is valid only when SPI is configured as a master device.

SPI_BAUDR
Address: Operational Base + offset (0x0010)
Baud Rate Select

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
15:0	RW	0x0000	BAUDR Baud Rate Select SPI Clock Divider. This register is valid only when the SPI is configured as a master device. The LSB for this field is always set to 0 and is unaffected by a write operation, which ensures an even value is held in this register. If the value is 0, the serial output clock (sclk_out) is disabled. The frequency of the sclk_out is derived from the following equation: Fsclk_out = Fspi_clk/ SCKDV Where SCKDV is any even value between 2 and 65534. For example: for Fspi_clk = 3.6864MHz and SCKDV =2 Fsclk_out = 3.6864/2= 1.8432MHz

SPI_TXFTLR
Address: Operational Base + offset (0x0014)
Transmit FIFO Threshold Level

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4:0	RW	0x00	TXFTLR Transmit FIFO Threshold Level When the number of transmit FIFO entries is less than or equal to this value, the transmit FIFO empty interrupt is triggered.

SPI_RXFTLR
Address: Operational Base + offset (0x0018)
Receive FIFO Threshold Level

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4:0	RW	0x00	RXFTLR Receive FIFO Threshold Level When the number of receive FIFO entries is greater than or equal to this value + 1, the receive FIFO full interrupt is triggered.

SPI_TXFLR
Address: Operational Base + offset (0x001c)
Transmit FIFO Level

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5:0	RO	0x00	TXFLR Transmit FIFO Level Contains the number of valid data entries in the transmit FIFO.

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SPI_RXFLR
Address: Operational Base + offset (0x0020)
Receive FIFO Level

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5:0	RO	0x00	RXFLR Receive FIFO Level Contains the number of valid data entries in the receive FIFO.

SPI_SR
Address: Operational Base + offset (0x0024)
SPI Status

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4	RO	0x0	RFF Receive FIFO Full 1'b0: Receive FIFO is not full 1'b1: Receive FIFO is full
3	RO	0x1	RFE Receive FIFO Empty 1'b0: Receive FIFO is not empty 1'b1: Receive FIFO is empty
2	RO	0x1	TFE Transmit FIFO Empty 1'b0: Transmit FIFO is not empty 1'b1: Transmit FIFO is empty
1	RO	0x0	TFF Transmit FIFO Full 1'b0: Transmit FIFO is not full 1'b1: Transmit FIFO is full
0	RO	0x0	BSF SPI Busy Flag When set, indicates that a serial transfer is in progress; when cleared indicates that the SPI is idle or disabled. 1'b0: SPI is idle or disabled 1'b1: SPI is actively transferring data

SPI_IPR
Address: Operational Base + offset (0x0028)
Interrupt Polarity

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
0	RW	0x0	IPR Interrupt Polarity Interrupt Polarity Register 1'b0: Active Interrupt Polarity Level is HIGH 1'b1: Active Interrupt Polarity Level is LOW

SPI_IMR
Address: Operational Base + offset (0x002c)
Interrupt Mask

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4	RW	0x0	RFFIM Receive FIFO Full Interrupt Mask 1'b0: spi_rxf_intr interrupt is masked 1'b1: spi_rxf_intr interrupt is not masked
3	RW	0x0	RFOIM Receive FIFO Overflow Interrupt Mask 1'b0: spi_rxo_intr interrupt is masked 1'b1: spi_rxo_intr interrupt is not masked
2	RW	0x0	RFUIM Receive FIFO Underflow Interrupt Mask 1'b0: spi_rxu_intr interrupt is masked 1'b1: spi_rxu_intr interrupt is not masked
1	RW	0x0	TFOIM Transmit FIFO Overflow Interrupt Mask 1'b0: spi_txo_intr interrupt is masked 1'b1: spi_txo_intr interrupt is not masked
0	RW	0x0	TFEIM Transmit FIFO Empty Interrupt Mask 1'b0: spi_txe_intr interrupt is masked 1'b1: spi_txe_intr interrupt is not masked

SPI_ISR
Address: Operational Base + offset (0x0030)
Interrupt Status

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4	RO	0x0	RFFIS Receive FIFO Full Interrupt Status 1'b0: spi_rxf_intr interrupt is not active after masking 1'b1: spi_rxf_intr interrupt is full after masking
3	RO	0x0	RFOIS Receive FIFO Overflow Interrupt Status 1'b0: spi_rxo_intr interrupt is not active after masking 1'b1: spi_rxo_intr interrupt is active after masking

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Bit	Attr	Reset Value	Description
2	RO	0x0	RFUIS Receive FIFO Underflow Interrupt Status 1'b0: spi_rxu_intr interrupt is not active after masking 1'b1: spi_rxu_intr interrupt is active after masking
1	RO	0x0	TFOIS Transmit FIFO Overflow Interrupt Status 1'b0: spi_txo_intr interrupt is not active after masking 1'b1: spi_txo_intr interrupt is active after masking
0	RO	0x0	TFEIS Transmit FIFO Empty Interrupt Status 1'b0: spi_txe_intr interrupt is not active after masking 1'b1: spi_txe_intr interrupt is active after masking

SPI_RISR
Address: Operational Base + offset (0x0034)
Raw Interrupt Status

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4	RO	0x0	RFFRIS Receive FIFO Full Raw Interrupt Status 1'b0: spi_rxf_intr interrupt is not active prior to masking 1'b1: spi_rxf_intr interrupt is full prior to masking
3	RO	0x0	RFORIS Receive FIFO Overflow Raw Interrupt Status 1'b0: spi_rxo_intr interrupt is not active prior to masking 1'b1: spi_rxo_intr interrupt is active prior to masking
2	RO	0x0	RFURIS Receive FIFO Underflow Raw Interrupt Status 1'b0: spi_rxu_intr interrupt is not active prior to masking 1'b1: spi_rxu_intr interrupt is active prior to masking
1	RO	0x0	TFORIS Transmit FIFO Overflow Raw Interrupt Status 1'b0: spi_txo_intr interrupt is not active prior to masking 1'b1: spi_txo_intr interrupt is active prior to masking
0	RO	0x1	TFERIS Transmit FIFO Empty Raw Interrupt Status 1'b0: spi_txe_intr interrupt is not active prior to masking 1'b1: spi_txe_intr interrupt is active prior to masking

SPI_ICR
Address: Operational Base + offset (0x0038)
Interrupt Clear

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Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3	WO	0x0	CTFOI Clear Transmit FIFO Overflow Interrupt Write 1 to Clear Transmit FIFO Overflow Interrupt
2	WO	0x0	CRFOI Clear Receive FIFO Overflow Interrupt Write 1 to Clear Receive FIFO Overflow Interrupt
1	WO	0x0	CRFUI Clear Receive FIFO Underflow Interrupt Write 1 to Clear Receive FIFO Underflow Interrupt
0	WO	0x0	CCI Clear Combined Interrupt Write 1 to Clear Combined Interrupt

SPI_DMACR
Address: Operational Base + offset (0x003c)
DMA Control

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x0	TDE Transmit DMA Enable 1'b0: Transmit DMA disabled 1'b1: Transmit DMA enabled
0	RW	0x0	RDE Receive DMA Enable 1'b0: Receive DMA disabled 1'b1: Receive DMA enabled

SPI_DMATDLR
Address: Operational Base + offset (0x0040)
DMA Transmit Data Level

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4:0	RW	0x00	TDL Transmit Data Level This bit field controls the level at which a DMA request is made by the transmit logic. It is equal to the watermark level; that is, the dma_tx_req signal is generated when the number of valid data entries in the transmit FIFO is equal to or below this field value, and Transmit DMA Enable (DMACR[1]) = 1.

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SPI_DMARDLR
Address: Operational Base + offset (0x0044)
DMA Receive Data Level

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4:0	RW	0x00	RDL Receive Data Level This bit field controls the level at which a DMA request is made by the receive logic. The watermark level = DMARDL+1; that is, dma_rx_req is generated when the number of valid data entries in the receive FIFO is equal to or above this field value + 1, and Receive DMA Enable(DMACR[0])=1.

SPI_TXDR
Address: Operational Base + offset (0x0048)
Transmit FIFO Data

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	WO	0x0000	TXDR Transmit FIFO Data Register. When it is written to, data are moved into the transmit FIFO.

SPI_RXDR
Address: Operational Base + offset (0x004c)
Receive FIFO Data

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0000	RXDR Receive FIFO Data Register. When the register is read, data in the receive FIFO is accessed.

24.5 Interface Description

SPI have 3 IOMUX, which is controlled by GRF_SOC_CON1[4:3].
When GRF_SOC_CON1[4:3] is 2'b00. The IOMUX is as follow.

Table 24-1 SPI interface description

Module Pin	Direction	Pad Name	IOMUX Setting
spi_clk	I/O	IO_SPIclk_UART1ctsn_GPIO1b0	GRF_GPIO1B_IOMUX[1:0]=2'b01
spi_csn0	I/O	IO_SPIcsn0_UART1rtsn_GPIO1b3	GRF_GPIO1B_IOMUX[7:6]=2'b01
spi_txd	O	IO_SPItxd_UART1sout_GPIO1b1	GRF_GPIO1B_IOMUX[3:2]=2'b01
spi_rxd	I	IO_SPIrxd_UART1sin_GPIO1b2	GRF_GPIO1B_IOMUX[5:4]=2'b01
spi_csn1	O	IO_SPIcsn1_GPIO1b4	GRF_GPIO1B_IOMUX[8]=1'b1

Notes: I=input, O=output, I/O=input/output, bidirectional. spi_csn1 can only be used in master mode

When GRF_SOC_CON1[4:3] is 2'b01. The IOMUX is as follow.

Table 24-2 SPI interface description

Module Pin	Direction	Pad Name	IOMUX Setting

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spi_clk	I/O	IO_NANDale_SPI1clk_GPIO2a0	GRF_GPIO2A_IOMUX[1:0]=2'b10
spi_csn0	I/O	IO_NANDd6_EMMCd6_SPI1csn0_GPIO1d6	GRF_GPIO1D_IOMUX[13:12]=2'b11
spi_txd	O	IO_NANDd5_EMMCd5_SPI1txd1_GPIO1d5	GRF_GPIO1D_IOMUX[11:10]=2'b11
spi_rxd	I	IO_NANDd4_EMMCd4_SPI1rxd1_GPIO1d4	GRF_GPIO1D_IOMUX[9:8]=2'b11
spi_csn1	O	IO_NANDd7_EMMCd7_SPI1csn1_GPIO1d7	GRF_GPIO1D_IOMUX[15:14]=2'b11

Notes: I=input, O=output, I/O=input/output, bidirectional. spi_csn1 can only be used in master mode

When GRF_SOC_CON1[4:3] is 2'b10. The IOMUX is as follow.

Table 24-3 SPI interface description

Module Pin	Direction	Pad Name	IOMUX Setting
spi_clk	I/O	IO_I2S1sclk_SPIclkm_GPIO0b1	GRF_GPIO0B_IOMUX[3:2]=2'b10
spi_csn0	I/O	IO_I2S1sdi_SPIcsn0m_GPIO0b6	GRF_GPIO0B_IOMUX[13:12]=2'b10
spi_txd	O	IO_I2S1lrckrx_SPItxdm_GPIO0b3	GRF_GPIO0B_IOMUX[7:6]=2'b10
spi_rxd	I	IO_I2S1sdo_SPIrxdm_GPIO0b5	GRF_GPIO0B_IOMUX[11:10]=2'b10

Notes: I=input, O=output, I/O=input/output, bidirectional. spi_csn1 can only be used in master mode

24.6 Application Notes

Clock Ratios

A summary of the frequency ratio restrictions between the bit-rate clock (sclk_out/sclk_in) and the SPI peripheral clock (spi_clk) are described as,

When SPI Controller works as master, the Fspi_clk>= 2 × (maximum Fsclk_out)

When SPI Controller works as slave, the Fspi_clk>= 6 × (maximum Fsclk_in)

Master Transfer Flow

When configured as a serial-master device, the SPI initiates and controls all serial transfers. The serial bit-rate clock, generated and controlled by the SPI, is driven out on the sclk_out line. When the SPI is disabled (SPI_ENR = 0), no serial transfers can occur and sclk_out is held in "inactive" state, as defined by the serial protocol under which it operates.

Slave Transfer Flow

When the SPI is configured as a slave device, all serial transfers are initiated and controlled by the serial bus master.

When the SPI serial slave is selected during configuration, it enables its txd data onto the serial bus. All data transfers to and from the serial slave are regulated on the serial clock line (sclk_in), driven from the serial-master device. Data are propagated from the serial slave on one edge of the serial clock line and sampled on the opposite edge.

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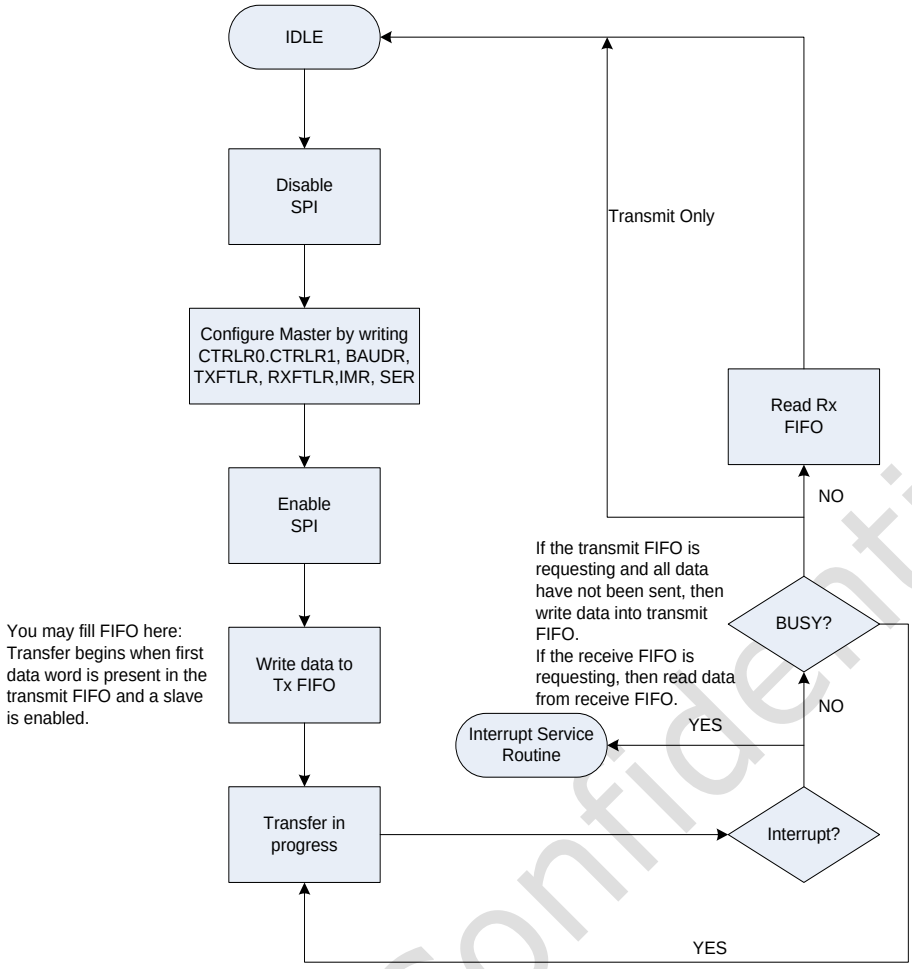


Fig. 24-7 SPI Master transfer flow diagram

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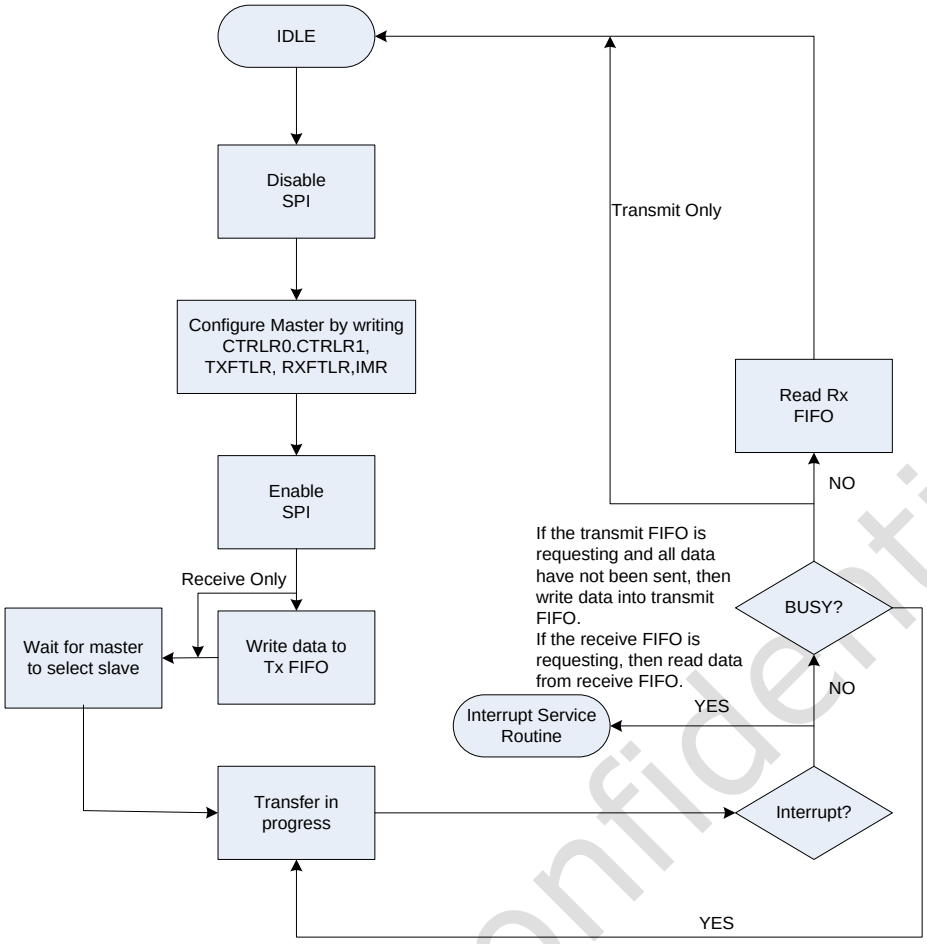


Fig. 24-8 SPI Slave transfer flow diagram

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Chapter 25 Transport Stream Processing Module (TSP)

25.1 Overview

The Transport Stream Processing Module(TSP) is designed for processing Transport Stream Packets, including receiving TS packets, PID filtering, TS descrambling, De-multiplexing and TS outputting. Processed data are transferred to memory buffer which are continued to be processing by software.

TSP supports the following features:

- Supports 1 TS input channels
- Supports 4 TS Input Mode: sync/valid mode in the case of serial TS input; nosync/valid mode, sync/valid, sync/burst mode in the case of parallel TS input
- Supports 2 TS sources: demodulators and local memory
- Supports 1 Built-in PTIs(Programmable Transport Interface) to process TS simultaneously
- Supports 1 PVR(Personal Video Recording) output channel
- 1 built-in multi-channel DMA Controller
- Support DMA LLP transfer
- Each PTI supports
  - 64 PID filters
  - TS descrambling with 16 sets of Control Word under CSA v2.0 standard, up to 104Mbps
  - 16 PES/ES filters with PTS/DTS extraction and ES start code detection
  - 4/8 PCR extraction channels
  - 64 Section filters with CRC check, and three interrupt mode: stop per unit, full-stop, recycle mode with version number check
  - PID done and error interrupts for each channel
  - PCR/DTS/PTS extraction interrupt for each channel
- Support 32 bit AXI MMU.

25.2 Block Diagram

The TSP wrapper comprises of following components:

- TSP module (include: AHB slave, register block ,PTI ,DMAC, AHB master)
- AHB/AXI bridge
- 32bit AXI MMU

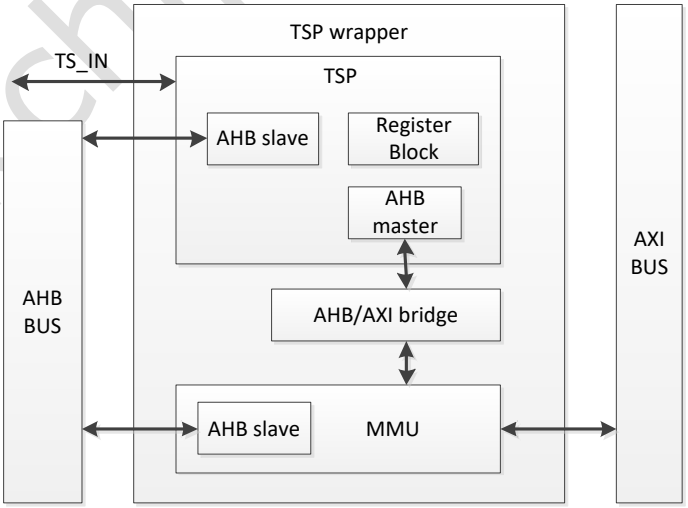


Fig. 25-1 TSP architecture

AHB Slave INTERFACE

The host processor can get access to the TSP and MMU register block through AHB slave interface. The slave interface supports 32bit access.

Register block

All registers in the TSP are addressed at 32-bit boundaries to remain consistent with the AHB bus. Where the physical size of any register is less than 32-bits wide, the upper

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unused bits of the 32-bit boundary are reserved. Writing to these bits has no effect; reading from these bits returns 0.

PTI

Most of the TS processing are dealt with PTI. TS packets are re-synchronized, filtered, descrambled and demultiplexing, and the processed packets are transferred to memory buffer to be processed further by software. The embedded TS in interface can receive TS packets by connecting to a compliant TS demodulator. TS stream stored in the local memory is another source to fed into PTI through by using LLP DMA mode.

DMAC

The DMAC performs all DMA transfers which get access to memory.

AHB/AXI bridge

Convert AHB master to AXI master.

MMU

Support AXI interface,4K page size and TLB pre-fetch. Data bus width is 32 bit.

25.3 Function Description

25.3.1 TS Stream of TS_IN Interface

TS_IN interface supports 4 input TS stream mode: sync/valid serial mode, sync/valid parallel mode, sync/burst parallel mode, nosync/valid parallel mode.

A.Sync/Valid Serial Mode

In this mode, TS_IN interface takes use of TSI_SYNC and TSI_VALID clocked with TSI_CLK signal to sample input serial TS packet data.

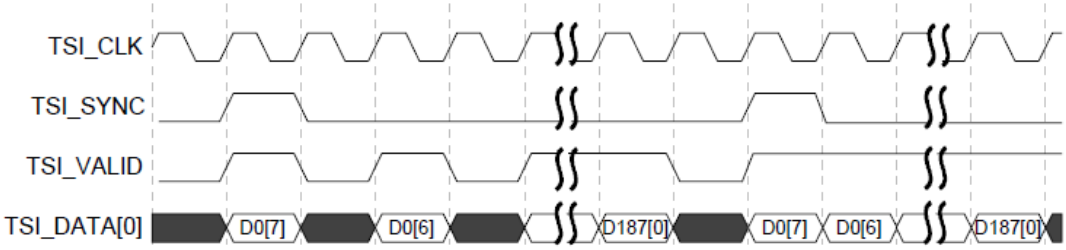


Fig. 25-2 Sync/Valid Serial Mode with Msb-Lsb Bit Ordering

TSI_SYNC must be active high together with TSI_VALID when indicating the first valid bit of a TS packet, and TSI_VALID indicates the 188*8 valid bits of a TS packet. TSI supports both msb-lsb and lsb-msb bit ordering.

B. Sync/Valid Parallel Mode

In this mode, TS_IN interface takes use of TSI_SYNC and TSI_VALID clocked with TSI_CLK signal to sample input parallel TS packet data.

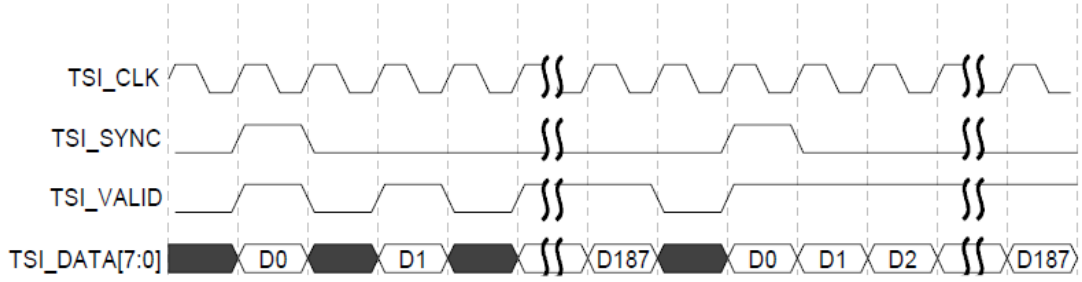


Fig. 25-3 Sync/valid Parallel Mode

TSI_SYNC must be active high together with TSI_VALID when indicating the first valid byte of a TS packet, and TSI_VALID indicates the 188 valid byte of a TS packet.

C. Sync/Burst Parallel Mode

In this mode, TSI only takes use of TSI_SYNC to sample input parallel TS packet data.

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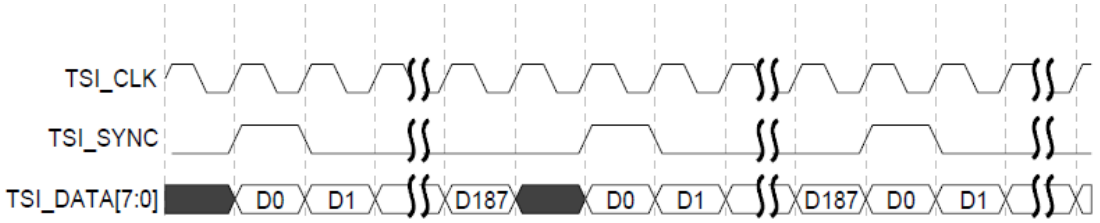


Fig. 25-4 Sync/Burst Parallel Mode

When active high, TSI_SYNC implies the first valid byte of a TS packet and remaining 187 valid bytes of a TS packet are upcoming within the following successive 187 clock cycles.

D. Nosync/Valid Parallel Mode

In this mode, TSI only takes uses of TSI_VALID to sample input parallel TS packet data.

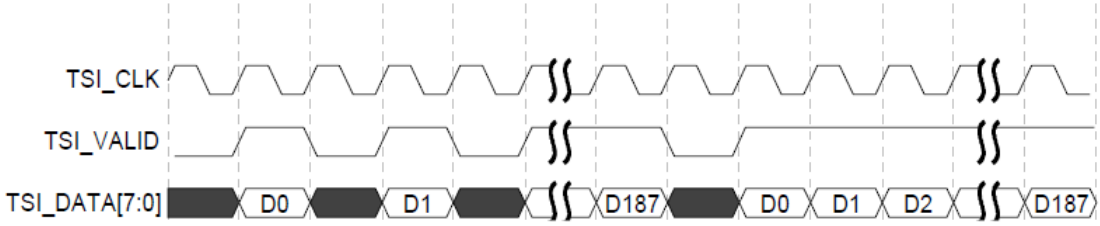


Fig. 25-5 Nosync/Valid Parallel Mode

When active high, TSI_VALID implies a valid byte of a TS packet.

25.3.2 TS output of TS Out Interface

TS out interface transmit the TS data in two mode: serial mode and parallel mode. In the serial mode, the bit order can be lsb-msb or msb-lsb.

The TS_SYNC will be active high when indicating the header of the TS packets, and it only lasts for one cycle. TS_VALID will be active high when the output TS data is valid. The output data is 188 byte TS packet data.

TS out interface also stamp the TS output stream with new PCR value, making PCR adjustment. PCR is used to measure the transport rate.

$$PCR(i) = PCR_base(i) \times 300 + PCR_ext(i)$$

where:

$$PCR_base(i) = ((system_clock_frequency \times t(i))\ DIV\ 300)\ \%\ 2^{33}$$

$$PCR_ext(i) = ((system_clock_frequency \times t(i))\ DIV\ 1)\ \%\ 300$$

$$transport_rate(i) = \frac{((i' - i'') \times system_clock_frequency)}{PCR(i') - PCR(i'')}$$

Where

i' is the index of the byte containing the last bit of the immediately following program_clock_reference_base field applicable to the program being decoded.

i is the is the index of any byte in the Transport Stream for i''< i < i'.

i''is the index of the byte containing the last bit of the most recent program_clock_reference_base fieldapplicable to the program being decoded.

System clock is 27Mhz.

25.3.3 Demux and descrambling

Each PTI has 64 PID channels to deal with demultiplexing and descrambling operation.

The PTI can descramble the TS Packets which are scrambled with CSA v2.0 standard. The TS packets can be scrambled either in TS level or PES level.

The demux module can do the section filtering, pes filtering and es filtering, or directly output TS packets.

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25.4 Register Description

25.4.1 TSP Register Summary

Name	Offset	Size	Reset Value	Description
TSP_GCFG	0x0000	W	0x00000000	Global Configuration Register
TSP_PVR_CTRL	0x0004	W	0x00000000	PVR Control Register
TSP_PVR_LEN	0x0008	W	0x00000000	PVR DMA Transaction Length
TSP_PVR_BASE_ADDR	0x000c	W	0x00000000	PVR DMA transaction starting address
TSP_PVR_INT_STS	0x0010	W	0x00000000	PVR DMA Interrupt Status Register
TSP_PVR_INT_ENA	0x0014	W	0x00000000	DMA Interrupt Enable Register
TSP_TSOUT_CTRL	0x0018	W	0x00000000	TS Out Control Register
TSP_PVR_TOP_ADDR	0x001c	W	0x00000000	PVR buffer top address
TSP_PVR_WRITE_ADDR	0x0020	W	0x00000000	PVR buffer write point
TSP_PTIx_CTRL	0x0100	W	0x00000000	PTI Channel Control Register
TSP_PTIx_LLP_CFG	0x0104	W	0x00000000	LLP DMA Control Register
TSP_PTIx_LLP_BASE	0x0108	W	0x00000000	LLP Descriptor BASE Address
TSP_PTIx_LLP_WRITE	0x010c	W	0x00000000	LLP DMA Writing Software Descriptor Counter
TSP_PTIx_LLP_READ	0x0110	W	0x00000000	LLP DMA Reading Hardware Descriptor Counter
TSP_PTIx_PID_STS0	0x0114	W	0x00000000	PTI PID Channel Status 0 Register
TSP_PTIx_PID_STS1	0x0118	W	0x00000000	PTI PID Channel Status 1 Register
TSP_PTIx_PID_STS2	0x011c	W	0x00000000	PTI PID Channel Status 2 Register
TSP_PTIx_PID_STS3	0x0120	W	0x00000000	PTI PID Channel Status 3 Register
TSP_PTIx_PID_INT_ENA0	0x0124	W	0x00000000	PID Interrupt Enable Register 0
TSP_PTIx_PID_INT_ENA1	0x0128	W	0x00000000	PID Interrupt Enable Register 1
TSP_PTIx_PID_INT_ENA2	0x012c	W	0x00000000	PID Interrupt Enable Register 2
TSP_PTIx_PID_INT_ENA3	0x0130	W	0x00000000	PID Interrupt Enable Register 3
TSP_PTIx_PCR_INT_STS	0x0134	W	0x00000000	PTI PCR Interrupt Status Register
TSP_PTIx_PCR_INT_ENA	0x0138	W	0x00000000	PTI PCR Interrupt Enable Register
TSP_PTIx_PCRn_CTRL	0x013c	W	0x00000000	PID PCR Control Register
TSP_PTIx_PCRn_H	0x015c	W	0x00000000	High Order PCR value
TSP_PTIx_PCRn_L	0x0160	W	0x00000000	Low Order PCR value
TSP_PTIx_DMA_STS	0x019c	W	0x00000000	LLP DMA Interrupt Status Register
TSP_PTIx_DMA_ENA	0x01a0	W	0x00000000	DMA Interrupt Enable Register
TSP_PTIx_DATA_FLAG0	0x01a4	W	0x00000000	PTI_PID_WRITE Flag 0
TSP_PTIx_DATA_FLAG1	0x01a8	W	0x00000000	PTI_PID_WRITE Flag 1
TSP_PTIx_LIST_FLAG	0x01ac	W	0x00000000	PTIx_LIST_WRITE Flag
TSP_PTIx_DST_STS0	0x01b0	W	0x00000000	PTI Destination Status Register
TSP_PTIx_DST_STS1	0x01b4	W	0x00000000	PTI Destination Status Register
TSP_PTIx_DST_ENA0	0x01b8	W	0x00000000	PTI Destination Interrupt Enable Register

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Name	Offset	Size	Reset Value	Description
TSP_PTIx_DST_ENA1	0x01bc	W	0x00000000	PTI Destination Interrupt Enable Register
TSP_PTIx_ECWn_H	0x0200	W	0x00000000	The Even Control Word High Order
TSP_PTIx_ECWn_L	0x0204	W	0x00000000	The Even Control Word Low Order
TSP_PTIx_OCWn_H	0x0208	W	0x00000000	The Odd Control Word High Order
TSP_PTIx_OCWn_L	0x020c	W	0x00000000	The Odd Control Word Low Order
TSP_PTIx_PIDn_CTRL	0x0300	W	0x00000000	PID Channel Control Register
TSP_PTIx_PIDn_BASE	0x0400	W	0x00000000	PTI Data Memory Buffer Base Address
TSP_PTIx_PIDn_TOP	0x0404	W	0x00000000	PTI Data Memory Buffer Top Address
TSP_PTIx_PIDn_WRITE	0x0408	W	0x00000000	PTI Data Memory Buffer Hardware Writing Address
TSP_PTIx_PIDn_READ	0x040c	W	0x00000000	PTI Data Memory Buffer Software Reading Address
TSP_PTIx_LISTn_BASE	0x0800	W	0x00000000	PTI List Memory Buffer Base Address
TSP_PTIx_LISTn_TOP	0x0804	W	0x00000000	PTI List Memory Buffer Top Address
TSP_PTIx_LISTn_WRITE	0x0808	W	0x00000000	PTI List Memory Buffer Hardware Writing Address
TSP_PTIx_LISTn_READ	0x080c	W	0x00000000	PTI List Memory Buffer Software Reading Address
TSP_PTIx_PIDn_CFG	0x0900	W	0x00000008	PID Demux Configure Register
TSP_PTIx_PIDn_FILT_0	0x0904	W	0x00000000	Fliter Word 0
TSP_PTIx_PIDn_FILT_1	0x0908	W	0x00000000	Fliter Word 1
TSP_PTIx_PIDn_FILT_2	0x090c	W	0x00000000	Fliter Word 2
TSP_PTIx_PIDn_FILT_3	0x0910	W	0x00000000	Fliter Word 3

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

25.4.2 TSP Detail Register Description

TSP_GCFG

Address: Operational Base + offset (0x0000)

Global Configuration Register

Bit	Attr	Reset Value	Description
31:7	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
6:4	RW	0x0	arbit_cnt DMA channel arbiter counter This field is used to adjust the priority of DMA channels to prevent one channel holds the highest priority for a long time. The 3-bit field sets the largest times for a DMA channel to hold the highest priority to send the bus request. After requested times reach this limit, the highest priority is passed to next DMA channel in order.
3	RW	0x0	tsout_on TS Output Module Switch 1: TS output module switched on 0: TS output module switched off
2	RW	0x0	pvr_on PVR Module Switch 1: PVR function turned on ; 0: PVR function turned off ;
1	RW	0x0	pti1_on PTI0 channel switch 1: PTI1 channel switched on 0: PTI1 channel switched off
0	RW	0x0	pti0_on PTI0 channel switch 1: PTI0 channel switched on 0: PTI1 channel switched off

TSP_PVR_CTRL
Address: Operational Base + offset (0x0004)
PVR Control Register

Bit	Attr	Reset Value	Description
31:7	RO	0x0	reserved
6	RW	0x0	fixaddr_en Fix Address Mode Select 1: fixed address mode; 0: incrementing address mode;
5:4	RW	0x0	burst_mode PVR burst mode PVR DMA burst mode 2'b00: INCR4 2'b01: INCR8 2'b10: INCR16 2'b11: Reserverd

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Bit	Attr	Reset Value	Description
3:2	RW	0x0	source PVR Source Select TS source for PVR output. 00: non-PID-filtered TS packets in PTI0; 01: PID filtered TS packets in PTI0; 10: non-PID-filtered TS packets in PTI1; 11: PID-filtered TS packets in PTI1;
1	R/WSC	0x0	stop PVR stop Write 1 to stop DMA channel. DMA will complete current burst transfer and then stop. It may takes several cycles. 1: PVR Stop ; 0: no effect ;
0	R/WSC	0x0	start PVR start Write 1 to start PVR. This bit will be cleared if PVR is stopped or PVR transaction is completed. 1: start PVR 0: no effect.

TSP_PVR_LEN
Address: Operational Base + offset (0x0008)
PVR DMA Transaction Length

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	len Transaction Length Transaction Length

TSP_PVR_BASE_ADDR
Address: Operational Base + offset (0x000c)
PVR DMA transaction starting address

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	addr PVR DMA transaction starting address PVR DMA transaction starting address

TSP_PVR_INT_STS
Address: Operational Base + offset (0x0010)
PVR DMA Interrupt Status Register

Bit	Attr	Reset Value	Description
31:3	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
2	W1C	0x0	pvr_update_flag pvr address pageover flag When write_addr >= (base + top_addr/2), or write addr >= top_addr, the pvr_update_flag will assert HIGH. The application can write 1 to this bit to clear it.
1	W1C	0x0	pvr_error PVR DMA transaction error 1: error response during PVR DMA transaction; 0: no error response during PVR DMA transaction;
0	W1C	0x0	pvr_done PVR DMA transaction done 1: PVR DMA transaction completed; 0: PVR DMA transaction not completed;

TSP_PVR_INT_ENA
Address: Operational Base + offset (0x0014)
DMA Interrupt Enable Register

Bit	Attr	Reset Value	Description
31:3	RO	0x0	reserved
2	RW	0x0	pvr_update_ena 1: pvr_update interrupt enable 0: pvr_update interrupt disable
1	RW	0x0	pvr_error_ena PVR DMA Transcation Error Interrupt Enable 1: Error Interrupt Enabled 0: Error Interrupt Disabled
0	RW	0x0	pvr_done_ena PVR DMA Transaction Done Interrupt Enable 1: Done Interrupt Enabled 0: Done Interrupt Disabled

TSP_TSOUT_CTRL
Address: Operational Base + offset (0x0018)
TS Out Control Register

Bit	Attr	Reset Value	Description
31:7	RO	0x0	reserved
6	RW	0x0	tso_sdo_sel TS serial data output 1: bit[0] use as serial data output ; 0: bit[7] use as serial data output ;
5	RW	0x0	tso_clk_phase TS output clock phase 0: ts output clock; 1: inverse of ts output clock.

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Bit	Attr	Reset Value	Description
4	RW	0x0	mode TS Output mode Selection Output mode select: 0: Serial Mode 1: Parallel Mode
3	RW	0x0	bit_order ts output serial data byte order Indicates that the output serial data byte order, ignored in the parallel: 0: MSB to LSB 1: LSB to MSB
2:1	RW	0x0	source TS Output Source Select TS source for TS out. 00: non-PID-filtered TS packets in PTI0; 01: PID filtered TS packets in PTI0; 10: non-PID-filtered TS packets in PTI1; 11: PID-filtered TS packets in PTI1;
0	RW	0x0	start TS out start 1: to start TS out function ; 0: to stop TS out function;

TSP_PVR_TOP_ADDR
Address: Operational Base + offset (0x001c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pvr_top_addr top address in pvr mode

TSP_PVR_WRITE_ADDR
Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pvr_write_addr The core will update this register to show the PVR write addr

TSP_PTIx_CTRL
Address: Operational Base + offset (0x0100)
PTI Channel Control Register

Bit	Attr	Reset Value	Description
31:22	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
21	RW	0x0	tsi_sdi_sel TS Serial Data Input Select 1: bit[0] use as serial input data 0: bit[7] use as serial input data
20:19	RW	0x0	tsi_error_handle TS ERROR Handle 00: don't output 01: set the error indicator to 1 10: don't care
18	RW	0x0	clk_phase_sel ts input clock phase select 1'b0: ts input clock 1'b1: inverse of ts input clock
17:16	RW	0x0	demux_burst_mode Demux DMA Burst Mode Demux DMA Mode 2'b00: INCR4 2'b01: INCR8 2'b10: INCR16 2'b11: Reserved
15	RW	0x0	sync_bypass Bypass mode Selection 1'b1: Bypass mode, indicating that input TS packets will not be resynchronized and directly fed into the following modules; 1'b0: Synchronous mode, default, indicating that input TS packets will be resynchronized;
14	RW	0x0	cw_byteorder Control Word format Configuration 0: Default: first byte of the word is the highest byte 1: first byte of the word is the lowest byte
13	RW	0x0	cm_on CSA Conformance Mechanism Configuration CSA Conformance Mechanism 0: CM turned off 1: CM turned on
12:11	RW	0x0	tsi_mode TSI Input Mode Selection Input mode selection: 00: Serial Sync/valid Mode 01: Parallel Sync/valid Mode 10: Parallel Sync/burst Mode 11: Parallel Nosync/valid Mode

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Bit	Attr	Reset Value	Description
10	RW	0x0	tsi_bit_order input serial data order Indicates that the input serial data byte order, ignored in the parallel mode: 0: MSB to LSB 1: LSB to MSB
9	RW	0x0	tsi_sel TS Input Source Select Select input TS source 1'b1: HSADC ; 1'b0: internel memory ;
8	RW	0x0	out_byteswap Output byteswap function When enabled, the word to be transferred to memory buffer "B4B3B2B1" is performed byteswapping to "B1B2B3B4".
7	RW	0x0	in_byteswap Input TS Word Byteswap When enabled, the input TS word "B4B3B2B1" is perfomed byteswapping to "B1B2B3B4".
6:4	RW	0x0	unsync_times TS Header Unsynchronized Times If synchronous mode is selected. This field sets the successive times of TS packet header error to re-lock TS header when TS is in locked status;
3:1	RW	0x0	sync_times TS Header Synchronized Times If synchronous mode is selected. This field sets the successive times of finding TS packet header to lock the TS header when TS is in unlocked status;
0	R/WSC	0x0	clear Software clear signal It will reset the core register . It will table several cycles. After reset done, soft_reset will be low. 1. reset; 0. no effect.

TSP_PTIx_LLP_CFG

Address: Operational Base + offset (0x0104)

LLP DMA Control Register

Bit	Attr	Reset Value	Description
31:10	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
9:8	RW	0x0	threshold LLP Transfer Threshold The depth for LLP descriptors is 64. An interrupt will be asserted when transfer reaches the threshold set if DMA transfer interrupt is enabled. 00: 1/1 depth 01: 1/2 depth 10: 1/4 depth 11: 1/8 depth
7:6	RW	0x0	burst_mode LLP DMA Burst Mode LLP DMA Burst Mode 2'b00: INCR4 2'b01: INCR8 2'b10: INCR16 2'b11: Reserverd
5	RW	0x0	hw_trigger Hardware Trigger Select 1. hardware trigger; 0. software trigger;
4	RW	0x0	fix_addr_en Fix Address Mode Select 1: fixed address mode; 0: incrementing address mode;
3	W1C	0x0	cfg_done LLP DMA Configuration Done When all descriptors of LLP are configured, write 1 to to this bit. The core will clear this bit when llp transction is finished ;
2	RW	0x0	pause LLP DMA Pause Write 1 to Pause DMA channel . DMA will complete current burst transfer and then pause. All register stay unchange. If software write 0 later , It will continue to work. It may take several cycles to pause. 1: pause; 0: continue to work ;
1	W1C	0x0	stop LLP DMA Stop Write 1 to stop DMA channel. DMA will complete current burst transter and then stop. It may takes several cycles. 1: stop ; 0: no effect ;

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Bit	Attr	Reset Value	Description
0	W1C	0x0	start LLP DMA start Write 1 to start DMA Channel , self clear after 1 cycle. 1: start ; 0: no effect

TSP_PTIx_LLP_BASE
Address: Operational Base + offset (0x0108)
LLP Descriptor BASE Address

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	addr LLP Descriptor BASE Address LLP Descriptor BASE address

TSP_PTIx_LLP_WRITE
Address: Operational Base + offset (0x010c)
LLP DMA Writing Software Descriptor Counter

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x00	counter LLP DMA Writing Software Descriptor Counter LLP DMA Writing Software Descriptor Counter

TSP_PTIx_LLP_READ
Address: Operational Base + offset (0x0110)
LLP DMA Reading Hardware Descriptor Counter

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RO	0x00	counter LLP DMA Reading Hardware Descriptor Counter LLP DMA Reading Hardware Descriptor Counter

TSP_PTIx_PID_STS0
Address: Operational Base + offset (0x0114)
PTI PID Channel Status 0 Register

Bit	Attr	Reset Value	Description
31	RW	0x0	pid31_done PID31 Channel Status 1 means done
30	W1C	0x0	pid30_done PID30 Channel Status 1 means done
29	W1C	0x0	pid29_done PID29 Channel Status 1 means done

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Bit	Attr	Reset Value	Description
28	W1C	0x0	pid28_done PID28 Channel Status 1 means done
27	W1C	0x0	pid27_done PID27 Channel Status 1 means done
26	W1C	0x0	pid26_done PID26 Channel Status 1 means done
25	W1C	0x0	pid25_done PID25 Channel Status 1 means done
24	W1C	0x0	pid24_done PID24 Channel Status 1 means done
23	W1C	0x0	pid23_done PID23 Channel Status 1 means done
22	W1C	0x0	pid22_done PID22 Channel Status 1 means done
21	W1C	0x0	pid21_done PID21 Channel Status 1 means done
20	W1C	0x0	pid20_done PID20 Channel Status 1 means done
19	W1C	0x0	pid19_done PID19 Channel Status 1 means done
18	W1C	0x0	pid18_done PID18 Channel Status 1 means done
17	W1C	0x0	pid17_done PID17 Channel Status 1 means done
16	W1C	0x0	pid16_done PID16 Channel Status 1 means done
15	W1C	0x0	pid15_done PID15 Channel Status 1 means done
14	W1C	0x0	pid14_done PID14 Channel Status 1 means done

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Bit	Attr	Reset Value	Description
13	W1C	0x0	pid13_done PID13 Channel Status 1 means done
12	W1C	0x0	pid12_done PID12 Channel Status 1 means done
11	W1C	0x0	pid11_done PID11 Channel Status 1 means done
10	W1C	0x0	pid10_done PID10 Channel Status 1 means done
9	W1C	0x0	pid9_done PID9 Channel Status 1 means done
8	W1C	0x0	pid8_done PID8 Channel Status 1 means done
7	W1C	0x0	pid7_done PID7 Channel Status 1 means done
6	W1C	0x0	pid6_done PID6 Channel Status 1 means done
5	W1C	0x0	pid5_done PID5 Channel Status 1 means done
4	W1C	0x0	pid4_done PID4 Channel Status 1 means done
3	W1C	0x0	pid3_done PID3 Channel Status 1 means done
2	RW	0x0	pid2_done PID2 Channel Status 1 means done
1	W1C	0x0	pid1_done PID1 Channel Status 1 means done
0	W1C	0x0	pid0_done PID0 Channel Status 1 means done

TSP_PTIx_PID_STS1
Address: Operational Base + offset (0x0118)

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PTI PID Channel Status 1 Register

Bit	Attr	Reset Value	Description
31	W1C	0x0	pid63_done PID63 Channel Status 1 means done
30	W1C	0x0	pid62_done PID62 Channel Status 1 means done
29	W1C	0x0	pid61_done PID61 Channel Status 1 means done
28	W1C	0x0	pid60_done PID60 Channel Status 1 means done
27	W1C	0x0	pid59_done PID59 Channel Status 1 means done
26	W1C	0x0	pid58_done PID58 Channel Status 1 means done
25	W1C	0x0	pid57_done PID57 Channel Status 1 means done
24	W1C	0x0	pid56_done PID56 Channel Status 1 means done
23	W1C	0x0	pid55_done PID55 Channel Status 1 means done
22	W1C	0x0	pid54_done PID54 Channel Status 1 means done
21	W1C	0x0	pid53_done PID53 Channel Status 1 means done
20	W1C	0x0	pid52_done PID52 Channel Status 1 means done
19	W1C	0x0	pid51_done PID51 Channel Status 1 means done
18	W1C	0x0	pid50_done PID51 Channel Status 1 means done

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Bit	Attr	Reset Value	Description
17	W1C	0x0	pid49_done PID49 Channel Status 1 means done
16	W1C	0x0	pid48_done PID48 Channel Status 1 means done
15	W1C	0x0	pid47_done PID47 Channel Status 1 means done
14	W1C	0x0	pid46_done PID46 Channel Status 1 means done
13	W1C	0x0	pid45_done PID45 Channel Status 1 means done
12	W1C	0x0	pid44_done PID44 Channel Status 1 means done
11	W1C	0x0	pid43_done PID43 Channel Status 1 means done
10	W1C	0x0	pid42_done PID42 Channel Status 1 means done
9	W1C	0x0	pid41_done PID41 Channel Status 1 means done
8	W1C	0x0	pid40_done PID40 Channel Status 1 means done
7	W1C	0x0	pid39_done PID39 Channel Status 1 means done
6	W1C	0x0	pid38_done PID38 Channel Status 1 means done
5	W1C	0x0	pid37_done PID37 Channel Status 1 means done
4	W1C	0x0	pid36_done PID36 Channel Status 1 means done
3	RW	0x0	pid35_done PID35 Channel Status 1 means done

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Bit	Attr	Reset Value	Description
2	W1C	0x0	pid34_done PID34 Channel Status 1 means done
1	W1C	0x0	pid33_done PID33 Channel Status 1 means done
0	RW	0x0	pid32_done PID32 Channel Status 1 means done

TSP_PTIx_PID_STS2
Address: Operational Base + offset (0x011c)
PTI PID Channel Status 2 Register

Bit	Attr	Reset Value	Description
31	RW	0x0	pid31_error PID31 Error Interrupt Status 1 means error detected
30	W1C	0x0	pid30_error PID30 Error Interrupt Status 1 means error detected
29	W1C	0x0	pid29_error PID29 Error Interrupt Status 1 means error detected
28	W1C	0x0	pid28_error PID28 Error Interrupt Status 1 means error detected
27	W1C	0x0	pid27_error PID27 Error Interrupt Status 1 means error detected
26	W1C	0x0	pid26_error PID26 Error Interrupt Status 1 means error detected
25	W1C	0x0	pid25_error PID25 Error Interrupt Status 1 means error detected
24	W1C	0x0	pid24_error PID24 Error Interrupt Status 1 means error detected
23	W1C	0x0	pid23_error PID23 Error Interrupt Status 1 means error detected
22	W1C	0x0	pid22_error PID22 Error Interrupt Status 1 means error detected

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Bit	Attr	Reset Value	Description
21	W1C	0x0	pid21_error PID21 Error Interrupt Status 1 means error detected
20	W1C	0x0	pid20_error PID20 Error Interrupt Status 1 means error detected
19	W1C	0x0	pid19_error PID19 Error Interrupt Status 1 means error detected
18	W1C	0x0	pid18_error PID18 Error Interrupt Status 1 means error detected
17	W1C	0x0	pid17_error PID17 Error Interrupt Status 1 means error detected
16	W1C	0x0	pid16_error PID16 Error Interrupt Status 1 means error detected
15	W1C	0x0	pid15_error PID15 Error Interrupt Status 1 means error detected
14	W1C	0x0	pid14_error PID14 Error Interrupt Status 1 means error detected
13	W1C	0x0	pid13_error PID13 Error Interrupt Status 1 means error detected
12	W1C	0x0	pid12_error PID12 Error Interrupt Status 1 means error detected
11	W1C	0x0	pid11_error PID11 Error Interrupt Status 1 means error detected
10	W1C	0x0	pid10_error PID10 Error Interrupt Status 1 means error detected
9	W1C	0x0	pid9_error PID9 Error Interrupt Status 1 means error detected
8	W1C	0x0	pid8_error PID8 Error Interrupt Status 1 means error detected
7	W1C	0x0	pid7_error PID7 Error Interrupt Status 1 means error detected

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Bit	Attr	Reset Value	Description
6	W1C	0x0	pid6_error PID6 Error Interrupt Status 1 means error detected
5	W1C	0x0	pid5_error PID5 Error Interrupt Status 1 means error detected
4	W1C	0x0	pid4_error PID4 Error Interrupt Status 1 means error detected
3	W1C	0x0	pid3_error PID3 Error Interrupt Status 1 means error detected
2	W1C	0x0	pid2_error PID2 Error Interrupt Status 1 means error detected
1	W1C	0x0	pid1_error PID1 Error Interrupt Status 1 means error detected
0	W1C	0x0	pid0_error PID0 Error Interrupt Status 1 means error detected

TSP_PTIx_PID_STS3
Address: Operational Base + offset (0x0120)
PTI PID Channel Status 3 Register

Bit	Attr	Reset Value	Description
31	W1C	0x0	pid63_error PID63 Error Interrupt Status 1 means error detected
30	W1C	0x0	pid62_error PID62 Error Interrupt Status 1 means error detected
29	W1C	0x0	pid61_error PID61 Error Interrupt Status 1 means error detected
28	W1C	0x0	pid60_error PID60 Error Interrupt Status 1 means error detected
27	W1C	0x0	pid59_error PID59 Error Interrupt Status 1 means error detected
26	W1C	0x0	pid58_error PID58 Error Interrupt Status 1 means error detected

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Bit	Attr	Reset Value	Description
25	W1C	0x0	pid57_error PID57 Error Interrupt Status 1 means error detected
24	W1C	0x0	pid56_error PID56 Error Interrupt Status 1 means error detected
23	W1C	0x0	pid55_error PID55 Error Interrupt Status 1 means error detected
22	W1C	0x0	pid54_error PID54 Error Interrupt Status 1 means error detected
21	W1C	0x0	pid53_error PID53 Error Interrupt Status 1 means error detected
20	W1C	0x0	pid52_error PID52 Error Interrupt Status 1 means error detected
19	W1C	0x0	pid51_error PID51 Error Interrupt Status 1 means error detected
18	W1C	0x0	pid50_error PID50 Error Interrupt Status 1 means error detected
17	W1C	0x0	pid49_error PID49 Error Interrupt Status 1 means error detected
16	W1C	0x0	pid48_error PID48 Error Interrupt Status 1 means error detected
15	W1C	0x0	pid47_error PID47 Error Interrupt Status 1 means error detected
14	W1C	0x0	pid46_error PID46 Error Interrupt Status 1 means error detected
13	W1C	0x0	pid45_error PID45 Error Interrupt Status 1 means error detected
12	W1C	0x0	pid44_error PID44 Error Interrupt Status 1 means error detected
11	W1C	0x0	pid43_error PID43 Error Interrupt Status 1 means error detected

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Bit	Attr	Reset Value	Description
10	W1C	0x0	pid42_error PID42 Error Interrupt Status 1 means error detected
9	W1C	0x0	pid41_error PID41 Error Interrupt Status 1 means error detected
8	W1C	0x0	pid40_error PID40 Error Interrupt Status 1 means error detected
7	W1C	0x0	pid39_error PID39 Error Interrupt Status 1 means error detected
6	W1C	0x0	pid38_error PID38 Error Interrupt Status 1 means error detected
5	W1C	0x0	pid37_error PID37 Error Interrupt Status 1 means error detected
4	W1C	0x0	pid36_error PID36 Error Interrupt Status 1 means error detected
3	W1C	0x0	pid35_error PID35 Error Interrupt Status 1 means error detected
2	W1C	0x0	pid34_error PID34 Error Interrupt Status 1 means error detected
1	W1C	0x0	pid33_error PID33 Error Interrupt Status 1 means error detected
0	W1C	0x0	pid32_error PID32 Error Interrupt Status 1 means error detected

TSP_PTIx_PID_INT_ENA0
Address: Operational Base + offset (0x0124)
PID Interrupt Enable Register 0

Bit	Attr	Reset Value	Description
31	RW	0x0	pid31_done_ena PID31 Done Enable 1:enabled 0:disabled

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Bit	Attr	Reset Value	Description
30	RW	0x0	pid30_done_ena PID30 Done Enable 1:enabled 0:disabled
29	RW	0x0	pid29_done_ena PID29 Done Enable 1:enabled 0:disabled
28	RW	0x0	pid28_done_ena PID28 Done Enable 1:enabled 0:disabled
27	RW	0x0	pid27_done_ena PID27 Done Enable 1:enabled 0:disabled
26	RW	0x0	pid26_done_ena PID26 Done Enable 1:enabled 0:disabled
25	RW	0x0	pid25_done_ena PID25 Done Enable 1:enabled 0:disabled
24	RW	0x0	pid24_done_ena PID24 Done Enable 1:enabled 0:disabled
23	RW	0x0	pid23_done_ena PID23 Done Enable 1:enabled 0:disabled
22	RW	0x0	pid22_done_ena PID22 Done Enable 1:enabled 0:disabled
21	RW	0x0	pid21_done_ena PID21 Done Enable 1:enabled 0:disabled
20	RW	0x0	pid20_done_ena PID20 Done Enable 1:enabled 0:disabled

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Bit	Attr	Reset Value	Description
19	RW	0x0	pid19_done_ena PID19 Done Enable 1:enabled 0:disabled
18	RW	0x0	pid18_done_ena PID18 Done Enable 1:enabled 0:disabled
17	RW	0x0	pid17_done_ena PID17 Done Enable 1:enabled 0:disabled
16	RW	0x0	pid16_done_ena PID16 Done Enable 1:enabled 0:disabled
15	RW	0x0	pid15_done_ena PID15 Done Enable 1:enabled 0:disabled
14	RW	0x0	pid14_done_ena PID14 Done Enable 1:enabled 0:disabled
13	RW	0x0	pid13_done_ena PID13 Done Enable 1:enabled 0:disabled
12	RW	0x0	pid12_done_ena PID12 Done Enable 1:enabled 0:disabled
11	RW	0x0	pid11_done_ena PID11 Done Enable 1:enabled 0:disabled
10	RW	0x0	pid10_done_ena PID10 Done Enable 1:enabled 0:disabled
9	RW	0x0	pid9_done_ena PID9 Done Enable 1:enabled 0:disabled

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Bit	Attr	Reset Value	Description
8	RW	0x0	pid8_done_ena PID8 Done Enable 1:enabled 0:disabled
7	RW	0x0	pid7_done_ena PID7 Done Enable 1:enabled 0:disabled
6	RW	0x0	pid6_done_ena PID6 Done Enable 1:enabled 0:disabled
5	RW	0x0	pid5_done_ena PID5 Done Enable 1:enabled 0:disabled
4	RW	0x0	pid4_done_ena PID4 Done Enable 1:enabled 0:disabled
3	RW	0x0	pid3_done_ena PID3 Done Enable 1:enabled 0:disabled
2	RW	0x0	pid2_done_ena PID2 Done Enable 1:enabled 0:disabled
1	RW	0x0	pid1_done_ena PID1 Done Enable 1:enabled 0:disabled
0	RW	0x0	pid0_done_ena PID0 Done Enable 1:enabled 0:disabled

TSP_PTIx_PID_INT_ENA1
Address: Operational Base + offset (0x0128)
PID Interrupt Enable Register 1

Bit	Attr	Reset Value	Description
31	RW	0x0	pid63_done PID63 Done Enable 1:enabled 0:disabled

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Bit	Attr	Reset Value	Description
30	RW	0x0	pid62_done PID62 Done Enable 1:enabled 0:disabled
29	RW	0x0	pid61_done PID61 Done Enable 1:enabled 0:disabled
28	RW	0x0	pid60_done PID60 Done Enable 1:enabled 0:disabled
27	RW	0x0	pid59_done PID59 Done Enable 1:enabled 0:disabled
26	RW	0x0	pid58_done PID58 Done Enable 1:enabled 0:disabled
25	RW	0x0	pid57_done PID57 Done Enable 1:enabled 0:disabled
24	RW	0x0	pid56_done PID56 Done Enable 1:enabled 0:disabled
23	RW	0x0	pid55_done PID55 Done Enable 1:enabled 0:disabled
22	RW	0x0	pid54_done PID54 Done Enable 1:enabled 0:disabled
21	RW	0x0	pid53_done PID53 Done Enable 1:enabled 0:disabled
20	RW	0x0	pid52_done PID52 Done Enable 1:enabled 0:disabled

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Bit	Attr	Reset Value	Description
19	RW	0x0	pid51_done PID51 Done Enable 1:enabled 0:disabled
18	RW	0x0	pid50_done PID50 Done Enable 1:enabled 0:disabled
17	RW	0x0	pid49_done PID49 Done Enable 1:enabled 0:disabled
16	RW	0x0	pid48_done PID48 Done Enable 1:enabled 0:disabled
15	RW	0x0	pid47_done PID47 Done Enable 1:enabled 0:disabled
14	RW	0x0	pid46_done PID46 Done Enable 1:enabled 0:disabled
13	RW	0x0	pid45_done PID45 Done Enable 1:enabled 0:disabled
12	RW	0x0	pid44_done PID44 Done Enable 1:enabled 0:disabled
11	RW	0x0	pid43_done PID43 Done Enable 1:enabled 0:disabled
10	RW	0x0	pid42_done PID42 Done Enable 1:enabled 0:disabled
9	RW	0x0	pid41_done PID41 Done Enable 1:enabled 0:disabled

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Bit	Attr	Reset Value	Description
8	RW	0x0	pid40_done PID40 Done Enable 1:enabled 0:disabled
7	RW	0x0	pid39_done PID39 Done Enable 1:enabled 0:disabled
6	RW	0x0	pid38_done PID38 Done Enable 1:enabled 0:disabled
5	RW	0x0	pid37_done PID37 Done Enable 1:enabled 0:disabled
4	RW	0x0	pid36_done PID36 Done Enable 1:enabled 0:disabled
3	RW	0x0	pid35_done PID35 Done Enable 1:enabled 0:disabled
2	RW	0x0	pid34_done PID34 Done Enable 1:enabled 0:disabled
1	RW	0x0	pid33_done PID33 Done Enable 1:enabled 0:disabled
0	RW	0x0	pid32_done PID32 Done Enable 1:enabled 0:disabled

TSP_PTIx_PID_INT_ENA2
Address: Operational Base + offset (0x012c)
PID Interrupt Enable Register 2

Bit	Attr	Reset Value	Description
31	RW	0x0	pid31_error PID31 Error Interrupt Enable 1:enabled 0:disabled

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Bit	Attr	Reset Value	Description
30	RW	0x0	pid30_error PID30 Error Interrupt Enable 1:enabled 0:disabled
29	RW	0x0	pid29_error PID29 Error Interrupt Enable 1:enabled 0:disabled
28	RW	0x0	pid28_error PID28 Error Interrupt Enable 1:enabled 0:disabled
27	RW	0x0	pid27_error PID27 Error Interrupt Enable 1:enabled 0:disabled
26	RW	0x0	pid26_error PID26 Error Interrupt Enable 1:enabled 0:disabled
25	RW	0x0	pid25_error PID25 Error Interrupt Enable 1:enabled 0:disabled
24	RW	0x0	pid24_error PID24 Error Interrupt Enable 1:enabled 0:disabled
23	RW	0x0	pid23_error PID23 Error Interrupt Enable 1:enabled 0:disabled
22	RW	0x0	pid22_error PID22 Error Interrupt Enable 1:enabled 0:disabled
21	RW	0x0	pid21_error PID21 Error Interrupt Enable 1:enabled 0:disabled
20	RW	0x0	pid20_error PID20 Error Interrupt Enable 1:enabled 0:disabled

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Bit	Attr	Reset Value	Description
19	RW	0x0	pid19_error PID19 Error Interrupt Enable 1:enabled 0:disabled
18	RW	0x0	pid18_error PID18 Error Interrupt Enable 1:enabled 0:disabled
17	RW	0x0	pid17_error PID17 Error Interrupt Enable 1:enabled 0:disabled
16	RW	0x0	pid16_error PID16 Error Interrupt Enable 1:enabled 0:disabled
15	RW	0x0	pid15_error PID15 Error Interrupt Enable 1:enabled 0:disabled
14	RW	0x0	pid14_error PID14 Error Interrupt Enable 1:enabled 0:disabled
13	RW	0x0	pid13_error PID13 Error Interrupt Enable 1:enabled 0:disabled
12	RW	0x0	pid12_error PID12 Error Interrupt Enable 1:enabled 0:disabled
11	RW	0x0	pid11_error PID11 Error Interrupt Enable 1:enabled 0:disabled
10	RW	0x0	pid10_error PID10 Error Interrupt Enable 1:enabled 0:disabled
9	RW	0x0	pid9_error PID9 Error Interrupt Enable 1:enabled 0:disabled

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Bit	Attr	Reset Value	Description
8	RW	0x0	pid8_error PID8 Error Interrupt Enable 1:enabled 0:disabled
7	RW	0x0	pid7_error PID7 Error Interrupt Enable 1:enabled 0:disabled
6	RW	0x0	pid6_error PID6 Error Interrupt Enable 1:enabled 0:disabled
5	RW	0x0	pid5_error PID5 Error Interrupt Enable 1:enabled 0:disabled
4	RW	0x0	pid4_error PID4 Error Interrupt Enable 1:enabled 0:disabled
3	RW	0x0	pid3_error PID3 Error Interrupt Enable 1:enabled 0:disabled
2	RW	0x0	pid2_error PID2 Error Interrupt Enable 1:enabled 0:disabled
1	RW	0x0	pid1_error PID1 Error Interrupt Enable 1:enabled 0:disabled
0	RW	0x0	pid0_error PID0 Error Interrupt Enable 1:enabled 0:disabled

TSP_PTIx_PID_INT_ENA3
Address: Operational Base + offset (0x0130)
PID Interrupt Enable Register 3

Bit	Attr	Reset Value	Description
31	RW	0x0	pid63_error PID63 Error Interrupt Enable 1:enabled 0:disabled

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Bit	Attr	Reset Value	Description
30	RW	0x0	pid62_error PID62 Error Interrupt Enable 1:enabled 0:disabled
29	RW	0x0	pid61_error PID61 Error Interrupt Enable 1:enabled 0:disabled
28	RW	0x0	pid60_error PID60 Error Interrupt Enable 1:enabled 0:disabled
27	RW	0x0	pid59_error PID59 Error Interrupt Enable 1:enabled 0:disabled
26	RW	0x0	pid58_error PID58 Error Interrupt Enable 1:enabled 0:disabled
25	RW	0x0	pid57_error PID57 Error Interrupt Enable 1:enabled 0:disabled
24	RW	0x0	pid56_error PID56 Error Interrupt Enable 1:enabled 0:disabled
23	RW	0x0	pid55_error PID55 Error Interrupt Enable 1:enabled 0:disabled
22	RW	0x0	pid54_error PID54 Error Interrupt Enable 1:enabled 0:disabled
21	RW	0x0	pid53_error PID53 Error Interrupt Enable 1:enabled 0:disabled
20	RW	0x0	pid52_error PID52 Error Interrupt Enable 1:enabled 0:disabled

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Bit	Attr	Reset Value	Description
19	RW	0x0	pid51_error PID51 Error Interrupt Enable 1:enabled 0:disabled
18	RW	0x0	pid50_error PID50 Error Interrupt Enable 1:enabled 0:disabled
17	RW	0x0	pid49_error PID49 Error Interrupt Enable 1:enabled 0:disabled
16	RW	0x0	pid48_error PID48 Error Interrupt Enable 1:enabled 0:disabled
15	RW	0x0	pid47_error PID47 Error Interrupt Enable 1:enabled 0:disabled
14	RW	0x0	pid46_error PID46 Error Interrupt Enable 1:enabled 0:disabled
13	RW	0x0	pid45_error PID45 Error Interrupt Enable 1:enabled 0:disabled
12	RW	0x0	pid44_error PID44 Error Interrupt Enable 1:enabled 0:disabled
11	RW	0x0	pid43_error PID43 Error Interrupt Enable 1:enabled 0:disabled
10	RW	0x0	pid42_error PID42 Error Interrupt Enable 1:enabled 0:disabled
9	RW	0x0	pid41_error PID41 Error Interrupt Enable 1:enabled 0:disabled

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Bit	Attr	Reset Value	Description
8	RW	0x0	pid40_error PID40 Error Interrupt Enable 1:enabled 0:disabled
7	RW	0x0	pid39_error PID39 Error Interrupt Enable 1:enabled 0:disabled
6	RW	0x0	pid38_error PID38 Error Interrupt Enable 1:enabled 0:disabled
5	RW	0x0	pid37_error PID37 Error Interrupt Enable 1:enabled 0:disabled
4	RW	0x0	pid36_error PID36 Error Interrupt Enable 1:enabled 0:disabled
3	RW	0x0	pid35_error PID35 Error Interrupt Enable 1:enabled 0:disabled
2	RW	0x0	pid34_error PID34 Error Interrupt Enable 1:enabled 0:disabled
1	RW	0x0	pid33_error PID33 Error Interrupt Enable 1:enabled 0:disabled
0	RW	0x0	pid32_error PID32 Error Interrupt Enable 1:enabled 0:disabled

TSP_PTIx_PCR_INT_STS
Address: Operational Base + offset (0x0134)
PTI PCR Interrupt Status Register

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
7	W1C	0x0	pcr7_done PCR7 Status 1: done; 0: not done;
6	W1C	0x0	pcr6_done PCR6 Status 1: done; 0: not done;
5	W1C	0x0	pcr5_done PCR5 Status 1: done; 0: not done;
4	W1C	0x0	pcr4_done PCR4 Status 1: done; 0: not done;
3	W1C	0x0	pcr3_done PCR3 Status 1: done; 0: not done;
2	W1C	0x0	pcr2_done PCR2 Status 1: done; 0: not done;
1	W1C	0x0	pcr1_done PCR1 Status 1: done; 0: not done;
0	W1C	0x0	pcr0_done PCR0 Status 1: done; 0: not done;

TSP_PTIx_PCR_INT_ENA
Address: Operational Base + offset (0x0138)
PTI PCR Interrupt Enable Register

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7	RW	0x0	pcr7_done_ena pcr7 done interrupt enable 1: enabled; 0: disabled;

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Bit	Attr	Reset Value	Description
6	RW	0x0	pcr6_done_ena pcr6 done interrupt enable 1: enabled; 0: disabled;
5	RW	0x0	pcr5_done_ena pcr5 done interrupt enable 1: enabled; 0: disabled;
4	RW	0x0	pcr4_done_ena pcr4 done interrupt enable 1: enabled; 0: disabled;
3	RW	0x0	pcr3_done_ena pcr3 done interrupt enable 1: enabled; 0: disabled;
2	RW	0x0	pcr2_done_ena pcr2 done interrupt enable 1: enabled; 0: disabled;
1	RW	0x0	pcr1_done_ena pcr1 done interrupt enable 1: enabled; 0: disabled;
0	RW	0x0	pcr0_done_ena pcr0 done interrupt enable 1: enabled; 0: disabled;

TSP_PTIx_PCRn_CTRL
Address: Operational Base + offset (0x013c)
PID PCR Control Register

Bit	Attr	Reset Value	Description
31:14	RO	0x0	reserved
13:1	RW	0x0000	pid PCR Extraction PID number This 13-bit field sets the PID number that needs PCR extraction.
0	RW	0x0	on PCR Extraction Switch 1'b1: PCR extraction switched on ; 1'b0: PCR extraction switched off ;

TSP_PTIx_PCRn_H
Address: Operational Base + offset (0x015c)
High Order PCR value

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Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RO	0x0	pcr PCR[32] pcr[32]

TSP_PTIx_PCRn_L
Address: Operational Base + offset (0x0160)
Low Order PCR value

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	pcr pcr[31:0] pcr[31:0]

TSP_PTIx_DMA_STS
Address: Operational Base + offset (0x019c)
LLP DMA Interrupt Status Register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	W1C	0x0	llp_error LLP DMA Error Status 1: error response during DMA transaction; 0: no error response during DMA transaction;
0	W1C	0x0	llp_done LLP DMA Done Status 1: DMA transaction completed; 0: DMA transaction not completed;

TSP_PTIx_DMA_ENA
Address: Operational Base + offset (0x01a0)
DMA Interrupt Enable Register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x0	llp_error_ena LLP DMA Error Interrupt Enable 1: enabled 0: disabled
0	RW	0x0	llp_done_ena LLP DMA Done Interrupt Enable 1: enabled 0: disabled

TSP_PTIx_DATA_FLAG0
Address: Operational Base + offset (0x01a4)
PTI_PID_WRITE Flag 0

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	data_write_flag_0 From PID0 TO PID31

TSP_PTIx_DATA_FLAG1
Address: Operational Base + offset (0x01a8)
PTI_PID_WRITE Flag 1

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	data_write_flag_1 From PID32 TO PID63

TSP_PTIx_LIST_FLAG
Address: Operational Base + offset (0x01ac)
PTIx_LIST_WRITE Flag

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0000	list_write_flag From PID0 TO PID15

TSP_PTIx_DST_STS0
Address: Operational Base + offset (0x01b0)
PTI Destination Status Register

Bit	Attr	Reset Value	Description
31:0	W1C	0x00000000	demux_dma_status_0 From 0 to 31 channel

TSP_PTIx_DST_STS1
Address: Operational Base + offset (0x01b4)
PTI Destination Status Register

Bit	Attr	Reset Value	Description
31:0	W1C	0x00000000	demux_dma_status_0 From 32 to 63 channel

TSP_PTIx_DST_ENA0
Address: Operational Base + offset (0x01b8)
PTI Destination Interrupt Enable Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	demux_dma_enable_0 From 0 to 31 channel

TSP_PTIx_DST_ENA1
Address: Operational Base + offset (0x01bc)
PTI Destination Interrupt Enable Register

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	demux_dma_enable_1 From 32 to 63 channel

TSP_PTIx_ECWn_H
Address: Operational Base + offset (0x0200)
The Even Control Word High Order

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ecw_h The Even Control Word High Order ECW[63:32]

TSP_PTIx_ECWn_L
Address: Operational Base + offset (0x0204)
The Even Control Word Low Order

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ecw_l The Even Control Word Low Order ECW[31:0]

TSP_PTIx_OCWn_H
Address: Operational Base + offset (0x0208)
The Odd Control Word High Order

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ocw_h The Odd Control Word High order OCW[63:32]

TSP_PTIx_OCWn_L
Address: Operational Base + offset (0x020c)
The Odd Control Word Low Order

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ocw_l The Odd Control Word Low Order OCW[31:0]

TSP_PTIx_PIDn_CTRL
Address: Operational Base + offset (0x0300)
PID Channel Control Register

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:16	RW	0x0	cw_num Control Word Order Number This fields indicates the corresponding order number of control word to be used to descramble TS packets.

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Bit	Attr	Reset Value	Description
15:3	RW	0x0000	pid PID number This 13-bit sets the desired PID number to be processed by PTI channel.
2	RW	0x0	csa_on Descrambling Switch 1'b1: Descrambling function turned on; 1'b0: Descrambling function turned off;
1	R/WSC	0x0	clear PID Channel Clear Write 1 to clear PID channel. This bit will be set to 0 if the channel is clear.
0	R/WSC	0x0	en PID Channel Enable Write 1 to enable channel. Write 0 to this bit will not take any effect. This bit will be 0 when channel is cleared.

TSP_PTIx_PIDn_BASE
Address: Operational Base + offset (0x0400)
PTI Data Memory Buffer Base Address

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	address PTI Data Memory Buffer Base Address PTI Data Memory Buffer Base Address

TSP_PTIx_PIDn_TOP
Address: Operational Base + offset (0x0404)
PTI Data Memory Buffer Top Address

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	address PTI Data Memory Buffer Top Address PTI Data Memory Buffer Top Address

TSP_PTIx_PIDn_WRITE
Address: Operational Base + offset (0x0408)
PTI Data Memory Buffer Hardware Writing Address

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	address PTI Data Memory Buffer Hardware Writing Address PTI Data Memory Buffer Hardware Writing Address

TSP_PTIx_PIDn_READ
Address: Operational Base + offset (0x040c)
PTI Data Memory Buffer Software Reading Address

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	address PTI Data Memory Buffer Software Reading Address PTI Data Memory Buffer Software Reading Address

TSP_PTIx_LISTn_BASE
Address: Operational Base + offset (0x0800)
PTI List Memory Buffer Base Address

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	address PTI Data Memory Buffer Software Reading Address PTI Data Memory Buffer Software Reading Address

TSP_PTIx_LISTn_TOP
Address: Operational Base + offset (0x0804)
PTI List Memory Buffer Top Address

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	address PTI List Memory Buffer Top Address PTI List Memory Buffer Top Address

TSP_PTIx_LISTn_WRITE
Address: Operational Base + offset (0x0808)
PTI List Memory Buffer Hardware Writing Address

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	address PTI List Memory Buffer Hardware Writing Address PTI List Memory Buffer Hardware Writing Address

TSP_PTIx_LISTn_READ
Address: Operational Base + offset (0x080c)
PTI List Memory Buffer Software Reading Address

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	address PTI List Memory Buffer Software Reading Address PTI List Memory Buffer Software Reading Address

TSP_PTIx_PIDn_CFG
Address: Operational Base + offset (0x0900)
PID Demux Configure Register

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	filter_en Filter Byte Enable The proper position of filter byte Enable. For Section filter. the 1st,4th,5th,..18th byte of section header are used to be filtered; For PES filter, the 4th,7th,8th...21th byte of pes header are used to be filtered.
15:12	RO	0x0	reserved
11	RW	0x0	scd_en Start Code Detection Switch Start code detection 1: enabled; 0: disabled; This bit is only valid when n < 16.
10	RW	0x0	cni_on Current Next Indicator Abort when current_next_indicator == 1'b1, 1'b1: abort ; 1'b0: do nothing ;
9:8	RW	0x0	filt_mode Section Filter Mode Filter Mode when the filter mode is configured as section filter. 2'b00: stop per unit; 2'b01: full stop; 2'b10: recycle, update when version number change 2'b11: reserverd
7:6	RW	0x0	video_type Video filtering Type 2'b00: MPEG2 2'b01: H264 2'b10: VC-1 2'b11: Reserved
5:4	RW	0x0	filt_type Filter Type 2'b00: section filtering; 2'b01: pes filtering; 2'b10: es filtering; 2'b11: ts filtering; if n>=16, it is reserved as only section filtering, other values are invalid.
3	RW	0x1	cc_abort Continue Counter Error Abort when continuity counter error happens: 1: abort; 0: do nothing;

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Bit	Attr	Reset Value	Description
2	RW	0x0	tei_abort Ts_error_indicator Abort when ts_error_indicator == 1: 1'b1: abort ; 1'b0: do nothing;
1	RW	0x0	crc_abort CRC Error Abort This bit is valid only when crc_on == 1'b1. When crc error happens, 1'b1: abort ; 1'b0: do nothing.
0	RW	0x0	crc_on CRC Check 1'b1: CRC check function turned on 1'b0: CRC check function turned off

TSP_PTIx_PIDn_FILT_0
Address: Operational Base + offset (0x0904)
Fliter Word 0

Bit	Attr	Reset Value	Description
31:24	RW	0x00	filt_byte_3 Fliter Byte 2 This byte refers to 6th byte of section header or 9th byte of pes header
23:16	RW	0x00	filt_byte_2 Fliter Byte 2 This byte refers to 5th byte of section header or 8th byte of pes header
15:8	RW	0x00	filt_byte_1 Fliter Byte 1 This byte refers to 4th byte of section header or 7th byte of pes header
7:0	RW	0x00	filt_byte_0 Fliter Byte 0 This byte refers to 1st byte of section header or 4th byte of pes header

TSP_PTIx_PIDn_FILT_1
Address: Operational Base + offset (0x0908)
Fliter Word 1

Bit	Attr	Reset Value	Description
31:24	RW	0x00	filt_byte_3 Fliter Byte 2 This byte refers to 10th byte of section header or 13rd byte of pes header

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Bit	Attr	Reset Value	Description
23:16	RW	0x00	filt_byte_2 Fliter Byte 2 This byte refers to 9th byte of section header or 12nd byte of pes header
15:8	RW	0x00	filt_byte_1 Fliter Byte 1 This byte refers to 8th byte of section header or 11st byte of pes header
7:0	RW	0x00	filt_byte_0 Fliter Byte 0 This byte refers to 7th byte of section header or 10th byte of pes header

TSP_PTIx_PIDn_FILT_2
Address: Operational Base + offset (0x090c)
Fliter Word 2

Bit	Attr	Reset Value	Description
31:24	RW	0x00	filt_byte_3 Fliter Byte 2 This byte refers to 14th byte of section header or 17th byte of pes header
23:16	RW	0x00	filt_byte_2 Fliter Byte 2 This byte refers to 13rd byte of section header or 16th byte of pes header
15:8	RW	0x00	filt_byte_1 Fliter Byte 1 This byte refers to 12nd byte of section header or 15th byte of pes header
7:0	RW	0x00	filt_byte_0 Fliter Byte 0 This byte refers to 11st byte of section header or 14th byte of pes header

TSP_PTIx_PIDn_FILT_3
Address: Operational Base + offset (0x0910)
Fliter Word 3

Bit	Attr	Reset Value	Description
31:24	RW	0x00	filt_byte_3 Fliter Byte 2 This byte refers to 18th byte of section header or 21st byte of pes header

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Bit	Attr	Reset Value	Description
23:16	RW	0x00	filt_byte_2 Fliter Byte 2 This byte refers to 17th byte of section header or 20th byte of pes header
15:8	RW	0x00	filt_byte_1 Fliter Byte 1 This byte refers to 16th byte of section header or 19th byte of pes header
7:0	RW	0x00	filt_byte_0 Fliter Byte 0 This byte refers to 15th byte of section header or 18th byte of pes header

25.4.3 MMU Register Summary

Name	Offset	Size	Reset Value	Description
TSP_MMU_DTE_ADDR	0x08800	W	0x00000000	MMU current page Table address
TSP_MMU_STATUS	0x08804	W	0x00000018	MMU status register
TSP_MMU_COMMAND	0x08808	W	0x00000000	MMU command register
TSP_MMU_PAGE_FAULT_ADDR	0x0880c	W	0x00000000	MMU logical address of last page fault
TSP_MMU_ZAP_ONE_LINE	0x08810	W	0x00000000	MMU Zap cache line register
TSP_MMU_INT_RAWSTAT	0x08814	W	0x00000000	MMU raw interrupt status register
TSP_MMU_INT_CLEAR	0x08818	W	0x00000000	MMU interrupt clear register
TSP_MMU_INT_MASK	0x0881c	W	0x00000000	MMU interrupt mask register
TSP_MMU_INT_STATUS	0x08820	W	0x00000000	MMU interrupt status register
TSP_MMU_AUTO_GATING	0x08824	W	0x00000001	MMU auto gating
TSP_MMU_MISS_CNT	0x08828	W	0x00000000	MMU miss counter
TSP_MMU_BURST_CNT	0x0882c	W	0x00000000	MMU burst counter

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

25.4.4 MMU Detail Register Description

TSP_MMU_DTE_ADDR

Address: Operational Base + offset (0x08800)

MMU current page Table address

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MMU_DTE_ADDR MMU dte base addr MMU dte base addr , the address must be 4kb aligned

TSP_MMU_STATUS

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Address: Operational Base + offset (0x08804)
MMU status register

Bit	Attr	Reset Value	Description
31:11	RO	0x0	reserved
10:6	RO	0x00	PAGE_FAULT_BUS_ID Index of master reponsible for last page fault
5	RO	0x0	PAGE_FAULT_IS_WRITE The direction of access for last page fault: 0 = Read 1 = Write
4	RO	0x1	REPLAY_BUFFER_EMPTY The MMU replay buffer is empty
3	RO	0x1	MMU_IDLE The MMU is idle when accesses are being translated and there are no unfinished translated accesses.
2	RO	0x0	STAIL_ACTIVE MMU stall mode currently enabled. The mode is enabled by command
1	RO	0x0	PAGE_FAULT_ACTIVE MMU page fault mode currently enabled . The mode is enabled by command.
0	RO	0x0	PAGING_ENABLED Paging is enabled

TSP_MMU_COMMAND
Address: Operational Base + offset (0x08808)
MMU command register

Bit	Attr	Reset Value	Description
31:3	RO	0x0	reserved
2:0	WO	0x0	MMU_CMD MMU_CMD. This can be: 0: MMU_ENABLE_PAGING 1: MMU_DISABLE_PAGING 2: MMU_ENABLE_STALL 3: MMU_DISABLE_STALL 4: MMU_ZAP_CACHE 5: MMU_PAGE_FAULT_DONE 6: MMU_FORCE_RESET

TSP_MMU_PAGE_FAULT_ADDR
Address: Operational Base + offset (0x0880c)
MMU logical address of last page fault

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	PAGE_FAULT_ADDR address of last page fault

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TSP_MMU_ZAP_ONE_LINE
Address: Operational Base + offset (0x08810)
MMU Zap cache line register

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	MMU_ZAP_ONE_LINE address to be invalidated from the page table cache

TSP_MMU_INT_RAWSTAT
Address: Operational Base + offset (0x08814)
MMU raw interrupt status register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x0	READ_BUS_ERROR read bus error
0	RW	0x0	PAGE_FAULT page fault

TSP_MMU_INT_CLEAR
Address: Operational Base + offset (0x08818)
MMU raw interrupt status register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	WO	0x0	READ_BUS_ERROR read bus error
0	WO	0x0	PAGE_FAULT page fault

TSP_MMU_INT_MASK
Address: Operational Base + offset (0x0881c)
MMU raw interrupt status register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x0	READ_BUS_ERROR read bus error enable an interrupt source if the corresponding mask bit is set to 1
0	RW	0x0	PAGE_FAULT page fault enable an interrupt source if the corresponding mask bit is set to 1

TSP_MMU_INT_STATUS
Address: Operational Base + offset (0x08820)
MMU raw interrupt status register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
1	RO	0x0	READ_BUS_ERROR read bus error
0	RO	0x0	PAGE_FAULT page fault

TSP_MMU_AUTO_GATING
Address: Operational Base + offset (0x08824)
mmu auto gating

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x1	mmu_auto_gating when it is 1'b1, the mmu will auto gating it self

TSP_MMU_mmu_miss_cnt
Address: Operational Base + offset (0x08828)
Register0000 Abstract

Bit	Attr	Reset Value	Description
31	RW	0x0	cnt_ctrl_sel sel the counter for mmu_miss or mmu_real_miss 1'b0: mmu_real_miss 1'b1: mmu_miss When sel 1'b1, an axi command miss may count for several times; when sel 1'b0, an axi command only count for a time
30	RW	0x0	miss_cnt_overflow_flag miss cnt overflow flag
29:0	RW	0x00000000	miss_cnt count for miss AXI command

TSP_MMU_mmu_burst_cnt
Address: Operational Base + offset (0x0882c)
Register0001 Abstract

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RW	0x0	bust_cnt_overflow_flag
29:0	RW	0x00000000	burst_cnt The AXI input burst counter

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25.5 Interface Description

Table 25-1 TSP interface description

Module Pin	Dir	Pad Name	IOMUX Setting
IOMUX0			
tsp_valid	I	IO_TSPvalidm0_CIFvsyncm0_SDMMC0EXTcmd_SPIclkm2_USB3PHYdebug1_I2S2sclkm1_GPIO3A0vccio6	GRF_GPIO3AL_IOMUX[2:0] = 3'b001

Module Pin	Dir	Pad Name	IOMUX Setting
tsp_fail	I	IO_TSPfail_CIFhref_SDMMC0EXTdet_SPItxdm2_USB3PHYdebug2_I2S2sdom1_GPIO3A1vccio6	GRF_GPIO3AL_IOMUX[5:3] = 3'b001
tsp_clk	I	IO_TSPclk_CIFclkin_SDMMC0EXTclkout_SPIrxdm2_USB3PHYdebug3_I2S2sdim1_GPIO3A2vccio6	GRF_GPIO3AL_IOMUX[8:6] = 3'b001
tsp_syncm0	I	IO_TSPsync_CIFclkout_SDMMC0EXTwp_GPIO3A3vccio6	GRF_GPIO3AL_IOMUX[11:9] = 3'b001
tsp_d0	I	IO_TSPd0_CIFda0_SDMMC0EXTd0_UART1tx_USB3PHYdebug4_GPIO3A4vccio6	GRF_GPIO3AL_IOMUX[14:12] = 3'b001
tsp_d1	I	IO_TSPd1_CIFdata1_SDMMC0EXTd1_UART1rtsn_USB3PHYdebug5_GPIO3A5vccio6	GRF_GPIO3AH_IOMUX[2:0] = 3'b001
tsp_d2	I	IO_TSPd2_CIFdata2_SDMMC0EXTd2_UART1rx_USB3PHYdebug6_GPIO3A6vccio6	GRF_GPIO3AH_IOMUX[5:3] = 3'b001
tsp_d3	I	IO_TSPd3_CIFdata3_SDMMC0EXTd3_UART1ctsn_USB3PHYdebug7_GPIO3A7vccio6	GRF_GPIO3AH_IOMUX[8:6] = 3'b001
tsp_d4	I	IO_TSPd4_CIFdata4_SPIcsn0m2_I2S2lrcktxm1_USB3PHYdebug8_I2S2lrckrxm1_GPIO3B0vccio6	GRF_GPIO3BL_IOMUX[2:0] = 3'b001
tsp_d5m0	I	IO_TSPd5m0_CIFdata5m0_GPIO3B1vccio6	GRF_GPIO3BH_IOMUX[3:2] = 2'b01
tsp_d6m0	I	IO_TSPd6m0_CIFdata6m0_GPIO3B2vccio6	GRF_GPIO3BH_IOMUX[5:4] = 2'b01
tsp_d7m0	I	IO_TSPd7m0_CIFdata7m0_GPIO3B3vccio6	GRF_GPIO3BH_IOMUX[7:6] = 2'b01
IOMUX1			
tsp_syncm1	I	IO_I2S1mclk_NOuse0_TSPsyncm1_CIFclkoutm1_GPIO2B7vccio5	GRF_GPIO2BH_IOMUX[2:0] = 3'b011
tsp_d5m1	I	IO_I2S1lrckrx_NOuse1_TSPd5m1_CIFdata5m1_GPIO2C0vccio5	GRF_GPIO2CL_IOMUX[2:0] = 3'b011
tsp_d6m1	I	IO_I2S1lrcktx_SPDIFtxm1_TSPd6m1_CIFdata6m1_GPIO2C1vccio5	GRF_GPIO2CL_IOMUX[5:3] = 3'b011
tsp_d7m1	I	IO_I2S1sclk_PDMclkm0_TSPd7m1_CIFdata7m1_GPIO2C2vccio5	GRF_GPIO2CL_IOMUX[8:6] = 3'b011

There are two groups of IO for tsp_sync and tsp_data[7:5]. Which group of IO to be used is controlled by GRF_IOMUX_CON[8] , this bit has a default value 1'b0. If this bit is set to 1'b1, the second group of IO is selected.

25.6 Application Notes

25.6.1 Overall Operation Sequence

- Enable desired modules to work by writing correspond bit with '1' in TSP_GCFG. Note: it is important to do this step at first, otherwise writing the corresponding registers will not take effect.
- Set up TS configuration by writing corresponding registers.
- Wait for the interrupts to pick up the desired TS packets following the rules detailed in the following section.

25.6.2 TS Source

TS source can be chosen by writing the bit 9 of TSP_PTIx_CTRL(x=0,1), '1' for

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demodulator, '0' for local memory.

1.TS_IN Interface

Writing bit 10 of TSP_PTIx_CTRL to choose bit ordering, and writing bit [12:11] to choose input TS mode.

TS_IN interface supports 4 input TS stream mode: sync/valid serial mode, sync/valid parallel mode, sync/burst parallel mode, nosync/valid parallel mode.

2.Local Memory

PTI also can process the TS data read from local memory by using LLP DMA mode.

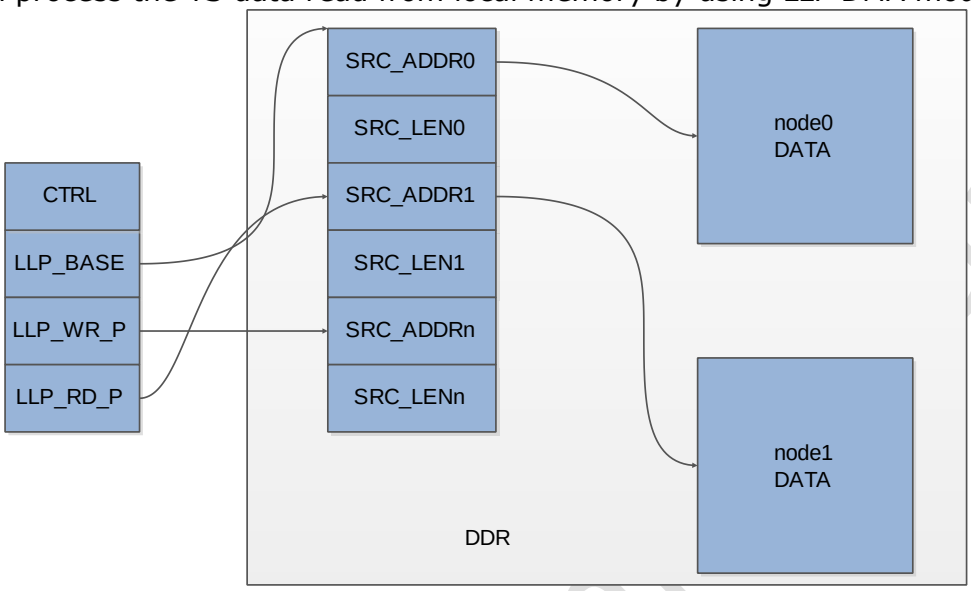


Fig. 25-6 LLPaddress architecture

(1) Write PTIx_LLP_BASE with the list base address;

(2) Starting from the list base address, write the list nodes. One list node comprised of two words. The first word describes the TS data base address, the second one describes the length of TS data in unit of word.

(3) Write the PTIx_LLP_WRITE with the number of words that you have written in list memory. Note it is not the number of LLP nodes, so that the number you are writing should be an even one.

(4) Write PTIx_LLP_CFG with the configuration you want. Write the bit 0 with 1 to start LLP DMA. If all the list nodes are written, don't forget to write 1 to bit 3 to tell DMAC that the configuration is finished.

Note:

- *The MSB(bit7) of the 8-bit pointer in the PTIx_LLP_Write and PTIx_LLP_Read is used as the flag bit, and remaining 7 bits are used for addressing. Therefore the the pointer is referred to 7-bit space, not 8-bit space, and remember write the pointer with the correct flag bit. For example, if you have configured 63 LLP nodes and then you have to write the 64th LLP node starting from the list base address,*
- *PTIx_LLP_READ informs that how many words has been processed by LLP DMA. An interrupt may be generated when number of the processed words has reach to the threshold set in the PTIx_LLP_CFG.*
- *If you write the PTIx_LLP_Write several times in a complete DMA transaction, it is important to notice the flag bit of PTIx_LLP_Write, and never make the writing pointer catch up with the reading pointer.*

25.6.3 TS Synchronous Operation

Synchronous mode and Bypass mode can be switched by writing bit 15 of TSP_PTIx_CTRL. In the synchronous mode, 188/192/204 byte TS packets are supported and self-adjusted. Set up locked times in TSP_PTIx_CTRL to inform the successive times of TS packet header detection needs to lock the header of TS packets when in the unlocked mode, and set up unlocked times to informs the successive times of TS packet header error needs to re-lock header of TS packets in the locked mode. It is recommended to use 2-3 as the locked times to quickly and correctly locked the header, and 2-3 as unlocked times to avoid

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unnecessarily entering into unlocked searching mode.
In the bypass mode, the input TS data will not be re-synchronized and directly fed into the PTI channel.

25.6.4 Descrambling Operation

Descrambler can achieve PES or TS level descrambling which conforms to the CSA v2.0.
Enable the channel you want by writing 1 to bit 0 of TSP_PTIx_PIDn_CTRL (x=0~1, n= 0~64);
Set the desired PID number
Turn on descrambling function by setting 1 to bit 2. If the corresponding CW is available or TS is required to be left undescrambled, CSA_ON bit is set to 0;
Choose corresponding Control Word by setting bit[19:16], and 16 set Control Word are available to be chosen. Don't forget Control Word should be preprared before the descrambling function is enabled.

Note: If the enabled channel is needed to be disabled, write the CLEAR bit to disabled the channel rather than write '0' to EN bit.

25.6.5 Demux Operation

Refer to TSP_PTIx_PIDn_CFG for Demux operation. The software users should be familiar with the demux knowledge.
Users should create a separate memory buffer to receive the processed data for each desired PID channel, and write the base and top address information of the memory buffer into TSP_PTIx_PIDn_BASE and TSP_PTIx_PIDn respectively. Also initial writing address and reading address, normally the same as base address, are also needed to be written into TSP_PTIx_PIDn_WRITE and TSP_PTIx_PIDn_READ respectively. For ES/PES filter, another separate memory needs to be created to store list data, which is used to assist obtaining PES/ES data. List base address, top address, initial writing address and reading address are also needed to write into corresponding registers.
Note:

For channel whose PID channel number larger than 15, the channels can only be used section filter. For others, there is no such limit. They can be configured as section filter, pes filter, es filter or ts filter.

Data memory address boundary should be aligned with word-size, and list memory address boundary should be aligned with word size. If the memory buffer is not larger to store processed data so that writing address reaches the top address, TSP will return to the base address to write data. So fetch the data in time, don't make the writing address catches up with reading address. The list memory buffer has the same issue.

Demux data obtain

1. TS filter
To obtain TS data and section data, when an desired PID done interrupt is generated, read TSP_PTIx_PIDn_READ firstly to know the address that last reading stops, and then read TSP_PTIx_PIDn_WRITE to know the address that hardware has reached. For ts data, start from the TSP_PTIx_PIDn_READ address to get the TS packet data, and stop at the address you want. However, the ending address should not catch up with writing address. It is recommended to obtain the TS data in the unit of TS packet which is 47-word size. At last, don't forget to write the ending address into TSP_PTIx_PIDn_READ to leave a hint where current reading stops.

B. Section filter
Section filter can run three mode to meet different needs: stop-per-unit; full stop; recycle , update when version number change. The PID done interrupt will be generated after each part of a complete section is processed in the first mode, and the PID done will be generated only after the whole section is completed in the last two modes. In the frist two mode, the PID channel will be disabled after the whole section is completed. In the recycle mode, the channel will remain active and start a new section processing when the version number changes. Section filter also supports 16-byte filtering function, which can assign 1st , 4th to 18th byte to be filtered.

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The process to obtain section data is similar to the process for TS data. After a PID done interrupt done is generated, refer to the corresponding PID error status register to check if the section data is correct. Read the frist word of the section start address to know the total length of the section according to the format of section data.
Section Length = {First Word[11:8], First Word[23:16]};
Total Length = Section Length;
Then start to fetch section data according to the total length. Again don't forget to write the stopped address.

C. PES/ES filter

PES filter supports 16-byte filtering function, which can assign 4th, 7th to 21st byte to be filtered.
ES filter supports start code detection, including MPEG2 start code 0x000001b3, 0x00000100, VC-1 start code 0x0000010d, 0x000010f, H264 start code 0x00001.
To obtain the pes/es data, the assistant of list descriptor is needed.

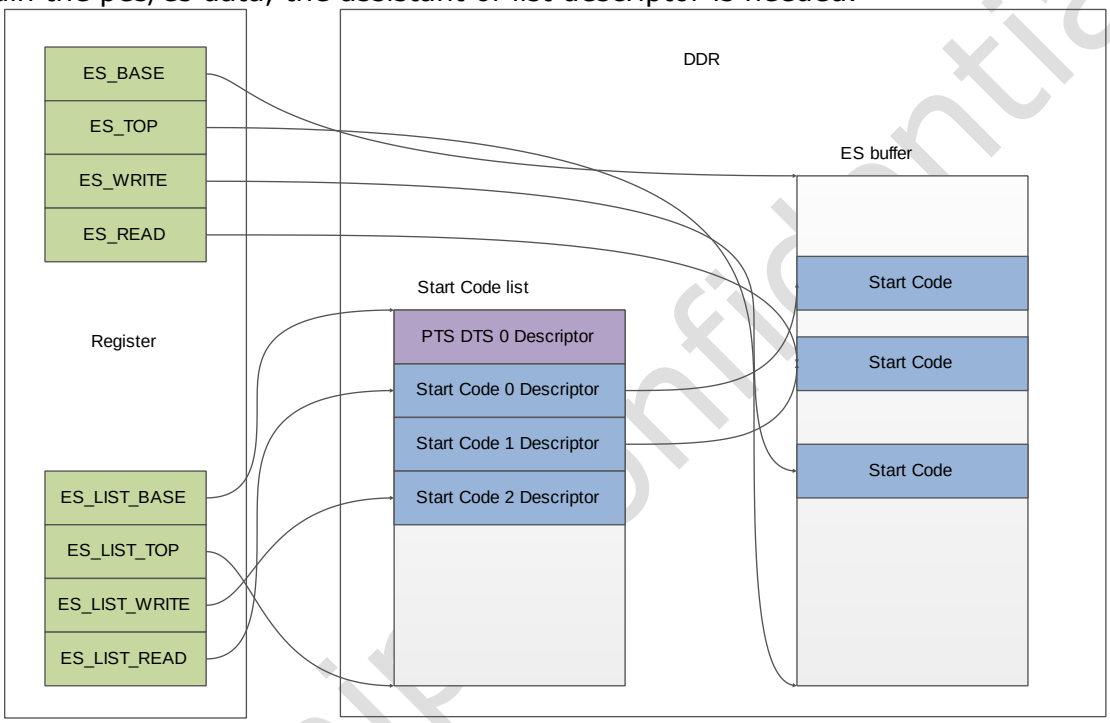


Fig. 25-7 LLPmemory architecture

List memory buffer contains descriptors which contains information to obtain es/pes data which are stored in data memory buffer.
The descriptor stored in list memory buffer can be separated into two groups: PTS_DTS Descriptor and Start Code Descriptor. The descriptor is composed by 4 word content, word_0, word_1, word_2 and word_3. The word_x (x means the sequence number in a descriptor, and they are stored in the memory in sequence order). The format of the 4 words are listed as follows:

start code descriptor

Word_0:
Word_0[29:28] indicates the attributes of the bytes of the pointed word. 2'b00 means the whole word belongs to the new ES/PES packet; 2'b01 means that word[7:0] belongs to the previous packet, and the remaining bytes belong to the new packet; 2'b10 means means that word[15:0] belongs to the previous packet, and the remaining bytes belong to the new packet; 2'b11 means 'b10 means means that word[23:0] belongs to the previous packet, and the remaining bytes belong to the new packet. This pointed word is the word where start code starts, word_2 describes the location of start code.
Word_0[27:24] is equal to 0x0 in the start code descriptor. Users can used to tell two kinds of descriptor.
If the video type is H.264, word_0[23:8] means first_mb_in slice, and word_0 means nal_nuit_type.

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Word_1:
the start code of stream.

Word_2:
DDR offset address in the DDR of the word where the start code is located.

Word_3:
0x0

PTS_DTS Descriptor
Word_0:
Word_0[29:28]: the same as start code descriptor
Word_0[27:24]: 0x1 in PTS_DTS descriptor.
Word_0[3] : PTS[32];
Word_0[2] : DTS[32];
Word_0[1:0] : pts_dts_flag;

Word_1:
DDR offset address of the word that valid data starts.

Word_2:
PTS[31:0]

Word_3
DTS[31:0]

To obtain PES data or ES data when start code detection is disabled, use PTS_DTS descriptor. To obtain ES data when start code detection is enabled, use start code descriptor.
When a PID done interrupt is generated, make sure there is no corresponding PID error generated. Read the TSP_PTIx_LISTn_READ to know the list reading address in the last time. Start from here, read the 4-word descriptor one by one to know the offset of the packets. Refer to the offset in the DDR where in the data memory buffer to obtain data. Finally write TSP_PTIx_LISTn_READ and TSP_PTIx_PIDn_READ with corresponding reading address.

25.6.6 PVR

PVR module provide you with the function to record the programs you want. The 4 sources can be assigned with PVR, and they are the same as TS out interface.
Assign the PVR length and PVR address, and then configure TSP_PVR_CTRL to start PVR module. If you want to stop PVR function during recording, write '1' to STOP bit (bit 0) to to TSP_PVR_CTRL to stop it. Remember to take care of the status of PVR_ON bit of TSP_GFCG when programming the PVR-related registers.

25.6.7 PCR extraction

PCR extraction can be enabled by configure PTIx_PCRn_CTRL. Then if the PID-matched TS data contain PCR field, the 33-bit PCR_base field will be written corresponding PTIx_PCRn_H and PTIx_PCRn_L registers. An interrupt will be asserted if PCR interrupt is enabled.

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Chapter 26 SAR-ADC

26.1 Overview

The ADC is a4-channel (0/1/2/6) signal-ended 10-bit Successive Approximation Register (SAR) A/D Converter. It uses the supply and ground as it reference which avoid use of any external reference. It converts the analog input signal into 10-bit binary digital codes at maximum conversion rate of 100KSPS with 1MHz A/D converter clock.

26.2 Block Diagram

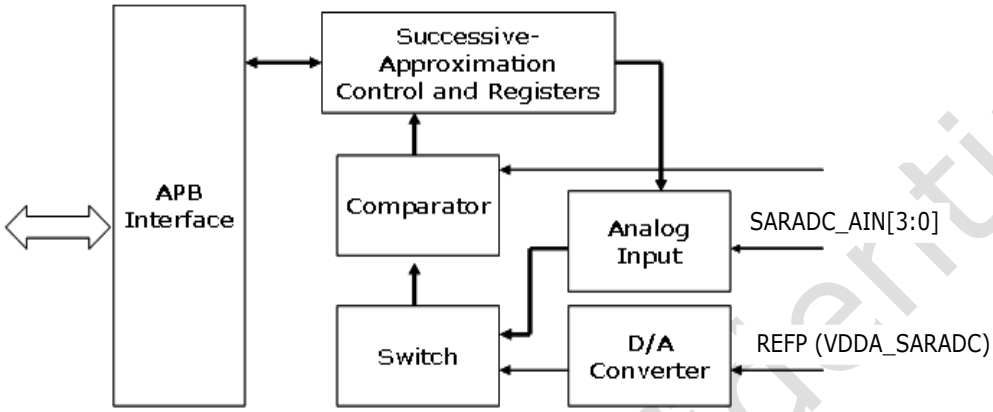


Fig. 26-1 SAR-ADC Block Diagram

- Successive-Approximate Register and Control Logic Block

This block is exploited to realize binary search algorithm, storing the intermediate result and generate control signal for analog block.

- Comparator Block

This block compares the analog input SARADC_AIN[3:0] with the voltage generated from D/A Converter, and output the comparison result to SAR and Control Logic Block for binary search. Three level amplifiers are employed in this comparator to provide enough gain.

26.3 Function Description

In PX3 SE, SAR-ADC works at single-sample operation mode.
This mode is useful to sample an analog input when there is a gap between two samples to be converted. In this mode START is asserted only on the rising edge of CLKIN where conversion is needed. At the end of every conversion EOC signal is made high and valid output data is available at the rising edge of EOC. The detailed timing diagram will be shown in the following.

26.4 Register Description

26.4.1 Registers Summary

Name	Offset	Size	Reset Value	Description
SARADC_DATA	0x0000	W	0x00000000	This register contains the data after A/D Conversion.
SARADC_STAS	0x0004	W	0x00000000	The status register of A/D Converter.
SARADC_CTRL	0x0008	W	0x00000000	The control register of A/D Converter.
SARADC_DLY_PU_SOC	0x000c	W	0x00000000	delay between power up and start command

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

26.4.2 Detail Register Description

SARADC_DATA

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Address: Operational Base + offset (0x0000)
This register contains the data after A/D Conversion.

Bit	Attr	Reset Value	Description
31:10	RO	0x0	reserved
9:0	RO	0x000	adc_data A/D value of the last conversion (DOUT[9:0])

SARADC_STAS
Address: Operational Base + offset (0x0004)
The status register of A/D Converter.

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RO	0x0	adc_status ADC status (EOC) 1'b0: ADC stop 1'b1: Conversion in progress

SARADC_CTRL
Address: Operational Base + offset (0x0008)
The control register of A/D Converter.

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5	RW	0x0	int_status Interrupt status. This bit will be set to 1 when end of conversion. Set 0 to clear the interrupt.
4	RW	0x0	int_en Interrupt enable. 1'b0: Disable 1'b1: Enable
3	RW	0x0	adc_power_ctrl ADC power down control bit 1'b0: ADC power down 1'b1: ADC power up and reset start signal will be asserted (DLY_PU_SOC+2) sclk clock period later after power up
2:0	RW	0x0	adc_input_src_sel ADC input source selection (CH_SEL[2:0]). 3'b000: Input source 0 (SARADC_AIN[0]) 3'b001: Input source 1 (SARADC_AIN[1]) 3'b010: Input source 2 (SARADC_AIN[2]) 3'b110: Input source 3 (SARADC_AIN[3]) Others : Reserved

SARADC_DLY_PU_SOC
Address: Operational Base + offset (0x000C)
delay between power up and start command.

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
5:0	RW	0x08	delay between power up and start command The start signal will be asserted (DLY_PU_SOC + 2) sclk clock period later after power up

26.5 Timing Diagram

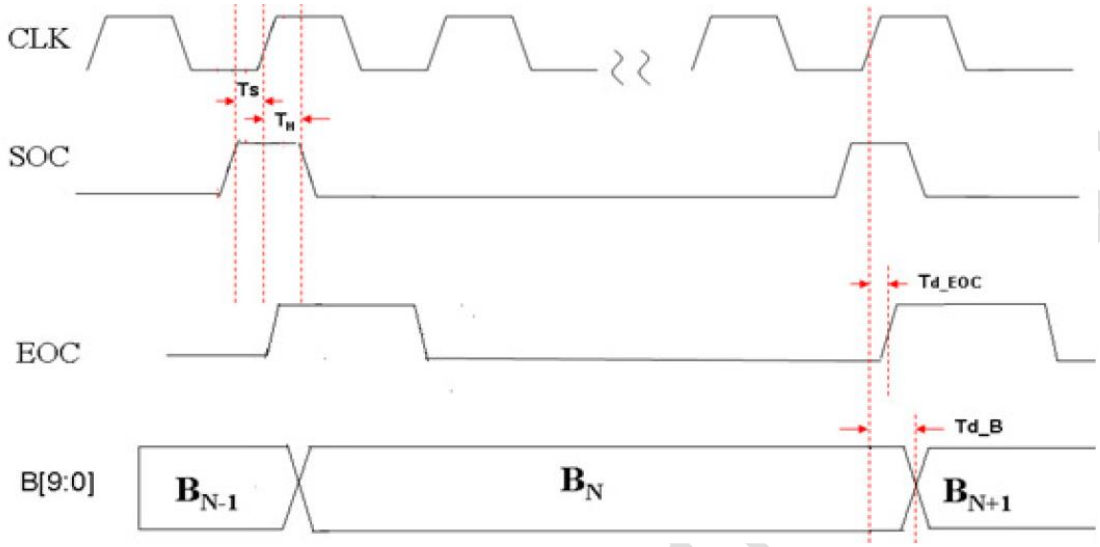


Fig. 26-2 SAR-ADC timing diagram in single-sample conversion mode

Table 26-1 SAR-ADC timing parameters list

Parameter	symbol	value			unit
		min	typ	max	
Setup time for SOC	T_S	0			ns
Hold time for SOC	T_H	10			ns
EOC delay from rising edge of CLK	T_{D_EOC}			10.9	ns
B[9:0] delay from rising edge of CLK	T_{d_B}			11.1	ns
CLK period		90			ns

26.6 Application Notes

Steps of adc conversion:

- Write SARADC_CTRL[3] as 0 to power down adc converter.
- Write SARADC_CTRL[2:0] as n to select adc channel(n).
- Write SARADC_CTRL[4] as 1 to enable adc interrupt.
- Write SARADC_CTRL[3] as 1 to power up adc converter.
- Wait for adc interrupt or poll SARADC_STAS register to assert whether the conversion is completed
- Read the conversion result from SARADC_DATA[9:0]

Note: The A/D converter was designed to operate at maximum 1MHZ.

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Chapter 27 Serial Flash Controller (SFC)

27.1 Overview

The serial flash controller (SFC) is used to control the data transfer between the chip system and the serial nor/nand flash device.
The SFC supports the following features:

- Support AHB slave interface to configure register and read/write serial flash
- Support AHB master interface to transfer data from/to spi flash device
- Support two independent clock domain: AHB clock and SPI clock
- Support x1,x2,x4 data bits mode
- Support 1 chip select
- Support interrupt output, interrupt maskable
- Support Spansion, MXIC,Gigadevice…vendor's nor flash memory.

27.2 Block Diagram

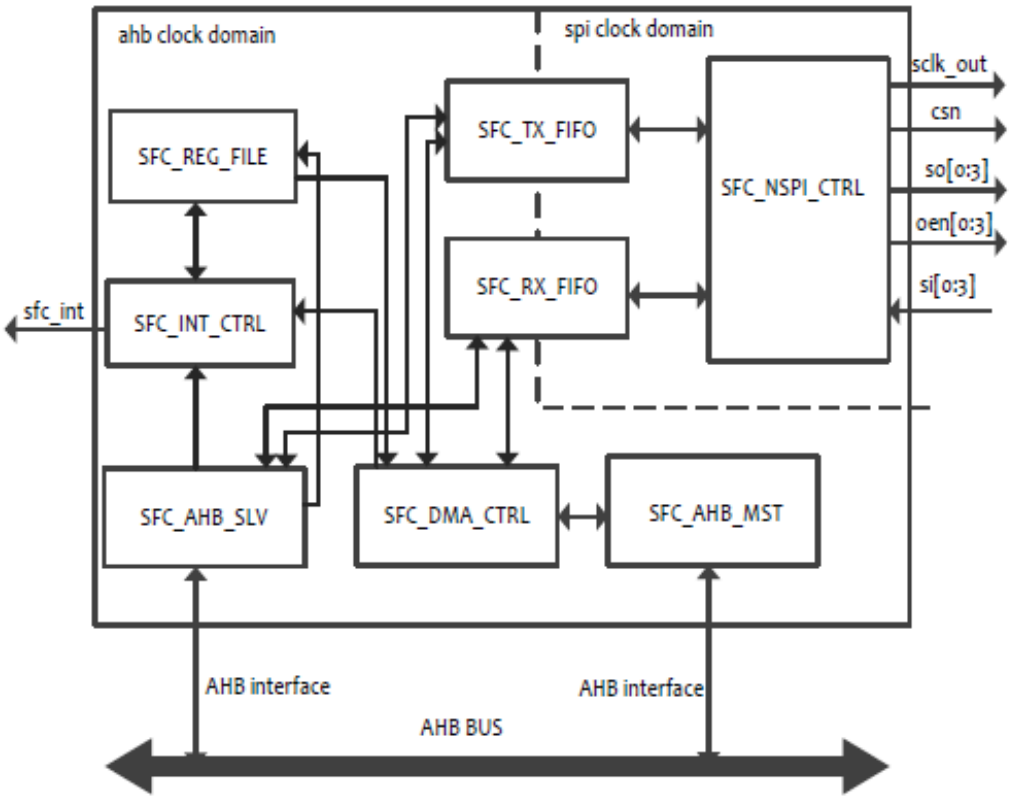


Fig. 27-1 SFC Block Diagram

27.3 Function Description

27.3.1 AHB Interface

The ahb slave is used to configure the register, and also write to/read from the serial nor/nand flash device.
The SFC_CTRL register is a global control register, when the controller is in busy state(SFC_SR), SFC_CTRL cannot be set. The field sclk_idle_level_cycles of this register is used to configure the idle level cycles of sclk before read the first bit of the read command. Like the following picture shows: the red line of the sclk is the idle cycles, during these cycles, the chip pad is switched to output. When sclk_idle_level_cycles=0, it means there will be not such idle level.

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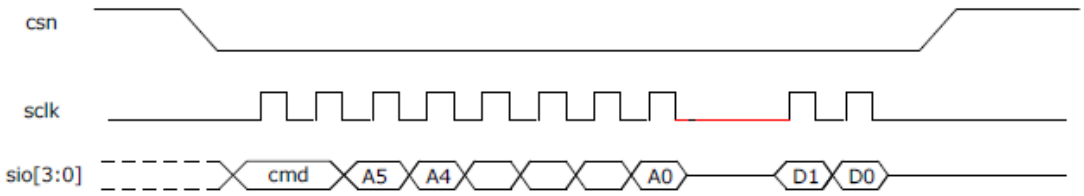


Fig. 27-2 SFC busy state timing diagram

When the field spi mode is set, the transfer waveform will like following, and switch to mode3.

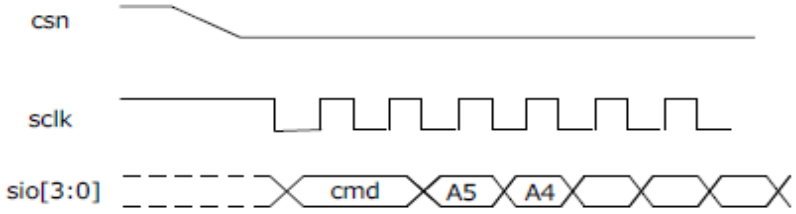


Fig. 27-3 SFC spi mode timing diagram

27.4 Register Description

27.4.1 Registers Summary

Table 27-1 SFC Register Description

Name	Offset	Size	Reset Value	Description
SFC_CTRL	0x0000	W	0x00000000	Control Register 0
SFC_IMR	0x0004	W	0x00000000	Interrupt Mask
SFC_ICLR	0x0008	W	0x00000000	Interrupt Clear
SFC_FTLR	0x000c	W	0x00000000	FIFO Threshold Level
SFC_RCVR	0x0010	W	0x00000000	SFC Recover
SFC_AX	0x0014	W	0x00000000	SFC AX Value
SFC_ABIT	0x0018	W	0x00000000	Flash Address bits
SFC_ISR	0x001c	W	0x00000000	Interrupt Status
SFC_FSR	0x0020	W	0x00000001	FIFO Status
SFC_SR	0x0024	W	0x00000000	SFC Status
SFC_RISR	0x0028	W	0x00000000	Raw Interrupt Status
SFC_VER	0x002c	W	0x05eb0001	Version Register
SFC_DMATR	0x0080	W	0x00000000	DMA Trigger
SFC_DMAADDR	0x0084	W	0x00000000	DMA Address
SFC_CMD	0x0100	W	0x00000000	SFC CMD
SFC_ADDR	0x0104	W	0x00000000	SFC Address
SFC_DATA	0x0108	W	0x00000000	SFC DATA

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

27.4.2 Detail Register Description

SFC_CTRL

Address: Operational Base + offset (0x0000)

Control Register 0

Bit	Attr	Reset Value	Description
31:14	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
13:12	RW	0x0	DATB Data bits width 00: 1bit 01: 2bits 10: 4bits
11:10	RW	0x0	ADRB Address bits width 00: 1bit 01: 2bits 10: 4bits
9:8	RW	0x0	CMDB Command bits width 00: 1bit 01: 2bits 10: 4bits 11:reserved
7:4	RW	0x0	IDLE_CYCLE Sclk Idle Level Cycles 4'b0: idel hold is disable 4'b1: hold the sclk_out in idle for two cycles when switch to shift in ....
3:2	RO	0x0	reserved
1	RW	0x0	SHIFTPHASE Shift Phase Select 0: shift in the data at posedge sclk_out 1: shift in the data at negedge sclk_out
0	RW	0x0	SPIM SPI MODE Select 0: mode 0 1: mode 3

SFC_IMR

Address: Operational Base + offset (0x0004)

Interrupt Mask

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7	RW	0x0	DMAM DMA finish interrupt mask 0: dma_intr interrupt is not masked 1: dma_intr interrupt is masked
6	RW	0x0	NSPIM SPI Error interrupt mask 0: nspi_intr interrupt is not masked 1: nspi_intr interrupt is masked

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Bit	Attr	Reset Value	Description
5	RW	0x0	AHBM AHB Error interrupt mask 0: ahb_intr interrupt is not masked 1: ahb_intr interrupt is masked
4	RW	0x0	TRANSM Transfer finish Interrupt Mask 0: transf_intr interrupt is not masked 1: transf_intr interrupt is masked
3	RW	0x0	TXEM Transmit FIFO Empty Interrupt Mask 0: txe_intr interrupt is not masked 1: txe_intr interrupt is masked
2	RW	0x0	TXOM Transmit FIFO Overflow Interrupt Mask 0: txo_intr interrupt is not masked 1: txo_intr interrupt is masked
1	RW	0x0	RXUM Receive FIFO Underflow Interrupt Mask 0: rxu_intr interrupt is not masked 1: rxu_intr interrupt is masked
0	RW	0x0	RXFM Receive FIFO Full Interrupt Mask 0: rxf_intr interrupt is not masked 1: rxf_intr interrupt is masked

SFC_ICLR
Address: Operational Base + offset (0x0008)
Interrupt Clear

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7	W1C	0x0	DMAC DMA finish Interrupt Clear Write and clear
6	W1C	0x0	NSPIC SPI Error Interrupt Clear Write and clear
5	W1C	0x0	AHBC AHB Error Interrupt Clear Write and clear
4	W1C	0x0	TRANSC Transfer finish Interrupt Clear Write and clear

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Bit	Attr	Reset Value	Description
3	W1C	0x0	TXEC Transmit FIFO Empty Interrupt Clear Write and clear
2	W1C	0x0	TXOC Transmit FIFO Overflow Interrupt Clear Write and clear
1	W1C	0x0	RXUC Receive FIFO Underflow Interrupt Clear Write and clear
0	W1C	0x0	RXFC Receive FIFO Full Interrupt Clear Write and clear

SFC_FTLR
Address: Operational Base + offset (0x000c)
FIFO Threshold Level

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:8	RW	0x00	RXFTLR Receive FIFO Threshold Level When the number of receive FIFO entries is bigger than or equal to this value, the receive FIFO full interrupt is triggered.
7:0	RW	0x00	TXFTLR Transmit FIFO Threshold Level When the number of transmit FIFO entries is less than or equal to this value, the transmit FIFO empty interrupt is triggered.

SFC_RCVR
Address: Operational Base + offset (0x0010)
SFC Recover

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	W	0x0	RCVR SFC Recover SFC Recover Write 1 to recover the SFC State Machine, FIFO state and other logic state.

SFC_AX
Address: Operational Base + offset (0x0014)

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SFC AX Value

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RO	0x00	AX The AX Value when doing the continuous read(enhance mode).

SFC_ABIT

Address: Operational Base + offset (0x0018)

Flash Address bits

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4:0	RW	0x0	ABIT Flash Address bits Flash Address bits

SFC_ISR

Address: Operational Base + offset (0x001c)

Interrupt Status

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7	RW	0x0	DMAS DMA Finish Interrupt Status 0: not active 1: active
6	RW	0x0	NSPIS SPI Error Interrupt Status 0: not active 1: active
5	RW	0x0	AHBS AHB Error Interrupt Status 0: not active 1: active
4	RW	0x0	TRANSS Transfer finish Interrupt Status 0: not active 1: active
3	RW	0x0	TXES Transmit FIFO Empty Interrupt Status 0: not active 1: active
2	RW	0x0	TXOS Transmit FIFO Overflow Interrupt Status 0: not active 1: active

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Bit	Attr	Reset Value	Description
1	RW	0x0	RXUS Receive FIFO Underflow Interrupt Status 0: not active 1: active
0	RW	0x0	RXFS Receive FIFO Full Interrupt Status 0: not active 1: active

SFC_FSR
Address: Operational Base + offset (0x0020)
FIFO Status

Bit	Attr	Reset Value	Description
31:21	RO	0x0	reserved
20:16	RW	0x00	RXWLVL RX FIFO Water Level 0: fifo is empty 1: 1 entry is taken ...
15:13	RO	0x0	reserved
12:8	RO	0x00	TXWLVL TX FIFO Water Level 0: fifo is full 1: left 1 entry ...
7:4	RO	0x0	reserved
3	RO	0x0	RXFS Receive FIFO Full Status 0: rx fifo is not full 1: rx fifo is full
2	RO	0x0	RXES Receive FIFO Empty Status 0: rx fifo is not empty 1: rx fifo is empty
1	RO	0x0	TXES Transmit FIFO Empty Status 0: tx fifo is not empty 1: tx fifo is empty
0	RO	0x1	TXFS Transmit FIFO Full Status 0: tx fifo is not full 1: tx fifo is full

SFC_SR
Address: Operational Base + offset (0x0024)

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SFC Status

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	WO	0x0	SR SFC Status 0: SFC is idle 1: SFC is busy When busy, don't set the control register.

SFC_RISR

Address: Operational Base + offset (0x0028)

Raw Interrupt Status

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7	RW	0x0	DMAS DMA Finish Interrupt Status 0: not active 1: active
6	RW	0x0	NSPIS SPI Error Interrupt Status 0: not active 1: active
5	RW	0x0	AHBS AHB Error Interrupt Status 0: not active 1: active
4	RW	0x0	TRANSS Transfer finish Interrupt Status 0: not active 1: active
3	RW	0x0	TXES Transmmit FIFO Empty Interrupt Status 0: not active 1: active
2	RW	0x0	TXOS Transmmit FIFO Overflow Interrupt Status 0: not active 1: active
1	RW	0x0	RXUS Receive FIFO Underflow Interrupt Status 0: not active 1: active
0	RW	0x0	RXFS Receive FIFO Full Interrupt Status 0: not active 1: active

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SFC_VER
Address: Operational Base + offset (0x002c)
Version Register

Bit	Attr	Reset Value	Description
31:0	RO	0x05eb0001	VER Version Register Version Register

SFC_DMATR
Address: Operational Base + offset (0x0080)
DMA Trigger

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	W1C	0x0	DMATR DMA Trigger Write 1 to start the dma transfer.

SFC_DMAADDR
Address: Operational Base + offset (0x0084)
DMA Address

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	DMAADDR DMA Address

SFC_CMD
Address: Operational Base + offset (0x0100)
SFC CMD

Bit	Attr	Reset Value	Description
31:30	RW	0x0	CS Flash chip select 00: chip select 0 01: chip select 1 10: chip select 2 11: chip select 3
29:16	RW	0x0000	TRB Transfer Bytes number Total Data Bytes number that will write to /read from the flash.

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Bit	Attr	Reset Value	Description
15:14	RW	0x0	ADDRB Address bits number select 00: 0bits 01: 24bits 10: 32bits 11: From the ABIT register
13	RW	0x0	CONT Continuous read mode 0: disable continuous read mode 1: enable continuous read mode
12	RW	0x0	WR Flash Write or Read 0:read 1:write
11:8	WO	0x0	DUMM Dummy Bits Number Dummy Bits Number
7:0	WO	0x00	CMD Flash CMD Flash Command

SFC_ADDR
Address: Operational Base + offset (0x0104)
SFC Address

Bit	Attr	Reset Value	Description
31:0	RW	0x0	ADDR SFC Address Flash's address

SFC_DATA
Address: Operational Base + offset (0x0108)
SFC DATA

Bit	Attr	Reset Value	Description
31:0	RW	0x0	DATA SFC DATA Flash's Data

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27.5 Interface Description

Table 27-2 SFC Interface Description

Module Pin	Dir	Pad Name	IOMUX Setting
sfc_clk	O	IO_NANDrdy_EMMCcmd1_SFCclk_GPIO2a4	GRF_GPIO2A_IOMUX[9:8]=2'b11
sfc_csn0	O	IO_NANDwrn_SFCcsn0_GPIO2a2	GRF_GPIO2A_IOMUX[5:4]=2'b10
sfc_cs1	O	IO_NANDrdn_SFCcsn1_GPIO2a3	GRF_GPIO2A_IOMUX[7:6]=2'b10
sfc_sioio0	I/O	IO_NANDd0_EMMCd0_SFCd0_GPIO1d0	GRF_GPIO1D_IOMUX[1:0]=2'b11

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Module Pin	Dir	Pad Name	IOMUX Setting
sfc_sioio1	I/O	IO_NANDd1_EMMCd1_SFCd1_GPIO1d1	GRF_GPIO1D_IOMUX[3:2]=2'b11
sfc_wpio2	I/O	IO_NANDd2_EMMCd2_SFCd2_GPIO1d2	GRF_GPIO1D_IOMUX[5:4]=2'b11
sfc_holdio3	I/O	IO_NANDd3_EMMCd3_SFCd3_GPIO1d3	GRF_GPIO1D_IOMUX[7:6]=2'b11

Notes: I=input, O=output, I/O=input/output, bidirectional

27.6 Application Notes

27.6.1 AHB Slave write flash flow

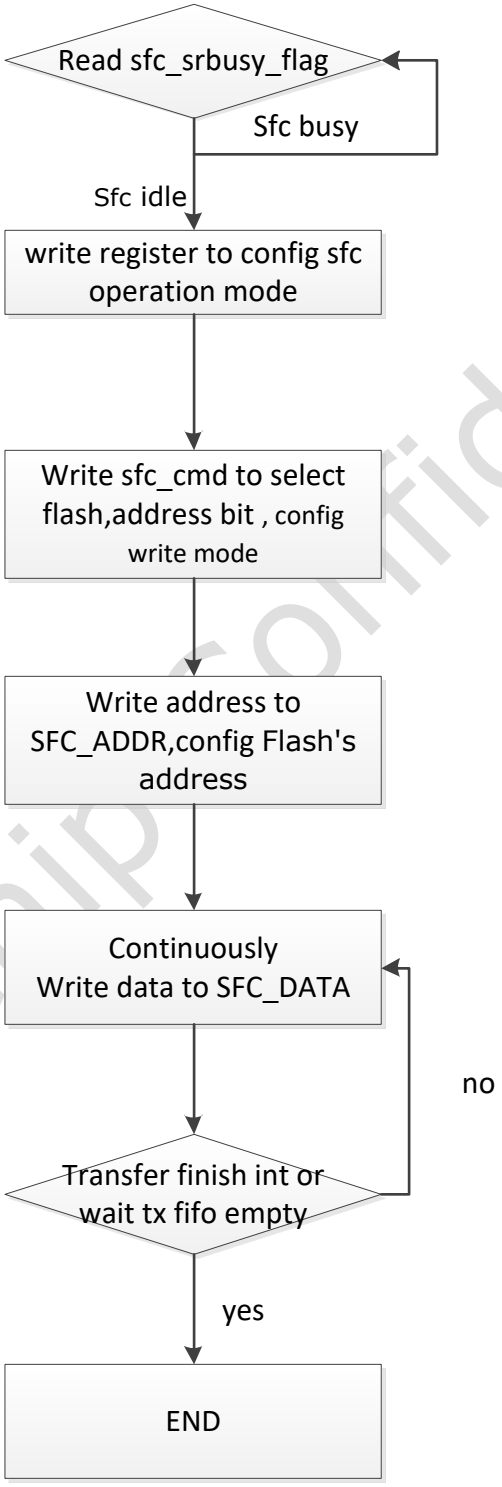


Fig. 27-4 SFC write flash flow

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27.6.2 AHB Slave read flash flow

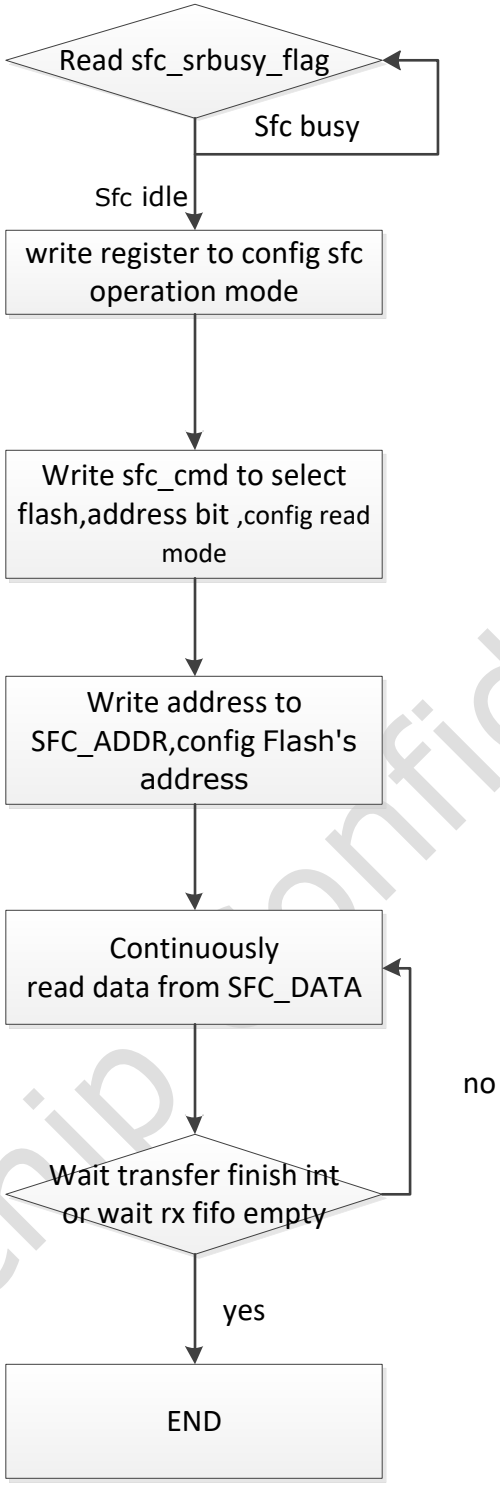


Fig. 27-5 SFC read flash flow

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