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Part2

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Chapter 1 Interconnect

1.1 Overview

The chip-level interconnect consists of main interconnect. It enables communication among the modules and subsystems in the device.
The main interconnect supports the following features:

- Cross-bar exchange network
- A special internal slave for accessing the configuration register
- Little-endian platform
- Embedded memory scheduler for DDR transaction generation
- QoS management for optimizing the transaction flow
- Transaction statistics for analyzing the transaction flow
- Security protection mechanism to compatible with the TrustZone technology

1.2 Block Diagram

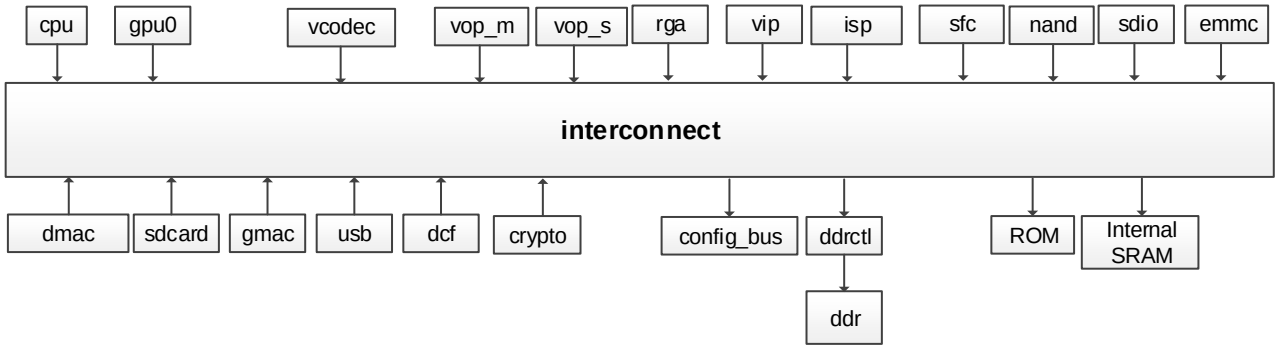


Fig. 1-1 Interconnect diagram

1.3 Function Description

1.3.1 QoS management

The main interconnect is connected with all the related IPs of the system, the interface between the IP and the interconnect is called as NIU(native interface unit).
The interconnect offers 4 modes of qos management:

- None, QoSGenerator is disabled, and priority information are stuck at 0.
- Fixed, QoSGenerator drives apply a fixed urgency to read transactions, and a (possibly different) urgency to write transactions.
- Limiter, QoSGenerator behaves as in fixed mode, but limits the traffic bandwidth coming from that socket, possibly stalling requests if the initiator attempts to exceed its budget.
- Regulator, QoSGenerator promotes are demotes hurry, depending the bandwidth obtained by the initiator is below or beyond a bandwidth budget. As transactions exceeding the bandwidth limit are sent (even though demoted), the regulator mode may be considered as a softer version of the limiter mode.

Limiter Behavior
When configured in bandwidth limiter, the unit uses a 23 bit counter to measure the average bandwidth. This counter has a 1/256 byte resolution and works as follows:

- Adds the number of byte rounded up to 16 (1 -> 16) and then multiplied by 256 to the current value, each time a request is sent.
- Subtracts the Bandwidth register value every cycle. If the Counter becomes negative, force it to 0.
- If the Counter value is greater than the Saturation register value multiplied by 16*256, any incoming request is stalled until this condition disappears. Note that the Counter cannot wrap-around because the maximum value it can reach is: SaturationMax*16*256 + BurstMax*256 = 1023*4K+4K*256 = 5116K or 223 = 8192K.

The following example will show the Counter behavior: 32 byte bursts, F=400MHz,

BW=200MB/s, T=0.32us. The Bandwidth register will be set to 256*200/400 = 128, and the Saturation register to 128*0.32*400/4096 = 4 (which corresponds to 64 bytes).

Regulator Behavior

When configured in bandwidth regulator, the unit uses a 23 bit counter to measure the average bandwidth. This counter has a 1/256 byte resolution and works as follows:

- Adds the number of byte rounded up to 16 and then multiplied by 256 to the current value, each time a response is received. If the result is greater than the Saturation register value multiplied by 16*256, saturation to this value is applied.
- Subtracts the Bandwidth register value every cycle. If the Counter becomes negative, force it to 0.
- If the Counter value is less than or equal to the Saturation register value multiplied by 16*256/2, the SocketMst Hurry signal will be set to the HurryHigh register, and HurryLow otherwise. Note that Urgency and Press will be also set to the same value.

The following example will show the Counter behavior: 1Kbyte bursts, F=500MHz, BW=2GB/s,T=2.048us. The Bandwidth register will be set to 256*2000/500 = 1024, and the Saturation register to 1024*2.048*500/4096 = 256 (which corresponds to 4 Kbytes).

QoS Generator Programming

Bandwidth: This log2 (socket.wData/8)+8 bits register defines the bandwidth in 1/256th byte per cycle unit. This allows a 2 MByte/s resolution at 500MHz. When thebandwidth is given in MByte/s, the value of this register will be equal to 256*BWMB/s / FMHz.

Saturation: This 10 bits register defines the number of byte used for bandwidth measurement. It is expressed in 16bytes unit (up to 16 Kbyte). Usually the integration window is given in us or in cycle: the value of this register will beequal to Bandwidh*Tus*FMHz/(256*16)or Bandwidh*Ncycle/(256*16).

The QoS management for peri-interconnect and main-interconnect inside each interconnect is independent. When master in peri-interconnect access main-interconnect, the QoS will be propagated to main-interconnect according to QoS configuration for ‘perilpslv_nsp’ (perilp master, cci_m0 and debug access slave register), ‘perilp_nsp’(perilp master, cci_m0 and debug access data memory) and ‘perihp_nsp’(perihp master access data memory). The masters in main-interconnect does not access peri-interconnect.

The default setting of master NIUs are listing below:

Table 1-1 QoS Generator

Master NIU	Priority0/1	Register Base Address
cpu	2	0xff508000
gpu	1	0xff520000
isp_128m	3	0xff548000
isp_rd_m	3	0xff548080
isp_wr_m	3	0xff548100
isp_m1	3	0xff548180
vip_m	3	0xff548200
rga_rd_m	1	0xff550000
rga_wr_m	1	0xff550080
vop_m0	3	0xff550100
vop_m1	3	0xff550180
vpu_m	2	0xff558000
vpu_r128	2	0xff558080
dcf	1	0xff500000
dmac	1	0xff500080
crypto	1	0xff510000
gmac	1	0xff518000
emmc	1	0xff538000
nand	1	0xff538080
sdio	1	0xff538100
sfc	1	0xff538180
sdmmc	1	0xff52c000

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Master NIU	Priority0/1	Register Base Address
usb_host	1	0xff540000
usb_otg	1	0xff540080

Note:

- All master NIU QoS generator mode is 'Regulator', bandwidth is 500MB/s and saturation is 1024.
- The bandwidth must be calculated based on actual operating frequency.
- Refer to chapter 7.4 for detail register. All generators have the same register except the valid bits of 'Bandwidth' filed may be different.

1.3.2 Probe

The interconnect provides a service called probe to trace packet and compute traffic statics, There are totally 4 probes to monitor the memory schedule traffic statics and each can be programmed by their register. They are listed below.

Table 1-2 Probe

Probe Name	Monitor Path	Register Base Address
cpu_probe	cpu to memory schedule	0xff532000
gpu_probe	gpu to memory schedule	0xff532400
mmip_probe	multimedia master to memory schedule	0xff532800
peri_probe	peripheral master to memory schedule	0xff532c00

Refer to chapter 7.4 for detail register.

1.4 Register Description

1.4.1 QoS Registers Summary

Name	Offset	Size	Reset Value	Description
QOS_Id_CoreId	0x0000	W	0x0d867004	Core id
QOS_Id_RevisionId	0x0004	W	0x0001aa00	Revision id
QOS_Priority	0x0008	W	0x80000101	QoS prirority
QOS_Mode	0x000c	W	0x00000000	Qos mode seletion
QOS_Bandwidth	0x0010	W	0x0000018a	QoS bandwidth
QOS_Saturation	0x0014	W	0x00000040	QoS saturation
QOS_ExtControl	0x0018	W	0x00000000	Qos external control

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

1.4.2 QoS Detail Register Description

QOS_Id_CoreId

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:8	RO	0x0d8670	CoreChecksum Field containing a checksum of the parameters of the IP
7:0	RO	0x04	CoreTypeId Field identifying the type of IP

QOS_Id_RevisionId

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:0	RO	0x0001aa00	RevisionId Constant

QOS_Priority

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31	RO	0x1	Mark Backward compatibility marker when 0
30:10	RO	0x0	reserved
9:8	RW	0x1	P1 In Programmable or Bandwidth Limiter mode, the priority level for read transactions. In Bandwidth regulator mode, the priority level when the used throughput is below the threshold. In Bandwidth Regulator mode, P1 should have a value equal or greater than P0
7:2	RO	0x0	reserved
1:0	RW	0x1	P0 In Programmable or Bandwidth Limiter mode, the priority level for write transactions. In Bandwidth Regulator mode, the priority level when the used throughput is above the threshold. In Bandwidth Regulator mode, P0 should have a value equal or lower than P1

QOS_Mode

Address: Operational Base + offset (0x000c)

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1:0	RW	0x0	Mode 0 = Programmable mode: a programmed priority is assigned to each read or write, 1 = Bandwidth Limiter Mode: a hard limit restricts throughput, 2 = Bypass mode: (<See SoC-specific QoS generator documentation>), 3 = Bandwidth Regulator mode: priority decreases when throughput exceeds a threshold

QOS_Bandwidth

Address: Operational Base + offset (0x0010)

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Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0x18a	Bandwidth In Bandwidth Limiter or Bandwidth Regulator mode, the bandwidth threshold in units of 1/256th bytes per cycle. For example, 80 MBps on a 250 MHz interface is value 0x0052. The valid bits may be different for different master NIU

QOS_Saturation

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:10	RO	0x0	reserved
9:0	RW	0x040	Saturation In Bandwidth Limiter or Bandwidth Regulator mode, the maximum data count value, in units of 16 bytes. This determines the window of time over which bandwidth is measured. For example, to measure bandwidth within a 1000 cycle window on a 64-bit interface is value 0x1F4

QOS_ExtControl

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	SocketQosEn Register field SocketQosEn determines how priority levels are driven when QoS generators and socket interfaces alternatively drive the levels for Urgency, Pressure, and Hurry signals: When set to 0, the QoS generator drives the levels. When set to 1, internal signals Pressure and Hurry are driven by the greater of the two levels from the socket interface or the QoS generator

1.4.3 Memory Schedule Registers Summary

Name	Offset	Size	Reset Value	Description
MSCH_Id_CoreId	0x0000	W	0x00dc1b18	Core id
MSCH_Id_RevisionId	0x0004	W	0x0001aa00	Revision id
MSCH_DeviceConf	0x0008	W	0x00000000	Register DeviceConf stores selectors to the predefined list of DDR configurationto be programmed at initialization phase. The register has two fields, Rank0 andRank1
MSCH_DeviceSize	0x000c	W	0x00000000	Register DeviceSize is used to set the size of DDR ranks

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Name	Offset	Size	Reset Value	Description
MSCH_DdrTimingA0	0x0010	W	0x28140916	Register DdrTimingA(n) of timing register bank n stores timing settings used bymemory schedulers to compute bank and page states
MSCH_DdrTimingB0	0x0014	W	0x12040702	Register DdrTimingB(n) of timing register bank n stores timing settings used bymemory schedulers to compute penalties pertaining to bank and page states
MSCH_DdrTimingC0	0x0018	W	0x00000602	Register DdrTimingC(n) of timing register bank n:Stores timing settings used by memory schedulers to compute penaltiespertaining to DRAM commands.Is used to configure the clock of the register bank
MSCH_DevToDev0	0x001c	W	0x00002222	Register DevToDev(n) of timing register bank n contains supplementary timingpenalties that are incurred when changing data-bus ownership of up to fourdevices.The penalties are expressed in scheduler clock cycles
MSCH_DdrMode	0x0110	W	0x0000004c	Register DdrMode stores the controller behavior description
MSCH_Ddr4Timing	0x0114	W	0x00000000	Long timing for DDR4 Bank Group support
MSCH_AgingX0	0x1000	W	0x00000004	Aging threshold multiplicator
MSCH_Aging0	0x1040	W	0x00000000	AGING slice threshold for port 0
MSCH_Aging1	0x1044	W	0x00000000	AGING slice threshold for port 1
MSCH_Aging2	0x1048	W	0x00000000	AGING slice threshold for port 2
MSCH_Aging3	0x104c	W	0x00000000	AGING slice threshold for port 3

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*
Base address for memory schedule 0 is 0xffa84000 and for memory schedule 1 is 0xffa8c0000.

1.4.4 Memory schedule Detail Register Description

MSCH_Id_CoreId
Address: Operational Base + offset (0x0000)

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Bit	Attr	Reset Value	Description
31:8	RO	0x00dc1b	CoreChecksum Field containing a checksum of the parameters of the IP. For memory schedule 0 , this value is 0x00dc1b For memory schedule 1 , this value is 0xc2f11d
7:0	RO	0x18	CoreTypeId Field identifying the type of IP

MSCH_Id_RevisionId

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:0	RO	0x0001aa00	RevisionId Constant

MSCH_DeviceConf

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:14	RO	0x0	reserved
13:8	RW	0x00	Rank1 Rank1 selector of predefined ddrConf configuration
7:0	RW	0x00	Rank0 Rank0 selector of predefined ddrConf configuration

MSCH_DeviceSize

Address: Operational Base + offset (0x000c)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:8	RW	0x00	Rank1 Rank0 size.The granule size is 64MB
7:0	RW	0x00	Rank0 Rank0 size. The granule size is 64MB

MSCH_DdrTimingA0

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:24	RW	0x28	ReadLatency Maximun delay between a read request and the first data response
23:22	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
21:16	RW	0x14	WrToMiss Minimum number of scheduler clock cycles between the last DRAM Write command and a new Read or Write command in another page of the same bank. The field must be set to the following value, rounded to an integer number of scheduler clock cycles: (WL ×tCkD + tWR + tRP + tRCD) / tCkG
15:14	RO	0x0	reserved
13:8	RW	0x09	RdToMiss Minimum number of scheduler clock cycles between the last DRAM Read command and a new Read or Write command in another page of the same bank. The field must be set to the following value, rounded to an integer number of scheduler clock cycles: (tRTP + tRP + tRCD –BL ×tCkD / 2) / tCkG
7:6	RO	0x0	reserved
5:0	RW	0x16	ActToAct Minimum number of scheduler clock cycles between two consecutive DRAM Activate commands on the same bank. The field must be set to the following value, rounded to an integer number of scheduler clock cycles: tRC / tCkG

MSCH_DdrTimingB0

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RW	0x12	Faw Number of cycle of the FAW period. The field must be set to the following value, rounded to an integer number of scheduler clock cycles: tFAW / tCkG
23:20	RO	0x0	reserved
19:16	RW	0x4	Rrd Number of cycle between two consecutive Activate commands on different Banks of the same device. The field must be set to the following value, rounded to an integer number of scheduler clock cycles: tRRD / tCkG
15:13	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
12:8	RW	0x07	WrToRd Minimum number of scheduler clock cycles between the last DRAM Write command and a Read command. The field must be set to the following value, rounded to an integer of scheduler clock cycles: (WL ×tCkD + tWTR) / tCkG, for DDR2 and DDR3 memories. (WL ×tCkD + tWTR_S) / tCkG, for DDR4 memories.
7:5	RO	0x0	reserved
4:0	RW	0x02	RdToWr Minimum number of scheduler clock cycles between the last DRAM Read command and a Write command. The field must be set to the following value, rounded to an integer number of scheduler clock cycles: 2 ×tCkD / tCkG, for DDR2 memories. (RL –WL + 2) ×tCkD / tCKG, for DDR3 and DDR4 memories.

MSCH_DdrTimingC0

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:14	RO	0x0	reserved
13:8	RW	0x06	WrToMwr Number of scheduler clock cycles between the last write data to the first data of a masked write command on the same bank. This field must be set to 3xBurstPenalty, and must be set to zero for the other DRAM
7:4	RO	0x0	reserved
3:0	RW	0x2	BurstPenalty DRAM burst duration on the DRAM data bus in scheduler clock cycles. The field must be set to Nd /Ns, where: Nd is the number of DRAM cycles needed to process a DRAM burst of determined size, expressed in bytes. Ns is the minimum number of scheduler cycles to process a DRAM burst of the same size

MSCH_DevToDev0

Address: Operational Base + offset (0x001c)

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Bit	Attr	Reset Value	Description
31:15	RO	0x0	reserved
14:12	RW	0x2	BusWrToWr number of cycle between the last write data to a device and the first write data of another device. The field must be set according to the third-party DDR controller specification
11	RO	0x0	reserved
10:8	RW	0x2	BusWrToRd number of cycle between the last write data to a device and the first read data of another device. The field must be set according to the third-party DDR controller specification
7	RO	0x0	reserved
6:4	RW	0x2	BusRdToWr number of cycle between the last read data of a device and the first write data to another device. The field must be set according to the third-party DDR controller specification
3	RO	0x0	reserved
2:0	RW	0x2	BusRdToRd number of cycle between the last read data of a device and the first read data of another device. The field must be set according to the third-party DDR controller specification

MSCH_DdrMode

Address: Operational Base + offset (0x0110)

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:16	RO	0x00	ForceOrderState ForceOrderState
15:8	RW	0x00	ForceOrder When bit n of register field ForceOrder is set to 1, DRAM commands are executed in the order they arrive at scheduler port n. When field bits are set to 1, and BypassFiltering is also set to 1, command execution order is guaranteed for the corresponding scheduler port
7	RO	0x0	reserved
6:5	RW	0x2	reserved

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Bit	Attr	Reset Value	Description
4:3	RW	0x1	BurstSize Register field BurstSize sets the DDR burst size, in bytes, as shown by the following table. 2'b00:16 2'b01:32 2'b10:64 2'b11:128
2	RW	0x1	FawBank Register field FawBank indicates the number of banks of a given device involved in the FAW period during which four banks can be active. It must be set to 0 for 2-bank memories, and 1 for memories with four banks or more
1	RW	0x0	BypassFiltering When register field BypassFiltering is set to 1, arbiter filters are bypassed and timing register outputs are internally set to an idle value.The field can be useful during DRAM initialization, when training or calibration sequences are performed, and scheduler arbitration is not needed. When the field is set to 0, scheduler arbitration is fully functional, this is the functional usage mode. NOTE: When the field is set to 1, the final arbitration level continues to elect transactions among those presented to the arbiter. Set field ForceOrder to ensure that transactions are executed in order, for instance during DRAM initialization
0	RW	0x0	AutoPrecharge When set to one, pages are automatically closed after each access, when set to zero, pages are left opened until an access in a different page occurs

MSCH_Ddr4Timing

Address: Operational Base + offset (0x0114)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
11:8	RW	0x0	RrdL Register field RrdL stores the minimum number of scheduler clock cycles on the DRAM command bus, between two Activate commands to different banks of the same bank group in the same device. The filed must be set to tRRD_L/tCkG
7:3	RW	0x00	WrToRdL Register field WrToRdL stores the result of nMin –tData, where nMin is the minimum number of scheduler clock cycles on the DRAM command bus in the interval between a Write command and the next Read command to an already opened page in the same bank group. The filed must be set to (WLxtCkD+tWTR_L)/tCkG
2:0	RW	0x0	CcdL Register field CcdL sets the minimum number of scheduler clock cycles between column access commands to an already opened page in the same bank group. The file must be set to: tCCD_L/tCkG

MSCH_AgingX0

Address: Operational Base + offset (0x1000)

Bit	Attr	Reset Value	Description
31:3	RO	0x0	reserved
2:0	RW	0x4	AgingX0 Aging threshold multiplicator

MSCH_Aging0

Address: Operational Base + offset (0x1040)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x00	Aging0 AGING slice threshold for port 0

MSCH_Aging1

Address: Operational Base + offset (0x1044)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x00	Aging1 AGING slice threshold for port 1

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MSCH_Aging2

Address: Operational Base + offset (0x1048)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x00	Aging2 AGING slice threshold for port 2

MSCH_Aging3

Address: Operational Base + offset (0x104c)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x00	Aging3 AGING slice threshold for port 3

1.4.5 Probe Registers Summary

Name	Offset	Size	Reset Value	Description
PROBE_Id_CoreId	0x0000	W	0x0d867006	Core id
PROBE_Id_RevisionId	0x0004	W	0x0001aa00	Revision id
PROBE_MainCtl	0x0008	W	0x00000000	Register MainCtl contains probe global control bits
PROBE_CfgCtl	0x000c	W	0x00000000	Register CfgCtl contains global enable and active bits. The register, which mustbe used by software before changing certain packet probe global registers
PROBE_StatPeriod	0x0024	W	0x00000000	Statistics Period
PROBE_StatGo	0x0028	W	0x00000000	Statistics begin control
PROBE_Counters_0_Src	0x0138	W	0x00000000	Register CntSrc indicates the event source used to increment the counter. Unassigned values (non-existing Press level or ExtEvent index, or unimplemented Filter) are equivalent to OFF
PROBE_Counters_0_Val	0x0140	W	0x00000000	Registers Counters_M_Val contain the statistics counter values
PROBE_Counters_1_Src	0x014c	W	0x00000000	Register CntSrc indicates the event source used to increment the counter. Unassigned values (non-existing Press level or ExtEvent index, or unimplemented Filter) are equivalent to OFF

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Name	Offset	Size	Reset Value	Description
PROBE_Counters_1_Val	0x0154	W	0x00000000	Registers Counters_M_Val contain the statistics counter values
PROBE_Counters_2_Src	0x0160	W	0x00000000	Register CntSrc indicates the event source used to increment the counter. Unassigned values (non-existing Press level or ExtEvent index, or unimplemented Filter) are equivalent to OFF
PROBE_Counters_2_Val	0x0168	W	0x00000000	Registers Counters_M_Val contain the statistics counter values
PROBE_Counters_3_Src	0x0174	W	0x00000000	Register CntSrc indicates the event source used to increment the counter. Unassigned values (non-existing Press level or ExtEvent index, or unimplemented Filter) are equivalent to OFF
PROBE_Counters_3_Val	0x017c	W	0x00000000	Registers Counters_M_Val contain the statistics counter values

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

1.4.6 Probe Detail Register Description

PROBE_Id_CoreId

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:8	RO	0x0d8670	CoreChecksum Field containing a checksum of the parameters of the IP
7:0	RO	0x06	CoreTypeId Field identifying the type of IP

PROBE_Id_RevisionId

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:0	RO	0x0001aa00	RevisionId Constant

PROBE_MainCtl

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
7	RW	0x0	FiltByteAlwaysChainableEn When set to 0, filters are mapped to all statistic counters when counting bytes or enabled bytes. Therefore, only filter events mapped to even counters can be counted using a pair of chained counters.When set to 1, filters are mapped only to even statistic counters when counting bytes or enabled bytes. Thus events from any filter can be counted using a pair of chained counters
6	RO	0x0	IntrusiveMode When set to 1, register field IntrusiveMode enables trace operation in Intrusive flow-control mode. When set to 0, the register enables trace operation in Overflow flow-control mode
5	RW	0x0	StatCondDump When set, register field StatCondDump enables the dump of a statistics frame to the range of counter values set for registers StatAlarmMin, StatAlarmMax, and AlarmMode. This field also renders register StatAlarmStatus inoperative. When parameter statisticsCounterAlarm is set to False, the StatCondDump register bit is reserved
4	RW	0x0	AlarmEn When set, register field AlarmEn enables the probe to collect alarm-related information. When the register field bit is null, both TraceAlarm and StatAlarm outputs are driven to 0
3	RW	0x0	StatEn When set to 1, register field StatEn enables statistics profiling. The probe sendS statistics results to the output for signal ObsTx. All statistics counters are cleared when the StatEn bit goes from 0 to 1. When set to 0, counters are disabled
2	RW	0x0	PayloadEn Register field PayloadEn, when set to 1, enables traces to contain headers and payload. When set ot 0, only headers are reported
1	RO	0x0	TraceEn Register field TraceEn enables the probe to send filtered packets (Trace) on the ObsTx observation output
0	RW	0x0	ErrEn Register field ErrEn enables the probe to send on the ObsTx output any packet with Error status, independently of filtering mechanisms, thus constituting a simple supplementary global filter

PROBE_CfgCtl

Address: Operational Base + offset (0x000c)

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved

Bit	Attr	Reset Value	Description
1	RO	0x0	Active Register field Active is used to inform software that the probe is active. Probe configuration is not allowed during the active state. This bit is raised when bit GlobalEn is set, and is cleared a few cycles after setting GlobalEn to zero (probe is Idle)
0	RW	0x0	GlobalEn Set register field GlobalEn to 1 enable the tracing and statistics collection sub-systems of the packet probe

PROBE_StatPeriod

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4:0	RW	0x00	StatPeriod Register StatPeriod is a 5-bit register that sets a period, within a range of 2 cycles to 2 gigacycles, during which statistics are collected before being dumped automatically. Setting the register implicitly enables automatic mode operation for statistics collection. The period is calculated with the formula: N_Cycle = 2**StatPeriodWhen register StatPeriod is set to its default value 0, automatic dump mode is disabled, and register StatGo is activated for manual mode operation. Note: When parameter statisticsCollection is set to False, StatPeriod is reserved

PROBE_StatGo

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	StatGo Writing a 1 to the 1-bit pulse register StatGo generates a statistics dump.The register is active when statistics collection operates in manual mode, that is, when register StatPeriod is set to 0.NOTE The written value is not stored in StatGo. A read always returns 0

PROBE_Counters_0_Src

Address: Operational Base + offset (0x0138)

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
4:0	RW	0x00	IntEvent Internal packet event 5'h00 OFF Counter disabled. 5'h01 CYCLE8 Probe clock cycles. 5'h02 IDLE Idle cycles during which no packet data is observed. 5'h03 XFER Transfer cycles during which packet data is transferred. 5'h04 BUSY Busy cycles during which the packet data is made available by the transmitting agent but the receiving agent is not ready to receive it. 5'h05 WAIT Wait cycles during a packet in which the transmitting agent suspends the transfer of packet data. 5'h06 PKT Packets. 5'h08 BYTE Total number of payload bytes. 5'h09 PRESS Clock cycles with pressure level > 0. 5'h0A PRESS Clock cycles with pressure level > 1. 5'h0B PRESS Clock cycles with pressure level > 2. 5'h10 CHAIN Carry from counter 2m to counter 2m + 1

PROBE_Counters_0_Val

Address: Operational Base + offset (0x0140)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RO	0x0000	Counters_0_Val Register Val is a read-only register that is always present. The register containsthe statistics counter value either pending StatAlarm output, or when statisticscollection is suspended subsequent to triggers or signal statSuspend

PROBE_Counters_1_Src

Address: Operational Base + offset (0x014c)

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
4:0	RW	0x00	IntEvent Internal packet event Event | source type | Event description 5'h00 OFF Counter disabled. 5'h01 CYCLE8 Probe clock cycles. 5'h02 IDLE Idle cycles during which no packet data is observed. 5'h03 XFER Transfer cycles during which packet data is transferred. 5'h04 BUSY Busy cycles during which the packet data is made available by the transmitting agent but the receiving agent is not ready to receive it. 5'h05 WAIT Wait cycles during a packet in which the transmitting agent suspends the transfer of packet data. 5'h06 PKT Packets. 5'h08 BYTE Total number of payload bytes. 5'h09 PRESS Clock cycles with pressure level > 0. 5'h0A PRESS Clock cycles with pressure level > 1. 5'h0B PRESS Clock cycles with pressure level > 2. 5'h10 CHAIN Carry from counter 2m to counter 2m + 1

PROBE_Counters_1_Val

Address: Operational Base + offset (0x0154)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RO	0x0000	Counters_0_Val Register Val is a read-only register that is always present. The register containsthe statistics counter value either pending StatAlarm output, or when statisticscollection is suspended subsequent to triggers or signal statSuspend

PROBE_Counters_2_Src

Address: Operational Base + offset (0x0160)

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
4:0	RW	0x00	IntEvent Internal packet event Event | source type | Event description 5'h00 OFF Counter disabled. 5'h01 CYCLE8 Probe clock cycles. 5'h02 IDLE Idle cycles during which no packet data is observed. 5'h03 XFER Transfer cycles during which packet data is transferred. 5'h04 BUSY Busy cycles during which the packet data is made available by the transmitting agent but the receiving agent is not ready to receive it. 5'h05 WAIT Wait cycles during a packet in which the transmitting agent suspends the transfer of packet data. 5'h06 PKT Packets. 5'h08 BYTE Total number of payload bytes. 5'h09 PRESS Clock cycles with pressure level > 0. 5'h0A PRESS Clock cycles with pressure level > 1. 5'h0B PRESS Clock cycles with pressure level > 2. 5'h10 CHAIN Carry from counter 2m to counter 2m + 1

PROBE_Counters_2_Val

Address: Operational Base + offset (0x0168)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RO	0x0000	Counters_0_Val Register Val is a read-only register that is always present. The register containsthe statistics counter value either pending StatAlarm output, or when statisticscollection is suspended subsequent to triggers or signal statSuspend

PROBE_Counters_3_Src

Address: Operational Base + offset (0x0174)

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
4:0	RW	0x00	IntEvent Internal packet event Event | source type | Event description 5'h00 OFF Counter disabled. 5'h01 CYCLE8 Probe clock cycles. 5'h02 IDLE Idle cycles during which no packet data is observed. 5'h03 XFER Transfer cycles during which packet data is transferred. 5'h04 BUSY Busy cycles during which the packet data is made available by the transmitting agent but the receiving agent is not ready to receive it. 5'h05 WAIT Wait cycles during a packet in which the transmitting agent suspends the transfer of packet data. 5'h06 PKT Packets. 5'h08 BYTE Total number of payload bytes. 5'h09 PRESS Clock cycles with pressure level > 0. 5'h0A PRESS Clock cycles with pressure level > 1. 5'h0B PRESS Clock cycles with pressure level > 2. 5'h10 CHAIN Carry from counter 2m to counter 2m + 1

PROBE_Counters_3_Val

Address: Operational Base + offset (0x017c)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RO	0x0000	Counters_0_Val Register Val is a read-only register that is always present. The register containsthe statistics counter value either pending StatAlarm output, or when statisticscollection is suspended subsequent to triggers or signal statSuspend

1.5 Application Notes

1.5.1 QoS setting

The VOP and isp have the external QoS control.
It's recommended that field 0 of QoS. ExtControl set to 1 to enable the external qos control. And priority setting of each master kept at 1.

1.5.2 Idle request

The main interconnect supports flushing the ongoing transaction when the software needed to do so.
If the GPU power domain need to disconnect from the main interconnect, Idle request has to be sent to GPU NIU, the NIU will respond a ack, and when it's ready to be disconnect, one Idle signal will be send out . Then, if GPU still have transaction to be sent to the memory scheduler, it will be stalled by the NIU.
If the GPU system power domain is disconnected as the above flow, then CPU want to access

to the GPU system, it will response error or held to CPU according to the corresponding grf register setting.

The sequence is like following figure shows:

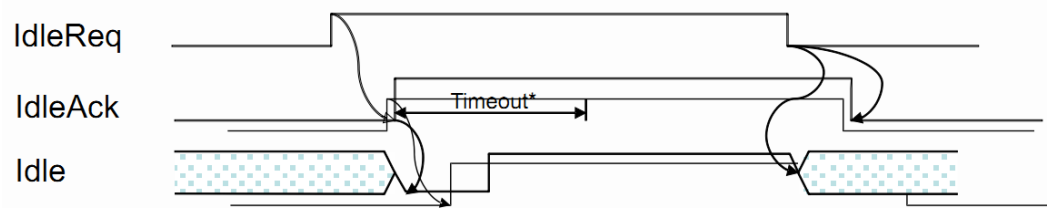


Fig. 7-2 Idle request

The idle request is set by GRF register.

1.5.3 Basic Packet Tracing

To trace packets, the packet probe must be programmed as follows:

- Select the interesting probe listed in section 7.3.4.
- Set field *TraceEn* of register *MainCtl* to 1 to enable forwarding of traced packets to the connected observer. Optionally set field *PayloadEn* of register *MainCtl* to 1 if the packet payload should be included in the trace.
- Set field *GlobalEn* of register *CfgCtl* to 1.

1.5.4 Counting packets over a fixed period

The following programming sequence counts packets at a given probe point using statistic counter 0.

- Select the interesting probe listed in section 7.3.4
- Set field *StatEn* to 1 in register *MainCtl*.
- Set register *Counters_0_Src* to 0x6 (PKT)to count packets.
- Specify the period during which the packets should be counted by setting register StatPeriod to: $\log_2$(interval expressed in number of probe clock cycles)
- Set field *GlobalEn* of register *CfgCtl* to 1 to enable packet counting.

Once time $2^{StatPeriod}$ has elapsed, the number of packets counted is dumped to the observer and can be read from *Counters_0_Val*.

1.5.5 Measuring bandwidth

The following programming sequence example shows how a packet probe can be used to measure bandwidth at a probe point.

Some important points to note about this example are:

- Statistics counters are chained together to support the maximum theoretical bandwidth. Counter 0 is configured to count bytes; counter 1 increments when counter 0 rolls over.
- The counter values are dumped to an observer after time $2^{StatPeriod}$.

The programming sequence is as follows:

- Select the interesting probe listed in section 7.3.4
- Set register *Counters_0_Src* to 0x8 (BYTES) to count bytes.
- Set register *Counters_1_Src* to 0x10 (CHAIN) to increment when counter 0 wraps.
- Specify the period during which the bytes should be counted by setting register *StatPeriod* to: $\log_2$(interval expressed in number of probe clock cycles).
- Set field *GlobalEn* of register *CfgCtl* to 1 to enable the counting of bytes.

Once time $2^{StatPeriod}$ has elapsed, the number of packets counted is dumped to the observer and can be read from *Counters_0_Val* and *Counters_0_Val*.

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Chapter 2 Dynamic Memory Interface (DMC)

2.1 Overview

The DMC includes DDR protocol controller (PCTL) and DDR PHY which are a complete memory interface solution for DDR memory subsystems.
The PCTL SoC application bus interface supports AXI interface, with a flexible address mapper logic allow application-specific mapping of row, column, bank, bank group and rank bits to achieve industry leading high-efficiency, low-latency and high-performance from memory interface.
The DDR PHY provides control features to ease the customer implementation of digitally controlled features of the PHY such as initialization, DQS gate training, write leveling training and programmable configuration controls.
The DMC supports the following features:

- Support DDR3/DDR3L/DDR4/LPDDR2/LPDDR3
- Support up to 2 ranks and up to 4GB capacity
- Support 32-bit, 16-bit and 8-bit DDR data bus width
- Support up to 14-type address mapping
- Support up to 32-bank (including bank group)
- Support DDR burst8 only
- Support different CL/WL latency
- Support DDR3/DDR3L/DDR4/LPDDR2/LPDDR3 SW frequency change
- Support DDR4 DBI, PDA
- Support auto gated clock through DDRC and AXI low power interface
- Support auto put DDR PHY entry or exit self-refresh by DFI lower power interface
- Support auto or SW issue entry or exit clock stop/power-down/self-refresh/deep power-down/max power saving mode
- Support SW or PMU auto let DDR PHY entry or exit retention/self-refresh
- Support open, close, intelligent pre-charge paging policy
- Support Advance refresh control
- Support APB interface for PCTL and PHY software-accessible registers
- Support automatic DQS gate training and automatic write leveling training
- Support TX DLL and RX DLL adjustment

2.2 Block Diagram

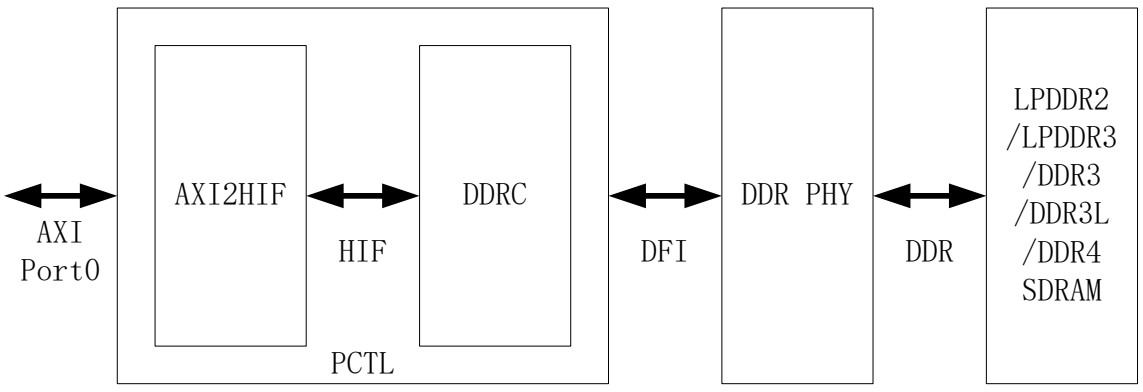


Fig. 2-1DMC Block Diagram

2.3 Function Description

2.3.1 PCTL

PCTL supports only one AXI Port0, it receives AXI transactions from memory schedule of

interconnect. These transactions are queued internally and scheduled for access in order to the SDRAM while satisfying SDRAM protocol timing requirements. It in turn issues commands on the DFI interface to the DDR PHY block which launches and captures data to and from the SDRAM. PCTL contains the following main components:

- AXI2HIF block: This block provides the AXI interface to system level and HIF interface to DDRC block. It provides bus protocol handing, data buffering, data bus size conversion and memory burst alignment. Read is stored in a SRAM, read re-order buffer and return in order to the AXI Port.
- DDRC block: This block issues the read/write commands in order, carries out the DRAM page management, issues DRAM maintenance commands, and implement the DFI interface. Write data is stored in an SRAM until its associated command is issued to the PHY. Read data is handled by the response engine in the DDRC and is returned in order on the HIF.

2.3.2 DDR PHY

DDR PHY supports DDR3/DDR3L/DDR4/LPDDR2/LPDDR3 SDRAM and provides turnkey physical interface solutions for ICs requiring access to JEDEC compatible SDRAM devices. It is optimized for low power and high speed (up to 1066Mbps for LPDDR2 and up to 1600Mbps for DDR3/DDR3L/LPDDR3/DDR4) applications with robust timing and small silicon area in 28nm process. It supports all JEDEC DDR3/DDR3L/DDR4/LPDDR2/LPDDR3 SDRAM components in the market. The PHY components contain DDR specialized functional and utility SSTL and HSUL I/Os up to 1600MHz in 28nm, critical timing synchronization module (TSM) and a low power/jitter DLLs with programmable fine-grain control for any SDRAM interface.

2.4 Register Description

Slave address can be divided into different length for different usage, which is shown as follows.

2.4.1 Registers Summary

Name	Offset	Size	Reset Value	Description
DDRC_MSTR	0x0000	W	0x03040001	Master Register 0
DDRC_STAT	0x0004	W	0x00000000	Operating Mode Status Register
DDRC_MRCTRL0	0x0010	W	0x00000000	Mode Register Read/Write Control Register 0
DDRC_MRCTRL1	0x0014	W	0x00000000	Mode Register Read/Write Control Register 1
DDRC_MRSTAT	0x0018	W	0x00000000	Mode Retgister Read/Write Status Register
DDRC_MRCTRL2	0x001c	W	0x00000000	Mode Register Read/Write Control Register 2
DDRC_DERATEEN	0x0020	W	0x00000000	Temperature Derate Enable Register
DDRC_DERATEINT	0x0024	W	0x00800000	Temperature Derate Interval Registesr
DDRC_PWRCTL	0x0030	W	0x00000000	Lower Power Control Register
DDRC_PWRTMG	0x0034	W	0x00402010	Lower Power Timing Register

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Name	Offset	Size	Reset Value	Description
DDRC_HWLPCTL	0x0038	W	0x00000003	Hardware Lower Power Control Register
DDRC_HWFFCCTL	0x003c	W	0x00000010	Hardware Fast Frequency Change Control Register
DDRC_HWFFCSTAT	0x0040	W	0x00000000	Hardware Fast Frequency Change Status Register
DDRC_RFSHCTL0	0x0050	W	0x00210000	Refresh Control Register
DDRC_RFSHCTL1	0x0054	W	0x00000000	Refresh Control Register 1
DDRC_RFSHCTL3	0x0060	W	0x00000000	Refresh Control Register 3
DDRC_RFSHTMG	0x0064	W	0x0062008c	Refresh Timing Register
DDRC_CRCPARCTL0	0x00c0	W	0x00000000	CRC Parity Control Register 0
DDRC_CRCPARCTL1	0x00c4	W	0x00001000	CRC Parity Control Register 1
DDRC_CRCPARSTAT	0x00cc	W	0x00000000	CRC Parity Status Register
DDRC_INIT0	0x00d0	W	0x0002004e	SDRAM Initilization Register 0
DDRC_INIT1	0x00d4	W	0x00000000	SDRAM Initialization Register 1
DDRC_INIT2	0x00d8	W	0x00000d05	SDRAM Initialization Register 2
DDRC_INIT3	0x00dc	W	0x00000510	SDRAM Initialization Register 3
DDRC_INIT4	0x00e0	W	0x00000000	SDRAM Initialization Register 4
DDRC_INIT5	0x00e4	W	0x00100004	SDRAM Initialization Register 5
DDRC_INIT6	0x00e8	W	0x00000000	SDRAM Initialization Register 6
DDRC_INIT7	0x00ec	W	0x00000000	SDRAM Initialization Register 7
DDRC_DIMMCTL	0x00f0	W	0x00000000	DIMM Control Register
DDRC_RANKCTL	0x00f4	W	0x0000066f	Rank Control Register
DDRC_DRAMTMG0	0x0100	W	0x0f101b0f	SDRAM Timing Register 0
DDRC_DRAMTMG1	0x0104	W	0x00080414	SDRAM Timing Register 1
DDRC_DRAMTMG2	0x0108	W	0x0305060d	SDRAM Timing Register 2
DDRC_DRAMTMG3	0x010c	W	0x0050400c	SDRAM Timing Register 3
DDRC_DRAMTMG4	0x0110	W	0x05040405	SDRAM Timing Register 4
DDRC_DRAMTMG5	0x0114	W	0x05050403	SDRAM Timing Register 5
DDRC_DRAMTMG6	0x0118	W	0x02020005	SDRAM Timing Register 6
DDRC_DRAMTMG7	0x011c	W	0x00000202	SDRAM Timing Register 7
DDRC_DRAMTMG8	0x0120	W	0x03034405	SDRAM Timing Register 8
DDRC_DRAMTMG9	0x0124	W	0x0004040d	SDRAM Timing Register 9

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Name	Offset	Size	Reset Value	Description
DDRC_DRAMTMG10	0x0128	W	0x001c180a	SDRAM Timing Register 10
DDRC_DRAMTMG11	0x012c	W	0x440c021c	SDRAM Timing Register 11
DDRC_DRAMTMG12	0x0130	W	0x00020010	SDRAM Timing Register 12
DDRC_DRAMTMG13	0x0134	W	0x1c200004	SDRAM Timing Register 13
DDRC_DRAMTMG14	0x0138	W	0x000000a0	SDRAM Timing Register 14
DDRC_DRAMTMG15	0x013c	W	0x00000000	SDRAM Timing Register 15
DDRC_DRAMTMG17	0x0144	W	0x00000000	SDRAM Timing Register 17
DDRC_ZQCTL0	0x0180	W	0x02000040	ZQ Control Register 0
DDRC_ZQCTL1	0x0184	W	0x02000100	ZQ Control Register 1
DDRC_ZQCTL2	0x0188	W	0x00000000	ZQ Control Register 2
DDRC_ZQSTAT	0x018c	W	0x00000000	ZQ Status Register
DDRC_DFITMG0	0x0190	W	0x07020002	DFI Timing Register 0
DDRC_DFITMG1	0x0194	W	0x00000404	DFI Timing Register 1
DDRC_DFILPCFG0	0x0198	W	0x07000000	DFI Lower Power Configuration Register 0
DDRC_DFILPCFG1	0x019c	W	0x00000000	DFI Lower Power Configuration Register 1
DDRC_DFIUPD0	0x01a0	W	0x00400003	DFI Update Register 0
DDRC_DFIUPD1	0x01a4	W	0x00000001	DFI Update Register 1
DDRC_DFIUPD2	0x01a8	W	0x00000001	DFI Update Register 2
DDRC_DFIMISC	0x01b0	W	0x00000001	DFI Miscellaneous Control Register
DDRC_DFITMG2	0x01b4	W	0x00000202	DFI Timing Register 2
DDRC_DFITMG3	0x01b8	W	0x00000000	DFI Timing Register 3
DDRC_DFISTAT	0x01bc	W	0x00000000	DFI Status Register
DDRC_DBICTL	0x01c0	W	0x00000001	DM/DBI Control Register
DDRC_DFIPHYMSTR	0x01c4	W	0x00000001	DFI PHY Master
DDRC_ADDRMAP0	0x0200	W	0x00000000	Address Map Register 0
DDRC_ADDRMAP1	0x0204	W	0x00000000	Address Map Register 1
DDRC_ADDRMAP2	0x0208	W	0x00000000	Address Map Register 2
DDRC_ADDRMAP3	0x020c	W	0x00000000	Address Map Register 3
DDRC_ADDRMAP4	0x0210	W	0x00000000	Address Map Register 4
DDRC_ADDRMAP5	0x0214	W	0x00000000	Address Map Register 5
DDRC_ADDRMAP6	0x0218	W	0x00000000	Address Map Register 6
DDRC_ADDRMAP7	0x021c	W	0x00000000	Address Map Register 7
DDRC_ADDRMAP8	0x0220	W	0x00000000	Address Map Register 8
DDRC_ADDRMAP9	0x0224	W	0x00000000	Address Map Register 9

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Name	Offset	Size	Reset Value	Description
DDRC_ADDRMAP10	0x0228	W	0x00000000	Address Map Register 10
DDRC_ADDRMAP11	0x022c	W	0x00000000	Address Map Register 11
DDRC_ODTCFG	0x0240	W	0x04000400	ODT Configuration Register
DDRC_ODTMAP	0x0244	W	0x00002211	ODT/Rank Map Register
DDRC_SCHED	0x0250	W	0x00000804	Scheduler Control Register
DDRC_SCHED1	0x0254	W	0x00000000	Scheduler Control Register 1
DDRC_PERFLPR1	0x0264	W	0x0f00007f	Low Priority Read CAM Register 1
DDRC_PERFWR1	0x026c	W	0x0f00007f	Write CAM Register 1
DDRC_DBG0	0x0300	W	0x00000000	Debug Register 0
DDRC_DBG1	0x0304	W	0x00000000	Debug Register 1
DDRC_DBGCAM	0x0308	W	0x00000000	CAM Debug Register
DDRC_DBGCMD	0x030c	W	0x00000000	Command Debug Register
DDRC_DBGSTAT	0x0310	W	0x00000000	Status Debug Register
DDRC_SWCTL	0x0320	W	0x00000001	Software Register Programming Control Enable
DDRC_SWSTAT	0x0324	W	0x00000001	Software Register Programming Control Status
DDRC_POISONCFG	0x036c	W	0x00110011	AXI Poison Configuration Register
DDRC_POISONSTAT	0x0370	W	0x00000000	AXI Poison Status Register
DDRC_PSTAT	0x03fc	W	0x00000000	Port Status Register
DDRC_PCCFG	0x0400	W	0x00000000	Port Common Configuration Register
DDRC_PCFGR_0	0x0404	W	0x00000000	Port 0 Configuration Read Register
DDRC_PCFGW_0	0x0408	W	0x00004000	Port 0 Configuration Write Register
DDRC_PCTRL_0	0x0490	W	0x00000000	Port 0 Control Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

Name	Offset	Size	Reset Value	Description
DDRPHY_REG0	0x0000	W	0x000000ff	DDR PHY register 00
DDRPHY_REG1	0x0004	W	0x00000008	DDR PHY register 01
DDRPHY_REG2	0x0008	W	0x00000000	DDR PHY register 02
DDRPHY_REG3	0x000c	W	0x00000022	DDR PHY register 03
DDRPHY_REG4	0x0010	W	0x00000022	DDR PHY register 04
DDRPHY_REG5	0x0014	W	0x00000000	DDR PHY register 05
DDRPHY_REG6	0x0018	W	0x00000002	DDR PHY register 06
DDRPHY_REG9	0x0024	W	0x00000000	DDR PHY register 09

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Name	Offset	Size	Reset Value	Description
DDRPHY_REGA	0x0028	W	0x00000000	DDR PHY register 0A
DDRPHY_REGB	0x002c	W	0x00000000	DDR PHY register 0B
DDRPHY_REGC	0x0030	W	0x00000000	DDR PHY register 0C
DDRPHY_REG11	0x0044	W	0x00000014	DDR PHY register 11
DDRPHY_REG12	0x0048	W	0x000000a2	DDR PHY register 12
DDRPHY_REG13	0x004c	W	0x0000000c	DDR PHY register 13
DDRPHY_REG14	0x0050	W	0x00000008	DDR PHY register 14
DDRPHY_REG15	0x0054	W	0x00000020	DDR PHY register 15
DDRPHY_REG16	0x0058	W	0x00000014	DDR PHY register 16
DDRPHY_REG17	0x005c	W	0x00000044	DDR PHY register 17
DDRPHY_REG18	0x0060	W	0x00000014	DDR PHY register 18
DDRPHY_REG1B	0x006c	W	0x00000000	DDR PHY register 1B
DDRPHY_REG1F	0x007c	W	0x00000030	DDR PHY register 1F
DDRPHY_REG20	0x0080	W	0x00000014	DDR PHY register 20
DDRPHY_REG21	0x0084	W	0x00000004	DDR PHY register 21
DDRPHY_REG22	0x0088	W	0x00000002	DDR PHY register 22
DDRPHY_REG26	0x0098	W	0x0000000c	DDR PHY register 26
DDRPHY_REG27	0x009c	W	0x00000000	DDR PHY register 27
DDRPHY_REG28	0x00a0	W	0x00000001	DDR PHY register 28
DDRPHY_REG29	0x00a4	W	0x00000002	DDR PHY register 29
DDRPHY_REG2B	0x00ac	W	0x00000081	DDR PHY register 2B
DDRPHY_REG2C	0x00b0	W	0x00000000	DDR PHY register 2C
DDRPHY_REG2D	0x00b4	W	0x00000000	DDR PHY register 2D
DDRPHY_REG2E	0x00b8	W	0x00000004	DDR PHY register 2E
DDRPHY_REG2F	0x00bc	W	0x00000014	DDR PHY register 2F
DDRPHY_REG30	0x00c0	W	0x00000014	DDR PHY register 30
DDRPHY_REG31	0x00c4	W	0x00000004	DDR PHY register 31
DDRPHY_REG32	0x00c8	W	0x00000002	DDR PHY register 32
DDRPHY_REG36	0x00d8	W	0x00000004	DDR PHY register 36
DDRPHY_REG37	0x00dc	W	0x00000000	DDR PHY register 37
DDRPHY_REG38	0x00e0	W	0x00000001	DDR PHY register 38
DDRPHY_REG39	0x00e4	W	0x00000002	DDR PHY register 39
DDRPHY_REG3A	0x00e8	W	0x00000001	DDR PHY register 3A
DDRPHY_REG3B	0x00ec	W	0x00000081	DDR PHY register 3B
DDRPHY_REG3C	0x00f0	W	0x00000000	DDR PHY register 3C
DDRPHY_REG3D	0x00f4	W	0x00000000	DDR PHY register 3D
DDRPHY_REG3E	0x00f8	W	0x00000004	DDR PHY register 3E
DDRPHY_REG3F	0x00fc	W	0x00000014	DDR PHY register 3F
DDRPHY_REG40	0x0100	W	0x00000014	DDR PHY register 40
DDRPHY_REG41	0x0104	W	0x00000004	DDR PHY register 41
DDRPHY_REG42	0x0108	W	0x00000002	DDR PHY register 42
DDRPHY_REG46	0x0118	W	0x0000000c	DDR PHY register 46
DDRPHY_REG47	0x011c	W	0x00000000	DDR PHY register 47

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Name	Offset	Size	Reset Value	Description
DDRPHY_REG48	0x0120	W	0x00000001	DDR PHY register 48
DDRPHY_REG49	0x0124	W	0x00000002	DDR PHY register 49
DDRPHY_REG4A	0x0128	W	0x00000001	DDR PHY register 4A
DDRPHY_REG4B	0x012c	W	0x00000091	DDR PHY register 4B
DDRPHY_REG4C	0x0130	W	0x00000000	DDR PHY register 4C
DDRPHY_REG4D	0x0134	W	0x00000000	DDR PHY register 4D
DDRPHY_REG4E	0x0138	W	0x00000004	DDR PHY register 4E
DDRPHY_REG4F	0x013c	W	0x00000014	DDR PHY register 4F
DDRPHY_REG50	0x0140	W	0x00000014	DDR PHY register 50
DDRPHY_REG51	0x0144	W	0x00000004	DDR PHY register 51
DDRPHY_REG52	0x0148	W	0x00000002	DDR PHY register 52
DDRPHY_REG56	0x0158	W	0x0000000c	DDR PHY register 56
DDRPHY_REG57	0x015c	W	0x00000000	DDR PHY register 57
DDRPHY_REG58	0x0160	W	0x00000001	DDR PHY register 58
DDRPHY_REG59	0x0164	W	0x00000002	DDR PHY register 59
DDRPHY_REG5A	0x0168	W	0x00000001	DDR PHY register 5A
DDRPHY_REG5B	0x016c	W	0x00000091	DDR PHY register 5B
DDRPHY_REG5C	0x0170	W	0x00000000	DDR PHY register 5C
DDRPHY_REG5D	0x0174	W	0x00000000	DDR PHY register 5D
DDRPHY_REG5E	0x0178	W	0x00000004	DDR PHY register 5E
DDRPHY_REG5F	0x017c	W	0x00000014	DDR PHY register 5F
DDRPHY_REG70	0x01c0	W	0x00000077	DDR PHY register 70
DDRPHY_REG71	0x01c4	W	0x00000077	DDR PHY register 71
DDRPHY_REG72	0x01c8	W	0x00000077	DDR PHY register 72
DDRPHY_REG73	0x01cc	W	0x00000077	DDR PHY register 73
DDRPHY_REG74	0x01d0	W	0x00000077	DDR PHY register 74
DDRPHY_REG75	0x01d4	W	0x00000077	DDR PHY register 75
DDRPHY_REG76	0x01d8	W	0x00000077	DDR PHY register 76
DDRPHY_REG77	0x01dc	W	0x00000077	DDR PHY register 77
DDRPHY_REG78	0x01e0	W	0x00000077	DDR PHY register 78
DDRPHY_REG79	0x01e4	W	0x00000077	DDR PHY register 79
DDRPHY_REG7A	0x01e8	W	0x00000007	DDR PHY register 7A
DDRPHY_REG7B	0x01ec	W	0x00000077	DDR PHY register 7B
DDRPHY_REG7C	0x01f0	W	0x00000077	DDR PHY register 7C
DDRPHY_REG7D	0x01f4	W	0x00000077	DDR PHY register 7D
DDRPHY_REG7E	0x01f8	W	0x00000077	DDR PHY register 7E
DDRPHY_REG7F	0x01fc	W	0x00000077	DDR PHY register 7F
DDRPHY_REG80	0x0200	W	0x00000077	DDR PHY register 80
DDRPHY_REG81	0x0204	W	0x00000077	DDR PHY register 81
DDRPHY_REG82	0x0208	W	0x00000077	DDR PHY register 82
DDRPHY_REG83	0x020c	W	0x00000077	DDR PHY register 83
DDRPHY_REG84	0x0210	W	0x00000077	DDR PHY register 84
DDRPHY_REG85	0x0214	W	0x00000007	DDR PHY register 85

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Name	Offset	Size	Reset Value	Description
DDRPHY_REG86	0x0218	W	0x00000077	DDR PHY register 86
DDRPHY_REG87	0x021c	W	0x00000077	DDR PHY register 87
DDRPHY_REG88	0x0220	W	0x00000077	DDR PHY register 88
DDRPHY_REG89	0x0224	W	0x00000077	DDR PHY register 89
DDRPHY_REG8A	0x0228	W	0x00000077	DDR PHY register 8A
DDRPHY_REG8B	0x022c	W	0x00000077	DDR PHY register 8B
DDRPHY_REG8C	0x0230	W	0x00000077	DDR PHY register 8C
DDRPHY_REG8D	0x0234	W	0x00000077	DDR PHY register 8D
DDRPHY_REG8E	0x0238	W	0x00000077	DDR PHY register 8E
DDRPHY_REG8F	0x023c	W	0x00000077	DDR PHY register 8F
DDRPHY_REG90	0x0240	W	0x00000007	DDR PHY register 90
DDRPHY_REG91	0x0244	W	0x00000077	DDR PHY register 91
DDRPHY_REG92	0x0248	W	0x00000077	DDR PHY register 92
DDRPHY_REG93	0x024c	W	0x00000077	DDR PHY register 93
DDRPHY_REG94	0x0250	W	0x00000077	DDR PHY register 94
DDRPHY_REG95	0x0254	W	0x00000077	DDR PHY register 95
DDRPHY_REG96	0x0258	W	0x00000077	DDR PHY register 96
DDRPHY_REG97	0x025c	W	0x00000077	DDR PHY register 97
DDRPHY_REG98	0x0260	W	0x00000077	DDR PHY register 98
DDRPHY_REG99	0x0264	W	0x00000077	DDR PHY register 99
DDRPHY_REG9A	0x0268	W	0x00000077	DDR PHY register 9A
DDRPHY_REG9B	0x026c	W	0x00000007	DDR PHY register 9B
DDRPHY_REGA3	0x028c	W	0x00000030	DDR PHY register A3
DDRPHY_REGAE	0x02b8	W	0x00000000	DDR PHY register AE
DDRPHY_REGB0	0x02c0	W	0x00000077	DDR PHY register B0
DDRPHY_REGB1	0x02c4	W	0x00000077	DDR PHY register B1
DDRPHY_REGB2	0x02c8	W	0x00000077	DDR PHY register B2
DDRPHY_REGB3	0x02cc	W	0x00000077	DDR PHY register B3
DDRPHY_REGB4	0x02d0	W	0x00000077	DDR PHY register B4
DDRPHY_REGB5	0x02d4	W	0x00000077	DDR PHY register B5
DDRPHY_REGB6	0x02d8	W	0x00000077	DDR PHY register B6
DDRPHY_REGB7	0x02dc	W	0x00000077	DDR PHY register B7
DDRPHY_REGB8	0x02e0	W	0x00000077	DDR PHY register B8
DDRPHY_REGB9	0x02e4	W	0x00000077	DDR PHY register B9
DDRPHY_REGBA	0x02e8	W	0x00000077	DDR PHY register BA
DDRPHY_REGBB	0x02ec	W	0x00000077	DDR PHY register BB
DDRPHY_REGBC	0x02f0	W	0x00000077	DDR PHY register BC
DDRPHY_REGBD	0x02f4	W	0x00000077	DDR PHY register BD
DDRPHY_REGBE	0x02f8	W	0x00000077	DDR PHY register BE
DDRPHY_REGC0	0x0300	W	0x00000077	DDR PHY register C0
DDRPHY_REGC1	0x0304	W	0x00000077	DDR PHY register C1
DDRPHY_REGC2	0x0308	W	0x00000077	DDR PHY register C2
DDRPHY_REGC3	0x030c	W	0x00000077	DDR PHY register C3

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Name	Offset	Size	Reset Value	Description
DDRPHY_REGC4	0x0310	W	0x00000077	DDR PHY register C4
DDRPHY_REGC5	0x0314	W	0x00000077	DDR PHY register C5
DDRPHY_REGC6	0x0318	W	0x00000077	DDR PHY register C6
DDRPHY_REGC7	0x031c	W	0x00000077	DDR PHY register C7
DDRPHY_REGC8	0x0320	W	0x00000077	DDR PHY register C8
DDRPHY_REGC9	0x0324	W	0x00000077	DDR PHY register C9
DDRPHY_REGCA	0x0328	W	0x00000007	DDR PHY register CA
DDRPHY_REGCB	0x032c	W	0x00000077	DDR PHY register CB
DDRPHY_REGCC	0x0330	W	0x00000077	DDR PHY register CC
DDRPHY_REGCD	0x0334	W	0x00000077	DDR PHY register CD
DDRPHY_REGCE	0x0338	W	0x00000077	DDR PHY register CE
DDRPHY_REGCF	0x033c	W	0x00000077	DDR PHY register CF
DDRPHY_REGD0	0x0340	W	0x00000077	DDR PHY register D0
DDRPHY_REGD1	0x0344	W	0x00000077	DDR PHY register D1
DDRPHY_REGD2	0x0348	W	0x00000077	DDR PHY register D2
DDRPHY_REGD3	0x034c	W	0x00000077	DDR PHY register D3
DDRPHY_REGD4	0x0350	W	0x00000077	DDR PHY register D4
DDRPHY_REGD5	0x0354	W	0x00000007	DDR PHY register D5
DDRPHY_REGD6	0x0358	W	0x00000077	DDR PHY register D6
DDRPHY_REGD7	0x035c	W	0x00000077	DDR PHY register D7
DDRPHY_REGD8	0x0360	W	0x00000077	DDR PHY register D8
DDRPHY_REGD9	0x0364	W	0x00000077	DDR PHY register D9
DDRPHY_REGDA	0x0368	W	0x00000077	DDR PHY register DA
DDRPHY_REGDB	0x036c	W	0x00000077	DDR PHY register DB
DDRPHY_REGDC	0x0370	W	0x00000077	DDR PHY register DC
DDRPHY_REGDD	0x0374	W	0x00000077	DDR PHY register DD
DDRPHY_REGDE	0x0378	W	0x00000070	DDR PHY register DE
DDRPHY_REGDF	0x037c	W	0x00000077	DDR PHY register DF
DDRPHY_REGE0	0x0380	W	0x00000007	DDR PHY register E0
DDRPHY_REGE1	0x0384	W	0x00000077	DDR PHY register E1
DDRPHY_REGE2	0x0388	W	0x00000077	DDR PHY register E2
DDRPHY_REGE3	0x038c	W	0x00000077	DDR PHY register E3
DDRPHY_REGE4	0x0390	W	0x00000077	DDR PHY register E4
DDRPHY_REGE5	0x0394	W	0x00000077	DDR PHY register E5
DDRPHY_REGE6	0x0398	W	0x00000077	DDR PHY register E6
DDRPHY_REGE7	0x039c	W	0x00000077	DDR PHY register E7
DDRPHY_REGE8	0x03a0	W	0x00000077	DDR PHY register E8
DDRPHY_REGE9	0x03a4	W	0x00000077	DDR PHY register E9
DDRPHY_REGEA	0x03a8	W	0x00000077	DDR PHY register EA
DDRPHY_REGEB	0x03ac	W	0x00000007	DDR PHY register EB
DDRPHY_REGEC	0x03b0	W	0x00000000	DDR PHY register EC
DDRPHY_REGF0	0x03c0	W	0x00000000	DDR PHY register F0
DDRPHY_REGF1	0x03c4	W	0x00000000	DDR PHY register F1

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Name	Offset	Size	Reset Value	Description
DDRPHY_REGF2	0x03c8	W	0x00000000	DDR PHY register F2
DDRPHY_REGF3	0x03cc	W	0x00000000	DDR PHY register F3
DDRPHY_REGF4	0x03d0	W	0x00000000	DDR PHY register F4
DDRPHY_REGFA	0x03e8	W	0x00000000	DDR PHY register FA
DDRPHY_REGFB	0x03ec	W	0x00000000	DDR PHY register FB
DDRPHY_REGFC	0x03f0	W	0x00000000	DDR PHY register FC
DDRPHY_REGFD	0x03f4	W	0x00000000	DDR PHY register FD
DDRPHY_REGFE	0x03f8	W	0x00000000	DDR PHY register FE
DDRPHY_REGFF	0x03fc	W	0x00000000	DDR PHY register FF

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

2.4.2 Detail Register Description

DDRC_MSTR

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	device_config Configuration of device used 00: x4 device 01: x8 device 10: x16 device 11: x32 device Programming Mode: Static
29	RW	0x0	frequency_mode Choose wich register are used 0: original registers 1: FREQ1 registers Programming Mode: Quasi-dynamic Group 2
28:26	RO	0x0	reserved
25:24	RW	0x3	active_ranks 01: One Rank 11: Two Ranks Programming Mode: Static
23	RO	0x0	reserved
22	RW	0x0	frequency_ratio selects the frequency ratio 0: 1:2 mode 1: 1:1 mode Programming Mode: Static
21:20	RW	0x0	active_logical_ranks Number of logical ranks for DDR4 3DS 0: monolithic (no stack) 1: 2H stack 2: 4H stack 3: 8H stack Programming Mode: Static

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Bit	Attr	Reset Value	Description
19:16	RW	0x4	burst_rdwr SDRAM burst length used: 0001: burst length of 2 0010: burst length of 4 0100: burst length of 8 1000: burst length of 16 Programming Mode: Static
15	RW	0x0	dll_off_mode 1: dll-off mode for lower frequency operation 0: dll-on mode for normal frequency operation Programming Mode: Quasi-dynamic Group 2
14	RO	0x0	reserved
13:12	RW	0x0	data_bus_width 00: full DQ bus width to SDRAM 01: half DQ bus width to SDRAM 1x: reserved Programming Mode: Static
11	RW	0x0	geardown_mode 1: enable geardow mode 0: normal mode Programming Mode: Quasi-dynamic Group 2
10	RW	0x0	en_2t_timing_mode 1: use 2T timing 0: use 1T timing Programming Mode: Static
9	RW	0x0	burstchop 1: enable burst-chop Programming Mode: Static
8	RW	0x0	burst_mode 0: sequential burst mode 1: interleaved burst mode Programming Mode: Static
7:6	RO	0x0	reserved
5	RW	0x0	lpddr4 1: LPDDR4 0: Non-LPDDR4 Programming Mode: Static
4	RW	0x0	ddr4 1: DDR4 0: Non-DDR4 Programming Mode: Static
3	RW	0x0	lpddr3 1: LPDDR3 0: Non-LPDDR3 Programming Mode: Static

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Bit	Attr	Reset Value	Description
2	RW	0x0	lpddr2 1: LPDDR2 0: Non-LPDDR2 Programming Mode: Static
1	RW	0x0	mobile 1: Mobile/LPDDR 0: Non-Mobile Programming Mode: Static
0	RW	0x1	ddr3 1: DDR3 0: Non-DDR3 Programming Mode: Static

DDRC_STAT

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12	RO	0x0	selfref_cam_not_empty Self refresh with CAMs not empty. Set to 1 when Self Refresh is entered but CAMs are not drained. Cleared after exiting Self Refresh Programming Mode: Dynamic
11:10	RO	0x0	reserved
9:8	RO	0x0	selfref_state Self refresh state. This indicates self refresh or self refresh power down state for LPDDR4. This register is used for frequency change and MRR/MRW access during self refresh. 00:SDRAM is not in Self Refresh. 01:Self refresh 1 10:Self refresh power down 11:Self refresh 2 Programming Mode: Dynamic
7:6	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
5:4	RO	0x0	selfref_type Flags if Self Refresh (except LPDDR4) or SR-Powerdown (LPDDR4) is entered and if it was under Automatic Self Refresh control only or not. 00:SDRAM is not in Self Refresh (except LPDDR4) or SR-Powerdown (LPDDR4). If retry is enabled by CRCPARCTRL1.crc_parity_retry_enable, this also indicates SRE command is still in parity error window or retry is in-progress. 11:SDRAM is in Self Refresh (except LPDDR4) or SRPowerdown (LPDDR4), which was caused by Automatic Self Refresh only. If retry is enabled, this guarantees SRE command is executed correctly without parity error. 10:SDRAM is in Self Refresh (except LPDDR4) or SRPowerdown (LPDDR4), which was not caused solely under Automatic Self Refresh control. It could have been caused by Hardware Low Power Interface and/or Software (PWRCTL.selfref_sw). If retry is enabled, this guarantees SRE command is executed correctly without parity error. 01: SDRAM is in Self Refresh, which was caused by PHY Master Request. Programming Mode: Dynamic
3	RO	0x0	reserved
2:0	RO	0x0	operating_mode Operating mode. This is 3-bits wide in configurations with mDDR/LPDDR2/LPDDR3/LPDDR4/DDR4 support and 2-bits in all other configurations. non-mDDR/LPDDR2/LPDDR3/LPDDR4 and non-DDR4 designs: 00: Init; 01:Normal; 10:Power-down; 11:Self refresh mDDR/LPDDR2/LPDDR3 or DDR4 designs: 000:Init; 001:Normal; 010:Power-down; 011:Self refresh; 1XX:Deep power-down / Maximum Power Saving Mode LPDDR4 designs: 000:Init; 001:Normal; 010:Power-down; 011:Self refresh / Self refresh power-down Programming Mode: Dynamic

DDRC_MRCTRL0

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31	RW	0x0	mr_wr Setting this register bit to 1 triggers a mode register read or write operation. When the MR operation is complete, the uMCTL2 automatically clears this bit. The other register fields of this register must be written in a separate APB transaction, before setting this mr_wr bit. It is recommended NOT to set this signal if in Init, Deep power-down or MPSM operating modes. Programming Mode: Dynamic
30	RW	0x0	pba_mode Indicates whether PBA access is executed. When setting this bit to 1 along with setting pda_en to 1, uMCTL2 initiates PBA access instead of PDA access. 0: Per DRAM Addressability mode; 1: Per Buffer Addressability mode The completion of PBA access is confirmed by MRSTAT.pda_done in the same way as PDA. Programming Mode: Dynamic
29:16	RO	0x0	reserved
15:12	RW	0x0	mr_addr Address of the mode register that is to be written to. 0000: MR0; 0001: MR1; 0010: MR2; 0011: MR3; 0100: MR4; 0101: MR5; 0110: MR6; 0111: MR7. Don't Care for LPDDR2/LPDDR3/LPDDR4 (see MRCTRL1.mr_data for mode register addressing in LPDDR2/LPDDR3/LPDDR4) In case of DDR4, the bit[3:2] corresponds to the bank group bits. Programming Mode: Dynamic
11:6	RO	0x0	reserved
5:4	RW	0x0	mr_rank Controls which rank is accessed by MRCTRL0.mr_wr. Normally, it is desired to access all ranks, so all bits should be set to 1. 0x1: select rank 0 only 0x2: select rank 1 only 0x3: select rank 0 and 1 Programming Mode: Dynamic

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Bit	Attr	Reset Value	Description
3	RW	0x0	sw_init_int Indicates whether Software intervention is allowed via MRCTRL0/MRCTRL1 before automatic SDRAM initialization routine or not. For DDR4, this bit can be used to initialize the DDR4 RCD (MR7) before automatic SDRAM initialization. For LPDDR4, this bit can be used to program additional mode registers before automatic SDRAM initialization if necessary. Note that this must be cleared to 0 after completing Software operation. Otherwise, SDRAM initialization routine will not re-start. 0: Software intervention is not allowed; 1: Software intervention is allowed Programming Mode: Dynamic
2	RW	0x0	pda_en Indicates whether the mode register operation is MRS in PDA mode or not 0: MRS; 1: MRS in Per DRAM Addressability mode Note that when pba_mode=1, PBA access is initiated instead of PDA access. Programming Mode: Dynamic
1	RW	0x0	mpr_en Indicates whether the mode register operation is MRS or WR/RD for MPR (only supported for DDR4) 0: MRS; 1: WR/RD for MPR Programming Mode: Dynamic
0	RW	0x0	mr_type Indicates whether the mode register operation is read or write. Only used for LPDDR2/LPDDR3/LPDDR4/DDR4. 0: Write; 1: Read Programming Mode: Dynamic

DDRC_MRCTRL1

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:18	RO	0x0	reserved
17:0	RW	0x00000	mr_data Mode register write data for all non-LPDDR2/non-LPDDR3/non-LPDDR4 modes. For LPDDR2/LPDDR3/LPDDR4, MRCTRL1[15:0] are interpreted as [15:8] MR Address [7:0] MR data for writes, don't care for reads. This is 18-bits wide in configurations with DDR4 support and 16-bits in all other configurations. Programming Mode: Dynamic

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DDRC_MRSTAT

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:9	RO	0x0	reserved
8	RO	0x0	pda_done The SoC core may initiate a MR write operation in PDA/PBA mode only if this signal is low. This signal goes high when three consecutive MRS commands related to the PDA/PBA mode are issued to the SDRAM. This signal goes low when MRCTRL0.pda_en becomes 0. Therefore, it is recommended to write MRCTRL0.pda_en to 0 after this signal goes high in order to prepare to perform PDA operation next time. 0: Indicates that mode register write operation related to PDA/PBA is in progress or has not started yet. 1: Indicates that mode register write operation related to PDA/PBA has competed. Programming Mode: Dynamic
7:1	RO	0x0	reserved
0	RO	0x0	mr_wr_busy The SoC core may initiate a MR write operation only if this signal is low. This signal goes high in the clock after the uMCTL2 accepts the MRW/MRR request. It goes low when the MRW/MRR command is issued to the SDRAM. It is recommended not to perform MRW/MRR commands when MRSTAT.mr_wr_busy is high. 0: Indicates that the SoC core can initiate a mode register write operation 1: Indicates that mode register write operation is in progress Programming Mode: Dynamic

DDRC_MRCTRL2

Address: Operational Base + offset (0x001c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mr_device_sel Indicates the device(s) to be selected during the MRS that happens in PDA mode. Each bit is associated with one device. For example, bit[0] corresponds to Device 0, bit[1] to Device 1 etc. A '1' should be programmed to indicate that the MRS command should be applied to that device. A '0' indicates that the MRS commands should be skipped for that device. Programming Mode: Dynamic

DDRC_DERATEEN

Address: Operational Base + offset (0x0020)

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Bit	Attr	Reset Value	Description
31:11	RO	0x0	reserved
10:8	RW	0x0	rc_derate_value Derate value of tRC for LPDDR4 0: Derating uses +1. 1: Derating uses +2. 2: Derating uses +3. 3: Derating uses +4. Present only in designs configured to support LPDDR4. The required number of cycles for derating can be determined by dividing 3.75ns by the core_ddrc_core_clk period, and rounding up the next integer. Programming Mode: Quasi-dynamic Group 2 and Group 4
7:4	RW	0x0	derate_byte Derate byte Present only in designs configured to support LPDDR2/LPDDR3/LPDDR4 Indicates which byte of the MRR data is used for derating. Programming Mode: Static
3:2	RO	0x0	reserved
1	RW	0x0	derate_value Derate value 0: Derating uses +1. 1: Derating uses +2. Present only in designs configured to support LPDDR2/LPDDR3/LPDDR4 Set to 0 for all LPDDR2 speed grades as derating value of +1.875 ns is less than a core_ddrc_core_clk period. For LPDDR3/4, if the period of core_ddrc_core_clk is less than 1.875ns, this register field should be set to 1; otherwise it should be set to 0. Programming Mode: Quasi-dynamic Group 2 and Group 4
0	RW	0x0	derate_enable Enables derating 0: Timing parameter derating is disabled 1: Timing parameter derating is enabled using MR4 read value. Present only in designs configured to support LPDDR2/LPDDR3/LPDDR4 This field must be set to 0 for non-LPDDR2/LPDDR3/LPDDR4 mode. Programming Mode: Dynamic

DDRC_DERATEINT

Address: Operational Base + offset (0x0024)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00800000	mr4_read_interval Interval between two MR4 reads, used to derate the timing parameters. Present only in designs configured to support LPDDR2/LPDDR3/LPDDR4. This register must not be set to zero. Unit: DFI clock cycle. Programming Mode: Static

DDRC_PWRCTL

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:9	RO	0x0	reserved
8	RW	0x0	lpddr4_sr_allowed Indicates whether transition from SR-PD to SR and back to SR-PD is allowed. This register field cannot be modified while PWRCTL.selfref_sw==1. 0: SR-PD -> SR -> SR-PD not allowed 1: SR-PD -> SR -> SR-PD allowed Programming Mode: Dynamic
7	RW	0x0	dis_cam_drain_selfref Indicates whether skipping CAM draining is allowed when entering Self-Refresh. This register field cannot be modified while PWRCTL.selfref_sw==1. 0: CAMs must be empty before entering SR 1: CAMs are not emptied before entering SR Programming Mode: Dynamic
6	RW	0x0	stay_in_selfref Self refresh state is an intermediate state to enter to Selfrefresh power down state or exit Self refresh power down state for LPDDR4. This register controls transition from the Self refresh state. 1: Prohibit transition from Self refresh state 0: Allow transition from Self refresh state Programming Mode: Dynamic
5	RW	0x0	selfref_sw A value of 1 to this register causes system to move to Self Refresh state immediately, as long as it is not in INIT or DPD/MPSM operating_mode. This is referred to as Software Entry/Exit to Self Refresh. 1: Software Entry to Self Refresh 0: Software Exit from Self Refresh Programming Mode: Dynamic

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Bit	Attr	Reset Value	Description
4	RW	0x0	mpsm_en When this is 1, the uMCTL2 puts the SDRAM into maximum power saving mode when the transaction store is empty. This register must be reset to '0' to bring uMCTL2 out of maximum power saving mode. Present only in designs configured to support DDR4. For non-DDR4, this register should not be set to 1. Programming Mode: Dynamic
3	RW	0x0	en_dfi_dram_clk_disable Enable the assertion of dfi_dram_clk_disable whenever a clock is not required by the SDRAM. If set to 0, dfi_dram_clk_disable is never asserted. Assertion of dfi_dram_clk_disable is as follows: In DDR2/DDR3, can only be asserted in Self Refresh. In DDR4, can be asserted in the Self Refresh and Maximum Power Saving Mode In mDDR/LPDDR2/LPDDR3, can be asserted in the Self Refresh, Power Down, Deep Power Down and Normal operation (Clock Stop) In LPDDR4, can be asserted in the Self Refresh Power Down, Power Down and Normal operation (Clock Stop) Programming Mode: Dynamic
2	RW	0x0	deeppowerdown_en When this is 1, uMCTL2 puts the SDRAM into deep powerdown mode when the transaction store is empty. This register must be reset to '0' to bring uMCTL2 out of deep power-down mode. Controller performs automatic SDRAM initialization on deep power-down exit. Present only in designs configured to support mDDR or LPDDR2 or LPDDR3. For non-mDDR/non-LPDDR2/nonLPDDR3, this register should not be set to 1. Programming Mode: Dynamic
1	RW	0x0	powerdown_en If true then the uMCTL2 goes into power-down after a programmable number of cycles "maximum idle clocks before power down" PWRTMG.powerdown_to_x32). This register bit may be re-programmed during the course of normal operation. Programming Mode: Dynamic
0	RW	0x0	selfref_en If true then the uMCTL2 puts the SDRAM into Self Refresh after a programmable number of cycles "maximum idle clocks before Self Refresh (PWRTMG.selfref_to_x32)". This register bit may be re-programmed during the course of normal operation. Programming Mode: Dynamic

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DDRC_PWRTMG

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:16	RW	0x40	selfref_to_x32 After this many clocks of the DDRC command channel being idle the uMCTL2 automatically puts the SDRAM into Self Refresh. The DDRC command channel is considered idle when there are no HIF commands outstanding. This must be enabled in the PWRCTL.selfref_en. Unit: Multiples of 32 DFI clocks. Programming Mode: Static
15:8	RW	0x20	t_dpd_x4096 Minimum deep power-down time. For mDDR, value from the JEDEC specification is 0 as mDDR exits from deep power-down mode immediately after PWRCTL.deeppowerdown_en is de-asserted. For LPDDR2/LPDDR3, value from the JEDEC specification is 500us. Unit: Multiples of 4096 DFI clocks. Programming Mode: Static
7:5	RO	0x0	reserved
4:0	RW	0x10	powerdown_to_x32 After this many clocks of the DDRC command channel being idle the uMCTL2 automatically puts the SDRAM into powerdown. The DDRC command channel is considered idle when there are no HIF commands outstanding. This must be enabled in the PWRCTL.powerdown_en. Unit: Multiples of 32 DFI clocks Programming Mode: Static

DDRC_HWLPCTL

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	hw_lp_idle_x32 Hardware idle period. The cactive_ddrc output is driven low if the DDRC command channel is idle for hw_lp_idle * 32 cycles if not in INIT or DPD/MPSM operating_mode. The DDRC command channel is considered idle when there are no HIF commands outstanding. The hardware idle function is disabled when hw_lp_idle_x32=0. Unit: Multiples of 32 DFI clocks. Programming Mode: Static
15:2	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
1	RW	0x1	hw_lp_exit_idle_en When this bit is programmed to 1 the cactive_in_ddrc pin of the DDRC can be used to exit from the automatic clock stop, automatic power down or automatic self-refresh modes. Note, it will not cause exit of Self-Refresh that was caused by Hardware Low Power Interface and/or Software (PWRCTL.selfref_sw). Programming Mode: Static
0	RW	0x1	hw_lp_en Enable for Hardware Low Power Interface. Programming Mode: Quasi-dynamic Group 3

DDRC_HWFFCCTL

Address: Operational Base + offset (0x003c)

Bit	Attr	Reset Value	Description
31:7	RO	0x0	reserved
6	RW	0x0	target_vrcg Set target value of VRCG (MR13 OP[3]). This field value is used when HWFFC request has been issued. Programming Mode: Static
5	RW	0x0	init_vrcg Set initial value of VRCG (MR13 OP[3]). This field value is used when HWFFCCTL.hwffc_en has been changed to 11. Programming Mode: Static
4	RW	0x1	init_fsp Set initial value of FSP-OP (MR13 OP[7]). This field value is used when HWFFCCTL.hwffc_en has been changed to 11. Programming Mode: Static
3:1	RO	0x0	reserved
0	RW	0x0	hwffc_en Enable HWFFC through Hardware Low Power Interface. The other fields of this register is used only when changing this field to 11. 00: Disable HWFFC 10: Intermediate, set only when disabling HWFFC 11: Enable HWFFC 01: Not allowed Programming Mode: Dynamic

DDRC_HWFFCSTAT

Address: Operational Base + offset (0x0040)

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Bit	Attr	Reset Value	Description
31:10	RO	0x0	reserved
9	RO	0x0	current_vrcg Indicates current value of VRCG (MR13 OP[3]). Programming Mode: Dynamic
8	RO	0x0	current_fsp Indicates current value of FSP-OP (MR13 OP[7]). Programming Mode: Dynamic
7:5	RO	0x0	reserved
4	RO	0x0	current_frequency Indicates the current frequency. 0: Frequency 0/Normal 1: Frequency 1/FREQ1 Programming Mode: Dynamic
3:2	RO	0x0	reserved
1	RO	0x0	hwffc_operating_mode Operating mode of HWFFC. 0: Normal 1: Self Refresh or SR-Powerdown Programming Mode: Dynamic
0	RO	0x0	hwffc_in_progress Indicates HWFFC is in progress. Programming Mode: Dynamic

DDRC_RFSHCTL0

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:20	RW	0x2	refresh_margin Threshold value in number of DFI clock cycles before the critical refresh or page timer expires. A critical refresh is to be issued before this threshold is reached. It is recommended that this not be changed from the default value, currently shown as 0x2. It must always be less than internally used t_rfc_nom_x32. Note that, in LPDDR2/LPDDR3/LPDDR4, internally used t_rfc_nom_x32 may be equal to RFSHTMG.t_rfc_nom_x32>>2 if derating is enabled (DERATEEN.derate_enable=1). Otherwise, internally used t_rfc_nom_x32 will be equal to RFSHTMG.t_rfc_nom_x32. Unit: Multiples of 32 DFI clocks. Programming Mode: Dynamic - Refresh Related
19:17	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
16:12	RW	0x10	refresh_to_x32 If the refresh timer (tRFCnom, also known as tREFI) has expired at least once, but it has not expired (RFSHCTL0.refresh_burst+1) times yet, then a speculative refresh may be performed. A speculative refresh is a refresh performed at a time when refresh would be useful, but before it is absolutely required. When the SDRAM bus is idle for a period of time determined by this RFSHCTL0.refresh_to_x32 and the refresh timer has expired at least once since the last refresh, then a speculative refresh is performed. Speculative refreshes continues successively until there are no refreshes pending or until new reads or writes are issued to the uMCTL2. Unit: Multiples of 32 DFI clocks. Programming Mode: Dynamic - Refresh Related
11:9	RO	0x0	reserved
8:4	RW	0x00	refresh_burst The programmed value + 1 is the number of refresh timeouts that is allowed to accumulate before traffic is blocked and the refreshes are forced to execute. Closing pages to perform a refresh is a one-time penalty that must be paid for each group of refreshes. Therefore, performing refreshes in a burst reduces the per-refresh penalty of these page closings. Higher numbers for RFSHCTL.refresh_burst slightly increases utilization; lower numbers decreases the worstcase latency associated with refreshes. 0: single refresh 1: burst-of-2 refresh 7: burst-of-8 refresh For DDR2/3, the refresh is always per-rank and not perbank. The rank refresh can be accumulated over 8*tREFI cycles using the burst refresh feature. In DDR4 mode, according to Fine Granularity feature, 8 refreshes can be postponed in 1X mode, 16 refreshes in 2X mode and 32 refreshes in 4X mode. If using PHY-initiated updates, care must be taken in the setting of RFSHCTL0.refresh_burst, to ensure that tRFCmax is not violated due to a PHY-initiated update occurring shortly before a refresh burst was due. In this situation, the refresh burst will be delayed until the PHYinitiated update is complete. Programming Mode: Dynamic - Refresh Related
3	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
2	RW	0x0	per_bank_refresh 1: Per bank refresh; 0: All bank refresh. Per bank refresh allows traffic to flow to other banks. Per bank refresh is not supported by all LPDDR2 devices but should be supported by all LPDDR3/LPDDR4 devices. Programming Mode: Static
1:0	RO	0x0	reserved

DDRC_RFSHCTL1

Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	refresh_timer1_start_value_x32 Refresh timer start for rank 1 (only present in multi-rank configurations). This is useful in staggering the refreshes to multiple ranks to help traffic to proceed. This is explained in Refresh Controls section of architecture chapter. Unit: Multiples of 32 DFI clock cycles. Programming Mode: Dynamic - Refresh Related
15:12	RO	0x0	reserved
11:0	RW	0x000	refresh_timer0_start_value_x32 Refresh timer start for rank 0 (only present in multi-rank configurations). This is useful in staggering the refreshes to multiple ranks to help traffic to proceed. This is explained in Refresh Controls section of architecture chapter. Unit: Multiples of 32 DFI clock cycles. Programming Mode: Dynamic - Refresh Related

DDRC_RFSHCTL3

Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:7	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
6:4	RW	0x0	refresh_mode Fine Granularity Refresh Mode 000: Fixed 1x (Normal mode) 001: Fixed 2x 010: Fixed 4x 101: Enable on the fly 2x (not supported) 110: Enable on the fly 4x (not supported) Everything else - reserved Note: Only Fixed 1x mode is supported if RFSHCTL3.dis_auto_refresh = 1. Note: The on-the-fly modes are not supported in this version of the uMCTL2. Note: This must be set up while the Controller is in reset or while the Controller is in self-refresh mode. Changing this during normal operation is not allowed. Making this a dynamic register will be supported in future version of the uMCTL2. Note: This register field has effect only if a DDR4 SDRAM device is in use (MSTR.ddr4 = 1). Programming Mode: Quasi-dynamic Group 2
3:2	RO	0x0	reserved
1	RW	0x0	refresh_update_level Toggle this signal (either from 0 to 1 or from 1 to 0) to indicate that the refresh register(s) have been updated. refresh_update_level must not be toggled when the DDRC is in reset (core_ddrc_rstn = 0). The refresh register(s) are automatically updated when exiting reset. Programming Mode: Dynamic
0	RW	0x0	dis_auto_refresh When '1', disable auto-refresh generated by the uMCTL2. When auto-refresh is disabled, the SoC core must generate refreshes using the registers DBGCMD.rankn_refresh. When dis_auto_refresh transitions from 0 to 1, any pending refreshes are immediately scheduled by the uMCTL2. If DDR4 CRC/parity retry is enabled (CRCPARCTL1.crc_parity_retry_enable = 1), disable autorefresh is not supported, and this bit must be set to '0'. (DDR4 only) If FGR mode is enabled (RFSHCTL3.refresh_mode > 0), disable auto-refresh is not supported, and this bit must be set to '0'. This register field is changeable on the fly. Programming Mode: Dynamic - Refresh Related

DDRC_RFSHTMG

Address: Operational Base + offset (0x0064)

Bit	Attr	Reset Value	Description
31	RW	0x0	t_rfc_nom_x1_sel Specifies whether the t_rfc_nom_x1_x32 register value is x1 or x32
30:28	RO	0x0	reserved
27:16	RW	0x062	t_rfc_nom_x1_x32 tREFI: Average time interval between refreshes per rank (Specification: 7.8us for DDR2, DDR3 and DDR4. See JEDEC specification for mDDR, LPDDR2, LPDDR3 and LPDDR4). For LPDDR2/LPDDR3/LPDDR4: if using all-bank refreshes (RFSHCTL0.per_bank_refresh= 0), this register should be set to tREFIab if using per-bank refreshes (RFSHCTL0.per_bank_refresh = 1), this register should be set to tREFIpb When the controller is operating in 1:2 frequency ratio mode, program this to (tREFI/2), no rounding up. In DDR4 mode, tREFI value is different depending on the refresh mode. The user should program the appropriate value from the spec based on the value programmed in the refresh mode register. Note that if RFSHTMG.t_rfc_nom_x1_sel==1, RFSHTMG.t_rfc_nom_x1_x32 must be greater than RFSHTMG.t_rfc_min; if RFSHTMG.t_rfc_nom_x1_sel==0, RFSHTMG.t_rfc_nom_x1_x32*32 must be greater than RFSHTMG.t_rfc_min; RFSHTMG.t_rfc_nom_x32 must be greater than 0x1. Non-DDR4 or DDR4 Fixed 1x mode:RFSHTMG.t_rfc_nom_x1_x32 must be less than or equal to 0xFFE. DDR4 Fixed 2x mode: RFSHTMG.t_rfc_nom_x1_x32 must be less than or equal to 0x7FF. DDR4 Fixed 4x mode: RFSHTMG.t_rfc_nom_x1_x32 must be less than or equal to 0x3FF. Unit: Clocks or multiples of 32 clocks, depending on RFSHTMG.t_rfc_nom_x1_sel. Programming Mode: Dynamic - Refresh Related
15	RW	0x0	lpddr3_trefbw_en Used only when LPDDR3 memory type is connected. Should only be changed when uMCTL2 is in reset. Specifies whether to use the tREFBW parameter (required by some LPDDR3 devices which comply with earlier versions of the LPDDR3 JEDEC specification) or not: 0: tREFBW parameter not used 1: tREFBW parameter used Programming Mode: Static
14:10	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
9:0	RW	0x08c	t_rfc_min tRFC (min): Minimum time from refresh to refresh or activate. t_rfc_min should be set to RoundUp(RoundUp(tRFCmin/tCK)/2). In LPDDR2/LPDDR3/LPDDR4 mode: if using all-bank refreshes, the tRFCmin value in the above equations is equal to tRFCab if using per-bank refreshes, the tRFCmin value in the above equations is equal to tRFCpb In DDR4 mode, the tRFCmin value in the above equations is different depending on the refresh mode (fixed 1X,2X,4X) and the device density. The user should program the appropriate value from the spec based on the 'refresh_mode' and the device density that is used. Unit: DFI Clocks. Programming Mode: Dynamic - Refresh Related

DDRC_CRCPARCTL0

Address: Operational Base + offset (0x00c0)

Bit	Attr	Reset Value	Description
31:3	RO	0x0	reserved
2	W1C	0x0	dfi_alert_err_cnt_clr DFI alert error count clear. Clear bit for DFI alert error counter. Asserting this bit will clear the DFI alert error counter, CRCPARSTAT.dfi_alert_err_cnt. When the clear operation is complete, the uMCTL2 automatically clears this bit. Programming Mode: Dynamic
1	W1C	0x0	dfi_alert_err_int_clr Interrupt clear bit for DFI alert error. If this bit is set, the alert error interrupt on CRCPARSTAT.dfi_alert_err_int will be cleared. When the clear operation is complete, the uMCTL2 automatically clears this bit. Programming Mode: Dynamic
0	RW	0x0	dfi_alert_err_int_en Interrupt enable bit for DFI alert error. If this bit is set, any parity/CRC error detected on the dfi_alert_n input will result in an interrupt being set on CRCPARSTAT.dfi_alert_err_int. Programming Mode: Dynamic

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DDRC_CRCPARCTL1

Address: Operational Base + offset (0x00c4)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	retry_add_rd_lat Retry additional read latency value. Delay value used is retry_add_rd_lat+1. Only used if CRCPARCTL1.retry_add_rd_lat_en is enabled. Selects the number of pipeline stages to dfi_rddata_valid/dfi_rddata/dfi_rddata_dbi before rest of internal uMCTL2 logic observes it. Required to compensate for fact delay in PHY/PCB for generating dfi_alert_n for retry may be more than the delay in PHY/PCB on read data path. Recommended settings (in terms of core_ddrc_core_clk): (Maximum Alert delay through PHY/PCB from erroneous read command including tPAR_UNKNOWN) - (Minimum Read data delay through PHY/PCB from erroneous read command) + (PHY's max granularity of dfi_rddata beats that may be corrupted before erroneous Read) Note: This calculation depends on various items such as RL, tPAR_ALERT_ON/tPAR_UNKNOWN/RCD/PHY/PCB behavior. Unit: DFI clock cycles. Programming Mode: Static
15	RW	0x0	retry_add_rd_lat_en Retry additional read latency enable. Number of pipeline stages selected is defined as CRCPARCTL1.retry_add_lat+1. Only set if CRCPARCTL1.crc_parity_retry_enable = 1 Programming Mode: Static
14:13	RO	0x0	reserved
12	RW	0x1	caparity_disable_before_sr If DDR4-SDRAM's CA parity is enabled by INIT6.mr5[2:0]!=0 and this register is set to 1, CA parity is automatically disabled before Self-Refresh entry and enabled after SelfRefresh exit by issuing MR5. 1: CA parity is disabled before Self-Refresh entry 0: CA parity is not disabled before Self-Refresh entry If Geardown is used by MSTR.geardown_mode=1, this register must be set to 1. If this register set to 0, DRAMTMG5.t_ckesr and DRAMTMG5.t_cksre must be increased by PL(Parity latency) Programming Mode: Static
11:8	RO	0x0	reserved

Bit	Attr	Reset Value	Description
7	RW	0x0	crc_inc_dm CRC Calculation setting register 1: CRC includes DM signal 0: CRC not includes DM signal Present only in designs configured to support DDR4. Programming Mode: Static
6:5	RO	0x0	reserved
4	RW	0x0	crc_enable CRC enable Register 1: Enable generation of CRC 0: Disable generation of CRC The setting of this register should match the CRC mode register setting in the DRAM. Programming Mode: Static
3:1	RO	0x0	reserved
0	RW	0x0	parity_enable C/A Parity enable register 1: Enable generation of C/A parity and detection of C/A parity error 0: Disable generation of C/A parity and disable detection of C/A parity error If RCD's parity error detection or SDRAM's parity detection is enabled, this register should be 1. Programming Mode: Static

DDRC_CRCPARSTAT

Address: Operational Base + offset (0x00cc)

Bit	Attr	Reset Value	Description
31:18	RO	0x0	reserved
17	RO	0x0	dfi_alert_err_fatl_int Fatal parity error interrupt. One or more these situation below happens, this interrupt bit is set: MPSMX caused parity error. (RCD's parity error detection only) Parity error happens again during software intervention time MRS was in retry_fifo_max_hold_timer_x4 window from alert_n=0 or STAT.operating_mode is Init. It remains set until cleared by CRCPARCTL0.dfi_alert_err_fatl_clr. If this interrupt is asserted, system reset is strongly recommended. Programming Mode: Static

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Bit	Attr	Reset Value	Description
16	RO	0x0	dfi_alert_err_int DFI alert error interrupt. If a parity/CRC error is detected on dfi_alert_n, and the interrupt is enabled by CRCPARCTL0.dfi_alert_err_int_en, this interrupt bit will be set. It will remain set until cleared by CRCPARCTL0.dfi_alert_err_int_clr Programming Mode: Static
15:0	RO	0x0000	dfi_alert_err_cnt DFI alert error count. If a parity/CRC error is detected on dfi_alert_n, this counter be incremented. This is independent of the setting of CRCPARCTL0.dfi_alert_err_int_en. It will saturate at 0xFFFF, and can be cleared by asserting CRCPARCTL0.dfi_alert_err_cnt_clr. Programming Mode: Static

DDRC_INIT0

Address: Operational Base + offset (0x00d0)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	skip_dram_init If lower bit is enabled the SDRAM initialization routine is skipped. The upper bit decides what state the controller starts up in when reset is removed 00: SDRAM Intialization routine is run after power-up 01: SDRAM Intialization routine is skipped after powerup. Controller starts up in Normal Mode 11: SDRAM Intialization routine is skipped after powerup. Controller starts up in Self-refresh Mode 10: SDRAM Intialization routine is run after power-up. Programming Mode: Quasi-dynamic Group 2
29:26	RO	0x0	reserved
25:16	RW	0x002	post_cke_x1024 Cycles to wait after driving CKE high to start the SDRAM initialization sequence. Unit: 1024 DFI clock cycles. DDR2 typically requires a 400 ns delay, requiring this value to be programmed to 2 at all clock speeds. LPDDR2/LPDDR3 typically requires this to be programmed for a delay of 200 us. LPDDR4 typically requires this to be programmed for a delay of 2 us. When the controller is operating in 1:2 frequency ratio mode, program this to JEDEC spec value divided by 2, and round it up to the next integer value. Programming Mode: Static
15:12	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
11:0	RW	0x04e	pre_cke_x1024 Cycles to wait after reset before driving CKE high to start the SDRAM initialization sequence. Unit: 1024 DFI clock cycles. DDR2 specifications typically require this to be programmed for a delay of >= 200 us. LPDDR2/LPDDR3: tINIT1 of 100 ns (min) LPDDR4: tINIT3 of 2 ms (min) When the controller is operating in 1:2 frequency ratio mode, program this to JEDEC spec value divided by 2, and round it up to the next integer value. Programming Mode: Static

DDRC_INIT1

Address: Operational Base + offset (0x00d4)

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24:16	RW	0x000	dram_rstn_x1024 Number of cycles to assert SDRAM reset signal during init sequence. This is only present for designs supporting DDR3, DDR4 or LPDDR4 devices. When the controller is operating in 1:2 frequency ratio mode, program this to JEDEC spec value divided by 2, and round it up to the next integer value. Unit: 1024 DFI clock cycles. Programming Mode: Static
15:4	RO	0x0	reserved
3:0	RW	0x0	pre_ocd_x32 Wait period before driving the OCD complete command to SDRAM. Unit: Counts of a global timer that pulses every 32 DFI clock cycles. There is no known specific requirement for this; it may be set to zero. Programming Mode: Static

DDRC_INIT2

Address: Operational Base + offset (0x00d8)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved

Bit	Attr	Reset Value	Description
15:8	RW	0x0d	idle_after_reset_x32 Idle time after the reset command, tINIT4. Present only in designs configured to support LPDDR2. When the controller is operating in 1:2 frequency ratio mode, program this to JEDEC spec value divided by 2, and round it up to the next integer value. Unit: 32 DFI clock cycles. Programming Mode: Static
7:4	RO	0x0	reserved
3:0	RW	0x5	min_stable_clock_x1 Time to wait after the first CKE high, tINIT2. Present only in designs configured to support LPDDR2/LPDDR3. LPDDR2/LPDDR3 typically requires 5 x tCK delay. When the controller is operating in 1:2 frequency ratio mode, program this to JEDEC spec value divided by 2, and round it up to the next integer value. Unit: DFI clock cycles. Programming Mode: Static

DDRC_INIT3

Address: Operational Base + offset (0x00dc)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	mr DDR2: Value to write to MR register. Bit 8 is for DLL and the setting here is ignored. The uMCTL2 sets this bit appropriately. DDR3/DDR4: Value loaded into MR0 register. mDDR: Value to write to MR register. LPDDR2/LPDDR3/LPDDR4 - Value to write to MR1 register Programming Mode: Quasi-dynamic Group 1 and Group 4
15:0	RW	0x0510	emr DDR2: Value to write to EMR register. Bits 9:7 are for OCD and the setting in this register is ignored. The uMCTL2 sets those bits appropriately. DDR3/DDR4: Value to write to MR1 register Set bit 7 to 0. If PHY-evaluation mode training is enabled, this bit is set appropriately by the uMCTL2 during write leveling. mDDR: Value to write to EMR register. LPDDR2/LPDDR3/LPDDR4 - Value to write to MR2 register Programming Mode: Quasi-dynamic Group 4

DDRC_INIT4

Address: Operational Base + offset (0x00e0)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	emr2 DDR2: Value to write to EMR2 register. DDR3/DDR4: Value to write to MR2 register LPDDR2/LPDDR3/LPDDR4: Value to write to MR3 register mDDR: Unused Programming Mode: Quasi-dynamic Group 4
15:0	RW	0x0000	emr3 DDR2: Value to write to EMR3 register. DDR3/DDR4: Value to write to MR3 register mDDR/LPDDR2/LPDDR3: Unused LPDDR4: Value to write to MR13 register Programming Mode: Quasi-dynamic Group 2 and Group 4

DDRC_INIT5

Address: Operational Base + offset (0x00e4)

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:16	RW	0x10	dev_zqinit_x32 ZQ initial calibration, tZQINIT. Present only in designs configured to support DDR3 or DDR4 or LPDDR2/LPDDR3. DDR3 typically requires 512 SDRAM clock cycles. DDR4 requires 1024 SDRAM clock cycles. LPDDR2/LPDDR3 requires 1 us. When the controller is operating in 1:2 frequency ratio mode, program this to JEDEC spec value divided by 2, and round it up to the next integer value. Unit: 32 DFI clock cycles. Programming Mode: Static
15:10	RO	0x0	reserved
9:0	RW	0x004	max_auto_init_x1024 Maximum duration of the auto initialization, tINIT5. Present only in designs configured to support LPDDR2/LPDDR3. LPDDR2/LPDDR3 typically requires 10 us. Unit: 1024 DFI clock cycles. Programming Mode: Static

DDRC_INIT6

Address: Operational Base + offset (0x00e8)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	mr4 DDR4- Value to be loaded into SDRAM MR4 registers. LPDDR4- Value to be loaded into SDRAM MR11 registers. Programming Mode: Quasi-dynamic Group 2 and Group 4

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Bit	Attr	Reset Value	Description
15:0	RW	0x0000	mr5 DDR4- Value to be loaded into SDRAM MR5 registers. LPDDR4- Value to be loaded into SDRAM MR12 registers. Programming Mode: Quasi-dynamic Group 1 and Group 4

DDRC_INIT7

Address: Operational Base + offset (0x00ec)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	mr6 DDR4- Value to be loaded into SDRAM MR6 registers. LPDDR4- Value to be loaded into SDRAM MR14 registers. Programming Mode: Quasi-dynamic Group 4
15:0	RW	0x0000	mr22 LPDDR4- Value to be loaded into SDRAM MR22 registers. Used in LPDDR4 designs only. Programming Mode: Quasi-dynamic Group 4

DDRC_DIMMCTL

Address: Operational Base + offset (0x00f0)

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4	RW	0x0	mrs_bg1_en Enable for BG1 bit of MRS command. BG1 bit of the mode register address is specified as RFU (Reserved for Future Use) and must be programmed to 0 during MRS. In case where DRAMs which do not have BG1 are attached and both the CA parity and the Output Inversion are enabled, this must be set to 0, so that the calculation of CA parity will not include BG1 bit. Note: This has no effect on the address of any other memory accesses, or of software-driven mode register accesses. If address mirroring is enabled, this is applied to BG1 of even ranks and BG0 of odd ranks. 1: Enabled; 0: Disabled Programming Mode: Static

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Bit	Attr	Reset Value	Description
3	RW	0x0	mrs_a17_en Enable for A17 bit of MRS command. A17 bit of the mode register address is specified as RFU (Reserved for Future Use) and must be programmed to 0 during MRS. In case where DRAMs which do not have A17 are attached and the Output Inversion are enabled, this must be set to 0, so that the calculation of CA parity will not include A17 bit. Note: This has no effect on the address of any other memory accesses, or of software-driven mode register accesses. 1: Enabled; 0: Disabled Programming Mode: Static
2:0	RO	0x0	reserved

DDRC_RANKCTL

Address: Operational Base + offset (0x00f4)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:8	RW	0x6	diff_rank_wr_gap Only present for multi-rank configurations. Indicates the number of clocks of gap in data responses when performing consecutive writes to different ranks. This is used to switch the delays in the PHY to match the rank requirements. This value should consider both PHY requirement and ODT requirement. PHY requirement: tphy_wrcsgap (see PHY databook for value of tphy_wrcsgap) If CRC feature is enabled, should be increased by 1. If write preamble is set to 2tCK(DDR4 only), should be increased by 1. If write postamble is set to 1.5tCK(LPDDR4 only), should be increased by 1. ODT requirement: The value programmed in this register takes care of the ODT switch off timing requirement when switching ranks during writes. For LPDDR4, the requirement is ODTLoff - ODTLon - BL/2 + 1 When the controller is operating in 1:2 mode, program this to the larger value divided by two and round it up to the next integer. Programming Mode: Quasi-dynamic Group 2

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Bit	Attr	Reset Value	Description
7:4	RW	0x6	diff_rank_rd_gap Only present for multi-rank configurations. Indicates the number of clocks of gap in data responses when performing consecutive reads to different ranks. This is used to switch the delays in the PHY to match the rank requirements. This value should consider both PHY requirement and ODT requirement. PHY requirement: tphy_rdcsgap (see PHY databook for value of tphy_rdcsgap) If read preamble is set to 2tCK(DDR4 only), should be increased by 1. If read postamble is set to 1.5tCK(LPDDR4 only), should be increased by 1. ODT requirement: The value programmed in this register takes care of the ODT switch off timing requirement when switching ranks during reads. When the controller is operating in 1:2 mode, program this to the larger value divided by two and round it up to the next integer. Programming Mode: Static
3:0	RW	0xf	max_rank_rd Only present for multi-rank configurations. Background: Reads to the same rank can be performed back-to-back. Reads to different ranks require additional gap dictated by the register RANKCTL.diff_rank_rd_gap. This is to avoid possible data bus contention as well as to give PHY enough time to switch the delay when changing ranks. The uMCTL2 arbitrates for bus access on a cycle-by-cycle basis; therefore after a read is scheduled, there are few clock cycles (determined by the value on RANKCTL.diff_rank_rd_gap register) in which only reads from the same rank are eligible to be scheduled. This prevents reads from other ranks from having fair access to the data bus. This parameter represents the maximum number of reads that can be scheduled consecutively to the same rank. After this number is reached, a delay equal to RANKCTL.diff_rank_rd_gap is inserted by the scheduler to allow all ranks a fair opportunity to be scheduled. Higher numbers increase bandwidth utilization, lower numbers increase fairness. This feature can be DISABLED by setting this register to 0. When set to 0, the Controller will stay on the same rank as long as commands are available for it. Minimum programmable value is 0 (feature disabled) and maximum programmable value is 0xF. Programming Mode: Static

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DDRC_DRAMTMG0

Address: Operational Base + offset (0x0100)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x0f	wr2pre Minimum time between write and precharge to same bank. Unit: DFI Clocks Specifications: WL + BL/2 + tWR = approximately 8 cycles + 15 ns = 14 clocks @400MHz and less for lower frequencies where: WL = write latency BL = burst length. This must match the value programmed in the BL bit of the mode register to the SDRAM. BST (burst terminate) is not supported at present. tWR = Write recovery time. This comes directly from the SDRAM specification. Add one extra cycle for LPDDR2/LPDDR3/LPDDR4 for this parameter. When the controller is operating in 1:2 frequency ratio mode, 1T mode, divide the above value by 2. No rounding up. When the controller is operating in 1:2 frequency ratio mode, 2T mode or LPDDR4 mode, divide the above value by 2 and round it up to the next integer value. Programming Mode: Quasi-dynamic Group 1 and Group 2 and Group 4
23:22	RO	0x0	reserved
21:16	RW	0x10	t_faw tFAW Valid only when 8 or more banks(or banks x bank groups) are present. In 8-bank design, at most 4 banks must be activated in a rolling window of tFAW cycles. When the controller is operating in 1:2 frequency ratio mode, program this to (tFAW/2) and round up to next integer value. In a 4-bank design, set this register to 0x1 independent of the 1:1/1:2 frequency mode. Unit: DFI Clocks Programming Mode: Quasi-dynamic Group 2 and Group 4
15	RO	0x0	reserved
14:8	RW	0x1b	t_ras_max tRAS(max): Maximum time between activate and precharge to same bank. This is the maximum time that a page can be kept open Minimum value of this register is 1. Zero is invalid. When the controller is operating in 1:2 frequency ratio mode, program this to (tRAS(max)-1)/2. No rounding up. Unit: Multiples of 1024 DFI clocks. Programming Mode: Quasi-dynamic Group 2 and Group 4

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Bit	Attr	Reset Value	Description
7:6	RO	0x0	reserved
5:0	RW	0x0f	t_ras_min tRAS(min): Minimum time between activate and precharge to the same bank. When the controller is operating in 1:2 frequency mode, 1T mode, program this to tRAS(min)/2. No rounding up. When the controller is operating in 1:2 frequency ratio mode, 2T mode or LPDDR4 mode, program this to (tRAS(min)/2) and round it up to the next integer value. Unit: DFI Clocks Programming Mode: Quasi-dynamic Group 2 and Group 4

DDRC_DRAMTMG1

Address: Operational Base + offset (0x0104)

Bit	Attr	Reset Value	Description
31:21	RO	0x0	reserved
20:16	RW	0x08	t_xp tXP: Minimum time after power-down exit to any operation. For DDR3, this should be programmed to tXPDLL if slow powerdown exit is selected in MR0[12]. If C/A parity for DDR4 is used, set to (tXP+PL) instead. If LPDDR4 is selected and its spec has tCKELPD parameter, set to the larger of tXP and tCKELPD instead. When the controller is operating in 1:2 frequency ratio mode, program this to (tXP/2) and round it up to the next integer value. Units: DFI Clocks Programming Mode: Quasi-dynamic Group 2 and Group 4
15:14	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
13:8	RW	0x04	rd2pre tRTP: Minimum time from read to precharge of same bank. DDR2: tAL + BL/2 + max(tRTP, 2) - 2 DDR3: tAL + max (tRTP, 4) DDR4: Max of following two equations: tAL + max (tRTP, 4) or, RL + BL/2 - tRP (*). mDDR: BL/2 LPDDR2: Depends on if it's LPDDR2-S2 or LPDDR2-S4: LPDDR2-S2: BL/2 + tRTP - 1. LPDDR2-S4: BL/2 + max(tRTP,2) - 2. LPDDR3: BL/2 + max(tRTP,4) - 4 LPDDR4: BL/2 + max(tRTP,8) - 8 (*) When both DDR4 SDRAM and ST-MRAM are used simultaneously, use SDRAM's tRP value for calculation. When the controller is operating in 1:2 mode, 1T mode, divide the above value by 2. No rounding up. When the controller is operating in 1:2 mode, 2T mode or LPDDR4 mode, divide the above value by 2 and round it up to the next integer value. Unit: DFI Clocks. Programming Mode: Quasi-dynamic Group 1 and Group 2 and Group 4
7	RO	0x0	reserved
6:0	RW	0x14	t_rc tRC: Minimum time between activates to same bank. When the controller is operating in 1:2 frequency ratio mode, program this to (tRC/2) and round up to next integer value. Unit: DFI Clocks. Programming Mode: Quasi-dynamic Group 2 and Group 4

DDRC_DRAMTMG2

Address: Operational Base + offset (0x0108)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
29:24	RW	0x03	write_latency Set to WL. Time from write command to write data on SDRAM interface. For mDDR, it should normally be set to 1. When the controller is operating in 1:2 frequency ratio mode, divide the value calculated using the above equation by 2, and round it up to next integer. This register field is not required for DDR2 and DDR3 (except if MEMC_TRAINING is set), as the DFI read and write latencies defined in DFITMG0 and DFITMG1 are sufficient for those protocols Unit: DFI clocks Programming Mode: Quasi-dynamic Group 1 and Group 2 and Group 4
23:22	RO	0x0	reserved
21:16	RW	0x05	read_latency Set to RL. Time from read command to read data on SDRAM interface. When the controller is operating in 1:2 frequency ratio mode, divide the value calculated using the above equation by 2, and round it up to next integer. This register field is not required for DDR2 and DDR3 (except if MEMC_TRAINING is set), as the DFI read and write latencies defined in DFITMG0 and DFITMG1 are sufficient for those protocols Unit: DFI clocks Programming Mode: Quasi-dynamic Group 1 and Group 2 and Group 4
15:14	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
13:8	RW	0x06	rd2wr DDR2/3/mDDR: RL + BL/2 + 2 - WL DDR4: RL + BL/2 + 1 + WR_PREAMBLE - WL LPDDR2/LPDDR3: RL + BL/2 + RU(tDQSCKmax/tCK) + 1 - WL LPDDR4(DQ ODT is Disabled): RL + BL/2 + RU(tDQSCKmax/tCK) + WR_PREAMBLE + RD_POSTAMBLE - WL LPDDR4(DQ ODT is Enabled) : RL + BL/2 + RU(tDQSCKmax/tCK) + RD_POSTAMBLE - ODTLon - RU(tODTon(min)/tCK) Minimum time from read command to write command. Include time for bus turnaround and all per-bank, per-rank, and global constraints. Please see the relevant PHY databook for details of what should be included here. Unit: DFI Clocks. Where: WL = write latency BL = burst length. This must match the value programmed in the BL bit of the mode register to the SDRAM RL = read latency = CAS latency WR_PREAMBLE = write preamble. This is unique to DDR4 and LPDDR4. RD_POSTAMBLE = read postamble. This is unique to LPDDR4. For LPDDR2/LPDDR3/LPDDR4, if derating is enabled (DERATEEN.derate_enable=1), derated tDQSCKmax should be used. When the controller is operating in 1:2 frequency ratio mode, divide the value calculated using the above equation by 2, and round it up to next integer. Programming Mode: Quasi-dynamic Group 1 and Group 2 and Group 4
7:6	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
5:0	RW	0x0d	wr2rd DDR4: CWL + PL + BL/2 + tWTR_L LPDDR2/3/4: WL + BL/2 + tWTR + 1 Others: CWL + BL/2 + tWTR In DDR4, minimum time from write command to read command for same bank group. In others, minimum time from write command to read command. Includes time for bus turnaround, recovery times, and all per-bank, per-rank, and global constraints. Unit: DFI Clocks. Where: CWL = CAS write latency WL = Write latency PL = Parity latency BL = burst length. This must match the value programmed in the BL bit of the mode register to the SDRAM tWTR_L = internal write to read command delay for same bank group. This comes directly from the SDRAM specification. tWTR = internal write to read command delay. This comes directly from the SDRAM specification. Add one extra cycle for LPDDR2/LPDDR3/LPDDR4 operation. When the controller is operating in 1:2 mode, divide the value calculated using the above equation by 2, and round it up to next integer. Programming Mode: Quasi-dynamic Group 1 and Group 2 and Group 4

DDRC_DRAMTMG3

Address: Operational Base + offset (0x010c)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved

Bit	Attr	Reset Value	Description
29:20	RW	0x005	t_mrw Time to wait after a mode register write or read (MRW or MRR). Present only in designs configured to support LPDDR2, LPDDR3 or LPDDR4. LPDDR2 typically requires value of 5. LPDDR3 typically requires value of 10. LPDDR4: Set this to the larger of tMRW and tMRWCKEL. For LPDDR2, this register is used for the time from a MRW/MRR to all other commands. When the controller is operating in 1:2 frequency ratio mode, program this to the above values divided by 2 and round it up to the next integer value. For LDPDR3, this register is used for the time from a MRW/MRR to a MRW/MRR. Programming Mode: Quasi-dynamic Group 2 and Group 4
19:18	RO	0x0	reserved
17:12	RW	0x04	t_mrd tMRD: Cycles to wait after a mode register write or read. Depending on the connected SDRAM, tMRD represents: DDR2/mDDR: Time from MRS to any command DDR3/4: Time from MRS to MRS command LPDDR2: not used LPDDR3/4: Time from MRS to non-MRS command. When the controller is operating in 1:2 frequency ratio mode, program this to (tMRD/2) and round it up to the next integer value. If C/A parity for DDR4 is used, set to tMRD_PAR(tMOD+PL) instead. Programming Mode: Quasi-dynamic Group 2 and Group 4
11:10	RO	0x0	reserved
9:0	RW	0x00c	t_mod tMOD: Parameter used only in DDR3 and DDR4. Cycles between load mode command and following non-load mode command. If C/A parity for DDR4 is used, set to tMOD_PAR(tMOD+PL) instead. If MPR writes for DDR4 are used, set to tMOD + AL (or tMPD_PAR + AL if C/A parity is also used). Set to tMOD/2 (rounded up to next integer) if controller is operating in 1:2 frequency ratio mode. Programming Mode: Quasi-dynamic Group 2 and Group 4

DDRC_DRAMTMG4

Address: Operational Base + offset (0x0110)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved

Bit	Attr	Reset Value	Description
28:24	RW	0x05	t_rcd tRCD - tAL: Minimum time from activate to read or write command to same bank. When the controller is operating in 1:2 frequency ratio mode, program this to ((tRCD - tAL)/2) and round it up to the next integer value. Minimum value allowed for this register is 1, which implies minimum (tRCD - tAL) value to be 2 when the controller is operating in 1:2 frequency ratio mode. Unit: DFI Clocks. Programming Mode: Quasi-dynamic Group 1 and Group 2 and Group 4
23:20	RO	0x0	reserved
19:16	RW	0x4	t_ccd DDR4: tCCD_L: This is the minimum time between two reads or two writes for same bank group. Others: tCCD: This is the minimum time between two reads or two writes. When the controller is operating in 1:2 frequency ratio mode, program this to (tCCD_L/2 or tCCD/2) and round it up to the next integer value. Unit: DFI clocks. Programming Mode: Quasi-dynamic Group 2 and Group 4
15:12	RO	0x0	reserved
11:8	RW	0x4	t_rrd DDR4: tRRD_L: Minimum time between activates from bank "a" to bank "b" for same bank group. Others: tRRD: Minimum time between activates from bank "a" to bank "b" When the controller is operating in 1:2 frequency ratio mode, program this to (tRRD_L/2 or tRRD/2) and round it up to the next integer value. Unit: DFI Clocks. Programming Mode: Quasi-dynamic Group 2 and Group 4
7:5	RO	0x0	reserved
4:0	RW	0x05	t_rp tRP: Minimum time from precharge to activate of same bank. When the controller is operating in 1:2 frequency ratio mode, t_rp should be set to RoundDown(RoundUp(tRP/tCK)/2) + 1. When the controller is operating in 1:2 frequency ratio mode in LPDDR4, t_rp should be set to RoundUp(RoundUp(tRP/tCK)/2). Unit: DFI Clocks. Programming Mode: Quasi-dynamic Group 2 and Group 4

DDRC_DRAMTMG5

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Address: Operational Base + offset (0x0114)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:24	RW	0x5	t_cksrx This is the time before Self Refresh Exit that CK is maintained as a valid clock before issuing SRX. Specifies the clock stable time before SRX. Recommended settings: mDDR: 1 LPDDR2: 2 LPDDR3: 2 LPDDR4: tCKCKEH DDR2: 1 DDR3: tCKSRX DDR4: tCKSRX When the controller is operating in 1:2 frequency ratio mode, program this to recommended value divided by two and round it up to next integer. Programming Mode: Quasi-dynamic Group 2 and Group 4
23:20	RO	0x0	reserved
19:16	RW	0x5	t_cksre This is the time after Self Refresh Down Entry that CK is maintained as a valid clock. Specifies the clock disable delay after SRE. Recommended settings: mDDR: 0 LPDDR2: 2 LPDDR3: 2 LPDDR4: tCKELCK DDR2: 1 DDR3: max (10 ns, 5 tCK) DDR4: max (10 ns, 5 tCK) (+ PL(parity latency)(*)) (*)Only if CRCPARCTL1.caparity_disable_before_sr=0, this register should be increased by PL. When the controller is operating in 1:2 frequency ratio mode, program this to recommended value divided by two and round it up to next integer. Programming Mode: Quasi-dynamic Group 2 and Group 4
15:14	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
13:8	RW	0x04	t_ckesr Minimum CKE low width for Self refresh or Self refresh power down entry to exit timing in memory clock cycles. Recommended settings: mDDR: tRFC LPDDR2: tCKESR LPDDR3: tCKESR LPDDR4: max(tCKE, tSR) DDR2: tCKE DDR3: tCKE + 1 DDR4: tCKE + 1 (+ PL(parity latency)(*)) (*)Only if CRCPARCTL1.caparity_disable_before_sr=0, this register should be increased by PL. When the controller is operating in 1:2 frequency ratio mode, program this to recommended value divided by two and round it up to next integer. Programming Mode: Quasi-dynamic Group 2 and Group 4
7:5	RO	0x0	reserved
4:0	RW	0x03	t_cke Minimum number of cycles of CKE HIGH/LOW during power-down and self refresh. LPDDR2/LPDDR3 mode: Set this to the larger of tCKE or tCKESR LPDDR4 mode: Set this to the larger of tCKE or tSR. Non-LPDDR2/non-LPDDR3/non-LPDDR4 designs: Set this to tCKE value. When the controller is operating in 1:2 frequency ratio mode, program this to (value described above)/2 and round it up to the next integer value. Unit: DFI Clocks. Programming Mode: Quasi-dynamic Group 2 and Group 4

DDRC_DRAMTMG6

Address: Operational Base + offset (0x0118)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved

Bit	Attr	Reset Value	Description
27:24	RW	0x2	t_ckdpde This is the time before Self Refresh Exit that CK is maintained as a valid clock before issuing SRX. Specifies the clock stable time before SRX. Recommended settings: mDDR: 1 LPDDR2: 2 LPDDR3: 2 LPDDR4: tCKCKEH DDR2: 1 DDR3: tCKSRX DDR4: tCKSRX When the controller is operating in 1:2 frequency ratio mode, program this to recommended value divided by two and round it up to next integer. Programming Mode: Quasi-dynamic Group 2 and Group 4
23:20	RO	0x0	reserved
19:16	RW	0x2	t_ckdpdx This is the time before Deep Power Down Exit that CK is maintained as a valid clock before issuing DPDX. Specifies the clock stable time before DPDX. Recommended settings: mDDR: 1 LPDDR2: 2 LPDDR3: 2 When the controller is operating in 1:2 frequency ratio mode, program this to recommended value divided by two and round it up to next integer. This is only present for designs supporting mDDR or LPDDR2 devices. Programming Mode: Quasi-dynamic Group 2 and Group 4
15:4	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
3:0	RW	0x5	t_ckcsx This is the time before Clock Stop Exit that CK is maintained as a valid clock before issuing Clock Stop Exit. Specifies the clock stable time before next command after Clock Stop Exit. Recommended settings: mDDR: 1 LPDDR2: tXP + 2 LPDDR3: tXP + 2 LPDDR4: tXP + 2 When the controller is operating in 1:2 frequency ratio mode, program this to recommended value divided by two and round it up to next integer. This is only present for designs supporting mDDR or LPDDR2/LPDDR3/LPDDR4 devices. Programming Mode: Quasi-dynamic Group 2 and Group 4

DDRC_DRAMTMG7

Address: Operational Base + offset (0x011c)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:8	RW	0x2	t_ckpde This is the time after Power Down Entry that CK is maintained as a valid clock. Specifies the clock disable delay after PDE. Recommended settings: mDDR: 0 LPDDR2: 2 LPDDR3: 2 LPDDR4: tCKELCK When using DDR2/3/4 SDRAM, this register should be set to the same value as DRAMTMG5.t_cksre. When the controller is operating in 1:2 frequency ratio mode, program this to recommended value divided by two and round it up to next integer. This is only present for designs supporting mDDR or LPDDR2/LPDDR3/LPDDR4 devices. Programming Mode: Quasi-dynamic Group 2 and Group 4
7:4	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
3:0	RW	0x2	t_ckpdx This is the time before Power Down Exit that CK is maintained as a valid clock before issuing PDX. Specifies the clock stable time before PDX. Recommended settings: mDDR: 0 LPDDR2: 2 LPDDR3: 2 LPDDR4: 2 When using DDR2/3/4 SDRAM, this register should be set to the same value as DRAMTMG5.t_cksrx. When the controller is operating in 1:2 frequency ratio mode, program this to recommended value divided by two and round it up to next integer. This is only present for designs supporting mDDR or LPDDR2/LPDDR3/LPDDR4 devices. Programming Mode: Quasi-dynamic Group 2 and Group 4

DDRC_DRAMTMG8

Address: Operational Base + offset (0x0120)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x03	t_xs_fast_x32 tXS_FAST: Exit Self Refresh to ZQCL, ZQCS and MRS (only CL, WR, RTP and Geardown mode). When the controller is operating in 1:2 frequency ratio mode, program this to the above value divided by 2 and round up to next integer value. Unit: Multiples of 32 DFI clocks. Note: This is applicable to only ZQCL/ZQCS commands. Note: Ensure this is less than or equal to t_xs_x32. Programming Mode: Quasi-dynamic Group 2 and Group 4
23	RO	0x0	reserved
22:16	RW	0x03	t_xs_abort_x32 tXS_ABORT: Exit Self Refresh to commands not requiring a locked DLL in Self Refresh Abort. When the controller is operating in 1:2 frequency ratio mode, program this to the above value divided by 2 and round up to next integer value. Unit: Multiples of 32 DFI clocks. Note: Ensure this is less than or equal to t_xs_x32. Programming Mode: Quasi-dynamic Group 2 and Group 4
15	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
14:8	RW	0x44	t_xs_dll_x32 tXSDLL: Exit Self Refresh to commands requiring a locked DLL. When the controller is operating in 1:2 frequency ratio mode, program this to the above value divided by 2 and round up to next integer value. Unit: Multiples of 32 DFI clocks. Note: Used only for DDR2, DDR3 and DDR4 SDRAMs. Programming Mode: Quasi-dynamic Group 2 and Group 4
7	RO	0x0	reserved
6:0	RW	0x05	t_xs_x32 tXS: Exit Self Refresh to commands not requiring a locked DLL. When the controller is operating in 1:2 frequency ratio mode, program this to the above value divided by 2 and round up to next integer value. Unit: Multiples of 32 DFI clocks. Note: Used only for DDR2, DDR3 and DDR4 SDRAMs. Programming Mode: Quasi-dynamic Group 2 and Group 4

DDRC_DRAMTMG9

Address: Operational Base + offset (0x0124)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RW	0x0	ddr4_wr_preamble DDR4 Write preamble mode 0: 1tCK preamble 1: 2tCK preamble Programming Mode: Quasi-dynamic Group 2 and Group 4
29:19	RO	0x0	reserved
18:16	RW	0x4	t_ccd_s tCCD_S: This is the minimum time between two reads or two writes for different bank group. For bank switching (from bank "a" to bank "b"), the minimum time is this value + 1. When the controller is operating in 1:2 frequency ratio mode, program this to (tCCD_S/2) and round it up to the next integer value. Present only in designs configured to support DDR4. Unit: DFI clocks. Programming Mode: Quasi-dynamic Group 2 and Group 4
15:12	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
11:8	RW	0x4	t_rrd_s tRRD_S: Minimum time between activates from bank "a" to bank "b" for different bank group. When the controller is operating in 1:2 frequency ratio mode, program this to (tRRD_S/2) and round it up to the next integer value. Present only in designs configured to support DDR4. Unit: DFI Clocks. Programming Mode: Quasi-dynamic Group 2 and Group 4
7:6	RO	0x0	reserved
5:0	RW	0x0d	wr2rd_s CWL + PL + BL/2 + tWTR_S Minimum time from write command to read command for different bank group. Includes time for bus turnaround, recovery times, and all per-bank, per-rank, and global constraints. Present only in designs configured to support DDR4. Unit: DFI Clocks. Where: CWL = CAS write latency PL = Parity latency BL = burst length. This must match the value programmed in the BL bit of the mode register to the SDRAM tWTR_S = internal write to read command delay for different bank group. This comes directly from the SDRAM specification. When the controller is operating in 1:2 mode, divide the value calculated using the above equation by 2, and round it up to next integer. Programming Mode: Quasi-dynamic Group 1 and Group 2 and Group 4

DDRC_DRAMTMG10

Address: Operational Base + offset (0x0128)

Bit	Attr	Reset Value	Description
31:21	RO	0x0	reserved

Bit	Attr	Reset Value	Description
20:16	RW	0x1c	t_sync_gear Indicates the time between MRS command and the sync pulse time. This must be even number of clocks. For DDR4-2666 and DDR4-3200, this parameter is defined as tMOD(min)+4nCK tMOD(min) is greater of 24nCK or 15ns 15ns / .625ns = 24 Max value for this register is 24+4 = 28 When the controller is operating in 1:2 mode, program this to (tSYNC_GEAR/2) and round it up to the next integer value. Unit: DFI Clocks Programming Mode: Quasi-dynamic Group 2 and Group 4
15:13	RO	0x0	reserved
12:8	RW	0x18	t_cmd_gear Sync pulse to first valid command. For DDR4-2666 and DDR4-3200, this parameter is defined as tMOD(min). tMOD(min) is greater of 24nCK or 15ns 15ns / .625ns = 24 Max value for this register is 24 When the controller is operating in 1:2 mode, program this to (tCMD_GEAR/2) and round it up to the next integer value. Unit: DFI Clocks Programming Mode: Quasi-dynamic Group 2 and Group 4
7:4	RO	0x0	reserved
3:2	RW	0x2	t_gear_setup Geardown setup time. Minimum value of this register is 1. Zero is invalid. For DDR4-2666 and DDR4-3200, this parameter is defined as 2 clks When the controller is operating in 1:2 frequency ratio mode, program this to (tGEAR_setup/2) and round it up to the next integer value. Unit: DFI Clocks Programming Mode: Quasi-dynamic Group 2 and Group 4
1:0	RW	0x2	t_gear_hold Geardown hold time. Minimum value of this register is 1. Zero is invalid. For DDR4-2666 and DDR4-3200, this parameter is defined as 2 clks When the controller is operating in 1:2 frequency ratio mode, program this to (tGEAR_hold/2) and round it up to the next integer value. Unit: DFI Clocks Value After Reset: 0x2 Programming Mode: Quasi-dynamic Group 2 and Group 4

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DDRC_DRAMTMG11

Address: Operational Base + offset (0x012c)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x44	post_mpsm_gap_x32 tXMPDLL: This is the minimum Exit MPSM to commands requiring a locked DLL. When the controller is operating in 1:2 frequency ratio mode, program this to (tXMPDLL/2) and round it up to the next integer value. Present only in designs configured to support DDR4. Unit: Multiples of 32 DFI clocks. Programming Mode: Quasi-dynamic Group 2 and Group 4
23:21	RO	0x0	reserved
20:16	RW	0x0c	t_mpx_lh tMPX_LH: This is the minimum CS_n Low hold time to CKE rising edge. When the controller is operating in 1:2 frequency ratio mode, program this to RoundUp(tMPX_LH/2)+1. Present only in designs configured to support DDR4. Unit: DFI clocks. Programming Mode: Quasi-dynamic Group 2 and Group 4
15:10	RO	0x0	reserved
9:8	RW	0x2	t_mpx_s tMPX_S: Minimum time CS setup time to CKE. When the controller is operating in 1:2 frequency ratio mode, program this to (tMPX_S/2) and round it up to the next integer value. Present only in designs configured to support DDR4. Unit: DFI Clocks. Programming Mode: Quasi-dynamic Group 2 and Group 4
7:5	RO	0x0	reserved
4:0	RW	0x1c	t_ckmpe tCKMPE: Minimum valid clock requirement after MPSM entry. Present only in designs configured to support DDR4. Unit: DFI Clocks. When the controller is operating in 1:2 frequency ratio mode, divide the value calculated using the above equation by 2, and round it up to next integer. Programming Mode: Quasi-dynamic Group 2 and Group 4

DDRC_DRAMTMG12

Address: Operational Base + offset (0x0130)

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Bit	Attr	Reset Value	Description
31:18	RO	0x0	reserved
17:16	RW	0x2	t_cmdcke tCMDCKE: Delay from valid command to CKE input LOW. Set this to the larger of tESCKE or tCMDCKE When the controller is operating in 1:2 frequency ratio mode, program this to (max(tESCKE, tCMDCKE)/2) and round it up to the next integer value. Programming Mode: Quasi-dynamic Group 2 and Group 4
15:5	RO	0x0	reserved
4:0	RW	0x10	t_mrd_pda tMRD_PDA: This is the Mode Register Set command cycle time in PDA mode. When the controller is operating in 1:2 frequency ratio mode, program this to (tMRD_PDA/2) and round it up to the next integer value. Programming Mode: Quasi-dynamic Group 2 and Group 4

DDRC_DRAMTMG13

Address: Operational Base + offset (0x0134)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x1c	odtloff LPDDR4: tODTLoff: This is the latency from CAS-2 command to tODToff reference. When the controller is operating in 1:2 frequency ratio mode, program this to (tODTLoff/2) and round it up to the next integer value. Unit: DFI Clocks. Programming Mode: Quasi-dynamic Group 2 and Group 4
23:22	RO	0x0	reserved
21:16	RW	0x20	t_ccd_mw LPDDR4: tCCDMW: This is the minimum time from write or masked write to masked write command for same bank. When the controller is operating in 1:2 frequency ratio mode, program this to (tCCDMW/2) and round it up to the next integer value. Unit: DFI Clocks. Programming Mode: Quasi-dynamic Group 2 and Group 4
15:3	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
2:0	RW	0x4	t_ppd LPDDR4: tPPD: This is the minimum time from precharge to precharge command. When the controller is operating in 1:2 frequency ratio mode, program this to (tPPD/2) and round it up to the next integer value. Unit: DFI Clocks. Programming Mode: Quasi-dynamic Group 2 and Group 4

DDRC_DRAMTMG14

Address: Operational Base + offset (0x0138)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0x0a0	t_xsr tXSR: Exit Self Refresh to any command. When the controller is operating in 1:2 frequency ratio mode, program this to the above value divided by 2 and round up to next integer value. Note: Used only for mDDR/LPDDR2/LPDDR3/LPDDR4 mode. Programming Mode: Quasi-dynamic Group 2 and Group 4

DDRC_DRAMTMG15

Address: Operational Base + offset (0x013c)

Bit	Attr	Reset Value	Description
31	RW	0x0	en_dfi_lp_t_stab 1: Enable using tSTAB when exiting DFI LP. Needs to be set when the PHY is stopping the clock during DFI LP to save maximum power. 0: Disable using tSTAB when exiting DFI LP Programming Mode: Quasi-dynamic Group 2 and Group 4
30:8	RO	0x0	reserved
7:0	RW	0x00	t_stab_x32 tSTAB: Stabilization time. It is required in the following two cases for DDR3/DDR4 RDIMM : when exiting power saving mode, if the clock was stopped, after re-enabling it the clock must be stable for a time specified by tSTAB in the case of input clock frequency change (DDR4) after issuing control words that refers to clock timing (Specification: 6us for DDR3, 5us for DDR4) When the controller is operating in 1:2 frequency ratio mode, program this to recommended value divided by two and round it up to next integer. Unit: Multiples of 32 DFI clock cycles. Programming Mode: Quasi-dynamic Group 2 and Group 4

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DDRC_DRAMTMG17

Address: Operational Base + offset (0x0144)

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:16	RW	0x00	t_vrcg_enable LPDDR4: tVRCG_ENABLE: VREF high current mode enable time. When the controller is operating in 1:2 frequency ratio mode, program this to (tVRCG_ENABLE/2) and round it up to the next integer value. Unit: DFI clocks Programming Mode: Quasi-dynamic Group 4
15:7	RO	0x0	reserved
6:0	RW	0x00	t_vrcg_disable LPDDR4: tVRCG_ENABLE: VREF high current mode disable time. When the controller is operating in 1:2 frequency ratio mode, program this to (tVRCG_DISABLE/2) and round it up to the next integer value. Unit: DFI clocks Programming Mode: Quasi-dynamic Group 4

DDRC_ZQCTL0

Address: Operational Base + offset (0x0180)

Bit	Attr	Reset Value	Description
31	RW	0x0	dis_auto_zq 1: Disable uMCTL2 generation of ZQCS/MPC(ZQ calibration) command. Register DBGCMD.zq_calib_short can be used instead to issue ZQ calibration request from APB module. 0: Internally generate ZQCS/MPC(ZQ calibration) commands based on ZQCTL1.t_zq_short_interval_x1024. This is only present for designs supporting DDR3/DDR4 or LPDDR2/LPDDR3/LPDDR4 devices. Programming Mode: Dynamic
30	RW	0x0	dis_srx_zqcl 1: Disable issuing of ZQCL/MPC(ZQ calibration) command at Self-Refresh/SR-Powerdown exit. Only applicable when run in DDR3 or DDR4 or LPDDR2 or LPDDR3 or LPDDR4 mode. 0: Enable issuing of ZQCL/MPC(ZQ calibration) command at Self-Refresh/SR-Powerdown exit. Only applicable when run in DDR3 or DDR4 or LPDDR2 or LPDDR3 or LPDDR4 mode. This is only present for designs supporting DDR3/DDR4 or LPDDR2/LPDDR3/LPDDR4 devices. Programming Mode: Quasi-dynamic Group 2 and Group 4

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Bit	Attr	Reset Value	Description
29	RW	0x0	zq_resistor_shared 1: Denotes that ZQ resistor is shared between ranks. Means ZQinit/ZQCL/ZQCS/MPC(ZQ calibration) commands are sent to one rank at a time with tZQinit/tZQCL/tZQCS/tZQCAL/tZQLAT timing met between commands so that commands to different ranks do not overlap. 0: ZQ resistor is not shared. This is only present for designs supporting DDR3/DDR4 or LPDDR2/LPDDR3/LPDDR4 devices. Programming Mode: Static
28	RW	0x0	dis_mpsmx_zqcl 1: Disable issuing of ZQCL command at Maximum Power Saving Mode exit. Only applicable when run in DDR4 mode. 0: Enable issuing of ZQCL command at Maximum Power Saving Mode exit. Only applicable when run in DDR4 mode. This is only present for designs supporting DDR4 devices. Note: Do not issue ZQCL command at Maximum Power Save Mode exit if the UMCTL2_SHARED_AC configuration parameter is set. Program it to 1'b1. The software can send ZQCS after exiting MPSM mode. Programming Mode: Static
27	RO	0x0	reserved
26:16	RW	0x200	t_zq_long_nop tZQoper for DDR3/DDR4, tZQCL for LPDDR2/LPDDR3, tZQCAL for LPDDR4: Number of DFI clock cycles of NOP required after a ZQCL (ZQ calibration long)/MPC(ZQ Start) command is issued to SDRAM. When the controller is operating in 1:2 frequency ratio mode: DDR3/DDR4: program this to tZQoper/2 and round it up to the next integer value. LPDDR2/LPDDR3: program this to tZQCL/2 and round it up to the next integer value. LPDDR4: program this to tZQCAL/2 and round it up to the next integer value. This is only present for designs supporting DDR3/DDR4 or LPDDR2/LPDDR3/LPDDR4 devices. Programming Mode: Static
15:10	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
9:0	RW	0x040	t_zq_short_nop tZQCS for DDR3/DD4/LPDDR2/LPDDR3, tZQLAT for LPDDR4: Number of DFI clock cycles of NOP required after a ZQCS (ZQ calibration short)/MPC(ZQ Latch) command is issued to SDRAM. When the controller is operating in 1:2 frequency ratio mode, program this to tZQCS/2 and round it up to the next integer value. This is only present for designs supporting DDR3/DDR4 or LPDDR2/LPDDR3/LPDDR4 devices. Programming Mode: Static

DDRC_ZQCTL1

Address: Operational Base + offset (0x0184)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x020	t_zq_reset_nop tZQReset: Number of DFI clock cycles of NOP required after a ZQReset (ZQ calibration Reset) command is issued to SDRAM. When the controller is operating in 1:2 frequency ratio mode, program this to tZQReset/2 and round it up to the next integer value. This is only present for designs supporting LPDDR2/LPDDR3/LPDDR4 devices. Programming Mode: Static
19:0	RW	0x00100	t_zq_short_interval_x1024 Average interval to wait between automatically issuing ZQCS (ZQ calibration short)/MPC(ZQ calibration) commands to DDR3/DDR4/LPDDR2/LPDDR3/LPDDR4 devices. Meaningless, if ZQCTL0.dis_auto_zq=1. Unit: 1024 DFI clock cycles. This is only present for designs supporting DDR3/DDR4 or LPDDR2/LPDDR3/LPDDR4 devices. Programming Mode: Static

DDRC_ZQCTL2

Address: Operational Base + offset (0x0188)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
0	RW	0x0	zq_reset Setting this register bit to 1 triggers a ZQ Reset operation. When the ZQ Reset operation is complete, the uMCTL2 automatically clears this bit. It is recommended NOT to set this signal if in Init, Self-Refresh(except LPDDR4) or SRPowerdown(LPDDR4) or Deep power-down operating modes. This is only present for designs supporting LPDDR2/LPDDR3/LPDDR4 devices. Programming Mode: Dynamic

DDRC_ZQSTAT

Address: Operational Base + offset (0x018c)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	zq_reset_busy SoC core may initiate a ZQ Reset operation only if this signal is low. This signal goes high in the clock after the uMCTL2 accepts the ZQ Reset request. It goes low when the ZQ Reset command is issued to the SDRAM and the associated NOP period is over. It is recommended not to perform ZQ Reset commands when this signal is high. 0: Indicates that the SoC core can initiate a ZQ Reset operation 1: Indicates that ZQ Reset operation is in progress Programming Mode: Dynamic

DDRC_DFITMG0

Address: Operational Base + offset (0x0190)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	RW	0x07	dfi_t_ctrl_delay Specifies the number of DFI clock cycles after an assertion or de-assertion of the DFI control signals that the control signals at the PHY-DRAM interface reflect the assertion or de-assertion. If the DFI clock and the memory clock are not phase-aligned, this timing parameter should be rounded up to the next integer value. Programming Mode: Quasi-dynamic Group 4

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Bit	Attr	Reset Value	Description
23	RW	0x0	dfi_rddata_use_dfi_phy_clk Defines whether dfi_rddata_en/dfi_rddata/dfi_rddata_valid is generated using HDR (DFI clock) or SDR (DFI PHY clock) values. Selects whether value in DFITMG0.dfi_t_rddata_en is in terms of HDR (DFI clock) or SDR (DFI PHY clock) cycles: 0: in terms of HDR (DFI clock) cycles, Only support HDR DFI clock. 1: in terms of SDR (DFI PHY clock) cycles Programming Mode: Static
22:16	RW	0x02	dfi_t_rddata_en Time from the assertion of a read command on the DFI interface to the assertion of the dfi_rddata_en signal. Refer to PHY specification for correct value. This corresponds to the DFI parameter trddata_en. Unit: DFI clock cycles Programming Mode: Quasi-dynamic Group 1 and Group 4
15	RW	0x0	dfi_wrdata_use_dfi_phy_clk Defines whether dfi_wrdata_en/dfi_wrdata/dfi_wrdata_mask is generated using HDR (DFI clock) or SDR (DFI PHY clock) values Selects whether value in DFITMG0.dfi_tphy_wrlat is in terms of HDR (DFI clock) or SDR (DFI PHY clock) cycles Selects whether value in DFITMG0.dfi_tphy_wrdata is in terms of HDR (DFI clock) or SDR (DFI PHY clock) cycles 0: in terms of HDR (DFI clock) cycles, Only support HDR DFI clock. 1: in terms of SDR (DFI PHY clock) cycles Programming Mode: Static
14	RO	0x0	reserved
13:8	RW	0x00	dfi_tphy_wrdata Specifies the number of clock cycles between when dfi_wrdata_en is asserted to when the associated write data is driven on the dfi_wrdata signal. This corresponds to the DFI timing parameter tphy_wrdata. Refer to PHY specification for correct value. Note, max supported value is 8. Unit: DFI clock cycles. Programming Mode: Quasi-dynamic Group 4
7:6	RO	0x0	reserved
5:0	RW	0x02	dfi_tphy_wrlat Write latency Number of clocks from the write command to write data enable (dfi_wrdata_en). This corresponds to the DFI timing parameter tphy_wrlat. Refer to PHY specification for correct value. For LPDDR4, dfi_tphy_wrlat>60 is not supported. Unit: DFI clock cycles Programming Mode: Quasi-dynamic Group 1 and Group 4

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DDRC_DFITMG1

Address: Operational Base + offset (0x0194)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	dfi_t_cmd_lat Specifies the number of DFI PHY clock cycles between when the dfi_cs signal is asserted and when the associated command is driven. This field is used for CAL mode, should be set to '0' or the value which matches the CAL mode register setting in the DRAM. If the PHY can add the latency for CAL mode, this should be set to '0'. Valid Range: 0, 3, 4, 5, 6, and 8 Programming Mode: Quasi-dynamic Group 2 and Group 4
27:26	RO	0x0	reserved
25:24	RW	0x0	dfi_t_parin_lat Specifies the number of DFI PHY clock cycles between when the dfi_cs signal is asserted and when the associated dfi_parity_in signal is driven. Programming Mode: Quasi-dynamic Group 4
23:21	RO	0x0	reserved
20:16	RW	0x00	dfi_t_wrdata_delay Specifies the number of DFI clock cycles between when the dfi_wrdata_en signal is asserted and when the corresponding write data transfer is completed on the DRAM bus. This corresponds to the DFI timing parameter twrdata_delay. Refer to PHY specification for correct value. Value to be programmed is in terms of DFI clocks, not PHY clocks. In FREQ_RATIO=2, divide PHY's value by 2 and round up to next integer. Programming Mode: Quasi-dynamic Group 4
15:13	RO	0x0	reserved
12:8	RW	0x04	dfi_t_dram_clk_disable Specifies the number of DFI clock cycles from the assertion of the dfi_dram_clk_disable signal on the DFI until the clock to the DRAM memory devices, at the PHY-DRAM boundary, maintains a low value. If the DFI clock and the memory clock are not phase aligned, this timing parameter should be rounded up to the next integer value. Programming Mode: Quasi-dynamic Group 4
7:5	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
4:0	RW	0x04	dfi_t_dram_clk_enable Specifies the number of DFI clock cycles from the deassertion of the dfi_dram_clk_disable signal on the DFI until the first valid rising edge of the clock to the DRAM memory devices, at the PHY-DRAM boundary. If the DFI clock and the memory clock are not phase aligned, this timing parameter should be rounded up to the next integer value. Programming Mode: Quasi-dynamic Group 4

DDRC_DFILPCFG0

Address: Operational Base + offset (0x0198)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	RW	0x07	dfi_tlp_resp Setting in DFI clock cycles for DFI's tlp_resp time. Same value is used for both Power Down, Self Refresh, Deep Power Down and Maximum Power Saving modes. DFI 2.1 specification onwards, recommends using a fixed value of 7 always. Programming Mode: Static
23:20	RW	0x0	dfi_lp_wakeup_dpd Value in DFI clock cycles to drive on dfi_lp_wakeup signal when Deep Power Down mode is entered. Determines the DFI's tlp_wakeup time: 0x0 - 16 cycles 0x1 - 32 cycles 0x2 - 64 cycles 0x3 - 128 cycles 0x4 - 256 cycles 0x5 - 512 cycles 0x6 - 1024 cycles 0x7 - 2048 cycles 0x8 - 4096 cycles 0x9 - 8192 cycles 0xA - 16384 cycles 0xB - 32768 cycles 0xC - 65536 cycles 0xD - 131072 cycles 0xE - 262144 cycles 0xF - Unlimited This is only present for designs supporting mDDR or LPDDR2/LPDDR3 devices. Programming Mode: Static
19:17	RO	0x0	reserved

Bit	Attr	Reset Value	Description
16	RW	0x0	dfi_lp_en_dpd Enables DFI Low Power interface handshaking during Deep Power Down Entry/Exit. 0 - Disabled; 1 - Enabled This is only present for designs supporting mDDR or LPDDR2/LPDDR3 devices. Programming Mode: Static
15:12	RW	0x0	dfi_lp_wakeup_sr Value in DFI clpck cycles to drive on dfi_lp_wakeup signal when Self Refresh mode is entered. Determines the DFI's tlp_wakeup time: 0x0 - 16 cycles 0x1 - 32 cycles 0x2 - 64 cycles 0x3 - 128 cycles 0x4 - 256 cycles 0x5 - 512 cycles 0x6 - 1024 cycles 0x7 - 2048 cycles 0x8 - 4096 cycles 0x9 - 8192 cycles 0xA - 16384 cycles 0xB - 32768 cycles 0xC - 65536 cycles 0xD - 131072 cycles 0xE - 262144 cycles 0xF - Unlimited Programming Mode: Static
11:9	RO	0x0	reserved
8	RW	0x0	dfi_lp_en_sr Enables DFI Low Power interface handshaking during Self Refresh Entry/Exit. 0 - Disabled; 1 - Enabled Programming Mode: Static

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Bit	Attr	Reset Value	Description
7:4	RW	0x0	dfi_lp_wakeup_pd Value in DFI clock cycles to drive on dfi_lp_wakeup signal when Power Down mode is entered. Determines the DFI's tlp_wakeup time: 0x0 - 16 cycles 0x1 - 32 cycles 0x2 - 64 cycles 0x3 - 128 cycles 0x4 - 256 cycles 0x5 - 512 cycles 0x6 - 1024 cycles 0x7 - 2048 cycles 0x8 - 4096 cycles 0x9 - 8192 cycles 0xA - 16384 cycles 0xB - 32768 cycles 0xC - 65536 cycles 0xD - 131072 cycles 0xE - 262144 cycles 0xF - Unlimited Programming Mode: Static
3:1	RO	0x0	reserved
0	RW	0x0	dfi_lp_en_pd Enables DFI Low Power interface handshaking during Power Down Entry/Exit. 0: Disabled; 1: Enabled Programming Mode: Static

DDRC_DFILPCFG1

Address: Operational Base + offset (0x019c)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved

Bit	Attr	Reset Value	Description
7:4	RW	0x0	dfi_lp_wakeup_mpsm Value in DFI clock cycles to drive on dfi_lp_wakeup signal when Maximum Power Saving Mode is entered. Determines the DFI's tlp_wakeup time: 0x0 - 16 cycles 0x1 - 32 cycles 0x2 - 64 cycles 0x3 - 128 cycles 0x4 - 256 cycles 0x5 - 512 cycles 0x6 - 1024 cycles 0x7 - 2048 cycles 0x8 - 4096 cycles 0x9 - 8192 cycles 0xA - 16384 cycles 0xB - 32768 cycles 0xC - 65536 cycles 0xD - 131072 cycles 0xE - 262144 cycles 0xF - Unlimited This is only present for designs supporting DDR4 devices. Programming Mode: Static
3:1	RO	0x0	reserved
0	RW	0x0	dfi_lp_en_mpsm Enables DFI Low Power interface handshaking during Maximum Power Saving Mode Entry/Exit. 0 - Disabled; 1 - Enabled This is only present for designs supporting DDR4 devices. Programming Mode: Static

DDRC_DFIUPD0

Address: Operational Base + offset (0x01a0)

Bit	Attr	Reset Value	Description
31	RW	0x0	dis_auto_ctrlupd When '1', disable the automatic dfi_ctrlupd_req generation by the uMCTL2. The core must issue the dfi_ctrlupd_req signal using register DBGCMD.ctrlupd. When '0', uMCTL2 issues dfi_ctrlupd_req periodically. Programming Mode: Quasi-dynamic Group 3
30	RW	0x0	dis_auto_ctrlupd_srx When '1', disable the automatic dfi_ctrlupd_req generation by the uMCTL2 at self-refresh exit. When '0', uMCTL2 issues a dfi_ctrlupd_req before or after exiting self-refresh, depending on DFIUPD0.ctrlupd_pre_srx. Programming Mode: Static

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Bit	Attr	Reset Value	Description
29	RW	0x0	ctrlupd_pre_srx Selects dfi_ctrlupd_req requirements at SRX: 0 : send ctrlupd after SRX 1 : send ctrlupd before SRX If DFIUPD0.dis_auto_ctrlupd_srx=1, this register has no impact, because no dfi_ctrlupd_req will be issued when SRX. Programming Mode: Static
28:26	RO	0x0	reserved
25:16	RW	0x040	dfi_t_ctrlup_max Specifies the maximum number of DFI clock cycles that the dfi_ctrlupd_req signal can assert. Lowest value to assign to this variable is 0x40. Programming Mode: Static
15:10	RO	0x0	reserved
9:0	RW	0x003	dfi_t_ctrlup_min Specifies the minimum number of DFI clock cycles that the dfi_ctrlupd_req signal must be asserted. The uMCTL2 expects the PHY to respond within this time. If the PHY does not respond, the uMCTL2 will de-assert dfi_ctrlupd_req after dfi_t_ctrlup_min + 2 cycles. Lowest value to assign to this variable is 0x3. Programming Mode: Static

DDRC_DFIUPD1

Address: Operational Base + offset (0x01a4)

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:16	RW	0x00	dfi_t_ctrlupd_interval_min_x1024 This is the minimum amount of time between uMCTL2 initiated DFI update requests (which is executed whenever the uMCTL2 is idle). Set this number higher to reduce the frequency of update requests, which can have a small impact on the latency of the first read request when the uMCTL2 is idle. Minimum allowed value for this field is 1. Unit: 1024 DFI clock cycles Programming Mode: Static
15:8	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
7:0	RW	0x01	dfi_t_ctrlupd_interval_max_x1024 This is the maximum amount of time between uMCTL2 initiated DFI update requests. This timer resets with each update request; when the timer expires dfi_ctrlupd_req is sent and traffic is blocked until the dfi_ctrlupd_ackx is received. PHY can use this idle time to recalibrate the delay lines to the DLLs. The DFI controller update is also used to reset PHY FIFO pointers in case of data capture errors. Updates are required to maintain calibration over PVT, but frequent updates may impact performance. Minimum allowed value for this field is 1. Note: Value programmed for DFIUPD1.dfi_t_ctrlupd_interval_max_x1024 must be greater than DFIUPD1.dfi_t_ctrlupd_interval_min_x1024. Unit: 1024 DFI clock cycles Programming Mode: Static

DDRC_DFIUPD2

Address: Operational Base + offset (0x01a8)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x1	dfi_phyupd_en Enables the support for acknowledging PHY-initiated updates: 0 - Disabled; 1 - Enabled Programming Mode: Static

DDRC_DFIMISC

Address: Operational Base + offset (0x01b0)

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12:8	RW	0x00	dfi_frequency Indicates the operating frequency of the system. The number of supported frequencies and the mapping of signal values to clock frequencies are defined by the PHY. Programming Mode: Quasi-dynamic Group 1
7:6	RO	0x0	reserved
5	RW	0x0	dfi_init_start PHY init start request signal.When asserted it triggers the PHY init start request Programming Mode: Quasi-dynamic Group 3
4	RW	0x0	ctl_idle_en Enables support of ctl_idle signal, which is non-DFI related pin specific to certain Synopsys PHYs. See signal description of ctl_idle signal for further details of ctl_idle functionality. Programming Mode: Static

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Bit	Attr	Reset Value	Description
3	RW	0x0	share_dfi_dram_clk_disable Indicate dfi_dram_clk_disable is shared for two channels or not. 1: Share mode 0: Not share. In Shared mode, Controller does not request PHY stop clock while any rank of any channel has not disable clock. Note: when dfi_dram_clk_disable is shared by two channels, an additional DFF is inserted, that will cause dram clock enable is delay one cycle. Suggest set dfi_t_dram_clk_enable value to Tdram_clk_enable+1. Tdram_clk_enable value is from PHY, which indicate how many cycles from dfi_dram_clk_disable de-assert to dram clock output. Programming Mode: Static
2	RW	0x0	dfi_data_cs_polarity Defines polarity of dfi_wrdata_cs and dfi_rddata_cs signals. 0: Signals are active low; 1: Signals are active high Programming Mode: Static
1	RW	0x0	phy_dbi_mode DBI implemented in DDRC or PHY. 0 - DDRC implements DBI functionality. 1 - PHY implements DBI functionality. Present only in designs configured to support DDR4 and LPDDR4. Programming Mode: Static
0	RW	0x1	dfi_init_complete_en PHY initialization complete enable signal. When asserted the dfi_init_complete signal can be used to trigger SDRAM initialisation Programming Mode: Quasi-dynamic Group 3

DDRC_DFITMG2

Address: Operational Base + offset (0x01b4)

Bit	Attr	Reset Value	Description
31:15	RO	0x0	reserved
14:8	RW	0x02	dfi_tphy_rdcslat Number of DFI PHY clock cycles between when a read command is sent on the DFI control interface and when the associated dfi_rddata_cs signal is asserted. This corresponds to the DFI timing parameter tphy_rdcslat. Refer to PHY specification for correct value. Programming Mode: Quasi-dynamic Group 2 and Group 4
7:6	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
5:0	RW	0x02	dfi_tphy_wrcslat Number of DFI PHY clock cycles between when a write command is sent on the DFI control interface and when the associated dfi_wrdata_cs signal is asserted. This corresponds to the DFI timing parameter tphy_wrcslat. Refer to PHY specification for correct value. Programming Mode: Quasi-dynamic Group 2 and Group 4

DDRC_DFITMG3

Address: Operational Base + offset (0x01b8)

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4:0	RW	0x00	dfi_t_geardown_delay The delay from dfi_geardown_en assertion to the time of the PHY being ready to receive commands. Refer to PHY specification for correct value. When the controller is operating in 1:2 frequency ratio mode, program this to (tgeardown_delay/2) and round it up to the next integer value. Unit: DFI Clocks Programming Mode: Static

DDRC_DFISTAT

Address: Operational Base + offset (0x01bc)

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x0	dfi_lp_ack Stores the value of the dfi_lp_ack input to the controller. Programming Mode: Dynamic
0	RO	0x0	dfi_init_complete The status flag register which announces when the DFI initialization has been completed. The DFI INIT triggered by dfi_init_start signal and then the dfi_init_complete flag is polled to know when the initialization is done. Programming Mode: Dynamic

DDRC_DBICTL

Address: Operational Base + offset (0x01c0)

Bit	Attr	Reset Value	Description
31:3	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
2	RW	0x0	rd_dbi_en Read DBI enable signal in DDRC. 0 - Read DBI is disabled. 1 - Read DBI is enabled. This signal must be set the same value as DRAM's mode register. DDR4: MR5 bit A12. When x4 devices are used, this signal must be set to 0. LPDDR4: MR3[6] Programming Mode: Quasi-dynamic Group 1
1	RW	0x0	wr_dbi_en Write DBI enable signal in DDRC. 0 - Write DBI is disabled. 1 - Write DBI is enabled. This signal must be set the same value as DRAM's mode register. DDR4: MR5 bit A11. When x4 devices are used, this signal must be set to 0. LPDDR4: MR3[7] Programming Mode: Quasi-dynamic Group 1
0	RW	0x1	dm_en DM enable signal in DDRC. 0 - DM is disabled; 1 - DM is enabled. This signal must be set the same logical value as DRAM's mode register. DDR4: Set this to same value as MR5 bit A10. When x4 devices are used, this signal must be set to 0. LPDDR4: Set this to inverted value of MR13[5] which is opposite polarity from this signal Programming Mode: Quasi-dynamic Group 3

DDRC_DFIPHYMSTR

Address: Operational Base + offset (0x01c4)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x1	dfi_phymstr_en Enables the PHY Master Interface: 0 - Disabled; 1 - Enabled Programming Mode: Dynamic

DDRC_ADDRMAP0

Address: Operational Base + offset (0x0200)

Bit	Attr	Reset Value	Description
31:21	RO	0x0	reserved

Bit	Attr	Reset Value	Description
20:16	RW	0x00	addrmap_dch_bit0 Selects the HIF address bit used as data channel address bit 0. Valid Range: 0 to 30, and 31 (Traffic constraints apply based on the register value when UMCTL2_EXCL_ACCESS>0. See Exclusive Access section for details.) Internal Base: 2 The selected address bit is determined by adding the internal base to the value of this field. If unused, set to 31 and then channel bit is set to 0. Programming Mode: Static
15:13	RO	0x0	reserved
12:8	RW	0x00	addrmap_cs_bit1 Selects the HIF address bit used as rank address bit 1. Valid Range: 0 to 28, and 31 Internal Base: 7 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 31 and then rank address bit 1 is set to 0. Programming Mode: Static
7:5	RO	0x0	reserved
4:0	RW	0x00	addrmap_cs_bit0 Selects the HIF address bit used as rank address bit 0. Valid Range: 0 to 29, and 31 Internal Base: 6 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 31 and then rank address bit 0 is set to 0. Programming Mode: Static

DDRC_ADDRMAP1

Address: Operational Base + offset (0x0204)

Bit	Attr	Reset Value	Description
31:22	RO	0x0	reserved
21:16	RW	0x00	addrmap_bank_b2 Selects the HIF address bit used as bank address bit 2. Valid Range: 0 to 31 and 63 Internal Base: 4 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 63 and then bank address bit 2 is set to 0. Programming Mode: Static
15:14	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
13:8	RW	0x00	addrmap_bank_b1 Selects the HIF address bits used as bank address bit 1. Valid Range: 0 to 32 and 63 Internal Base: 3 The selected HIF address bit for each of the bank address bits is determined by adding the internal base to the value of this field. If unused, set to 63 and then bank address bit 1 is set to 0. Programming Mode: Static
7:6	RO	0x0	reserved
5:0	RW	0x00	addrmap_bank_b0 Selects the HIF address bits used as bank address bit 0. Valid Range: 0 to 32 and 63 Internal Base: 2 The selected HIF address bit for each of the bank address bits is determined by adding the internal base to the value of this field. If unused, set to 63 and then bank address bit 0 is set to 0. Programming Mode: Static

DDRC_ADDRMAP2

Address: Operational Base + offset (0x0208)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:24	RW	0x0	addrmap_col_b5 Full bus width mode: Selects the HIF address bit used as column address bit 5. Half bus width mode: Selects the HIF address bit used as column address bit 6. Valid Range: 0 to 7, and 15 Internal Base: 5 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 15 and then this column address bit is set to 0. Programming Mode: Static
23:20	RO	0x0	reserved
19:16	RW	0x0	addrmap_col_b4 Full bus width mode: Selects the HIF address bit used as column address bit 4. Half bus width mode: Selects the HIF address bit used as column address bit 5. Valid Range: 0 to 7, and 15 Internal Base: 4 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 15 and then this column address bit is set to 0. Programming Mode: Static

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Bit	Attr	Reset Value	Description
15:12	RO	0x0	reserved
11:8	RW	0x0	addrmap_col_b3 Full bus width mode: Selects the HIF address bit used as column address bit 3. Half bus width mode: Selects the HIF address bit used as column address bit 4. Valid Range: 0 to 7 Internal Base: 3 The selected HIF address bit is determined by adding the internal base to the value of this field. Note, if UMCTL2_INCL_ARB=1, MEMC_BURST_LENGTH=16, Full bus width (MSTR.data_bus_width=00) and BL16 (MSTR.burst_rdwr=1000), it is recommended to program this to 0. Programming Mode: Static
7:4	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
3:0	RW	0x0	addrmap_col_b2 Full bus width mode: Selects the HIF address bit used as column address bit 2. Half bus width mode: Selects the HIF address bit used as column address bit 3. Valid Range: 0 to 7 Internal Base: 2 The selected HIF address bit is determined by adding the internal base to the value of this field. Note, if UMCTL2_INCL_ARB=1 and MEMC_BURST_LENGTH=8, it is required to program this to 0 unless: in Half or Quarter bus width (MSTR.data_bus_width!=00) and PCCFG.bl_exp_mode==1 and either In DDR4 and ADDRMAP8.addrmap_bg_b0==0 or In LPDDR4 and ADDRMAP1.addrmap_bank_b0==0 If UMCTL2_INCL_ARB=1 and MEMC_BURST_LENGTH=16, it is required to program this to 0 unless: in Half or Quarter bus width (MSTR.data_bus_width!=00) and PCCFG.bl_exp_mode==1 and In DDR4 and ADDRMAP8.addrmap_bg_b0==0 Otherwise, if MEMC_BURST_LENGTH=8 and Full Bus Width (MSTR.data_bus_width==00), it is recommended to program this to 0 so that HIF[2] maps to column address bit 2. If MEMC_BURST_LENGTH=16 and Full Bus Width (MSTR.data_bus_width==00), it is recommended to program this to 0 so that HIF[2] maps to column address bit 2. If MEMC_BURST_LENGTH=16 and Half Bus Width (MSTR.data_bus_width==01), it is recommended to program this to 0 so that HIF[2] maps to column address bit 3. Programming Mode: Static

DDRC_ADDRMAP3

Address: Operational Base + offset (0x020c)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved

Bit	Attr	Reset Value	Description
28:24	RW	0x00	addrmap_col_b9 Full bus width mode: Selects the HIF address bit used as column address bit 9. Half bus width mode: Selects the HIF address bit used as column address bit 11 (10 in LPDDR2/LPDDR3 mode). Valid Range: 0 to 7, and 31. Internal Base: 9 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 31 and then this column address bit is set to 0. Note: Per JEDEC DDR2/3/mDDR specification, column address bit 10 is reserved for indicating auto-precharge, and hence no source address bit can be mapped to column address bit 10. In LPDDR2/LPDDR3, there is a dedicated bit for autoprecharge in the CA bus and hence column bit 10 is used. Programming Mode: Static
23:21	RO	0x0	reserved
20:16	RW	0x00	addrmap_col_b8 Full bus width mode: Selects the HIF address bit used as column address bit 8. Half bus width mode: Selects the HIF address bit used as column address bit 9. Valid Range: 0 to 7, and 31. Internal Base: 8 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 31 and then this column address bit is set to 0. Note: Per JEDEC DDR2/3/mDDR specification, column address bit 10 is reserved for indicating auto-precharge, and hence no source address bit can be mapped to column address bit 10. In LPDDR2/LPDDR3, there is a dedicated bit for autoprecharge in the CA bus and hence column bit 10 is used. Programming Mode: Static
15:13	RO	0x0	reserved
12:8	RW	0x00	addrmap_col_b7 Full bus width mode: Selects the HIF address bit used as column address bit 7. Half bus width mode: Selects the HIF address bit used as column address bit 8. Valid Range: 0 to 7, and 31. Internal Base: 7 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 31 and then this column address bit is set to 0. Programming Mode: Static

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Bit	Attr	Reset Value	Description
7:4	RO	0x0	reserved
3:0	RW	0x0	addrmap_col_b6 Full bus width mode: Selects the HIF address bit used as column address bit 6. Half bus width mode: Selects the HIF address bit used as column address bit 7. Valid Range: 0 to 7, and 15 Internal Base: 6 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 15 and then this column address bit is set to 0. Programming Mode: Static

DDRC_ADDRMAP4

Address: Operational Base + offset (0x0210)

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12:8	RW	0x00	addrmap_col_b11 Full bus width mode: Selects the HIF address bit used as column address bit 13 (11 in LPDDR2/LPDDR3 mode). Half bus width mode: Unused. To make it unused, this should be tied to 4'hF. Valid Range: 0 to 7, and 31. Internal Base: 11 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 31 and then this column address bit is set to 0. Note: Per JEDEC DDR2/3/mDDR specification, column address bit 10 is reserved for indicating auto-precharge, and hence no source address bit can be mapped to column address bit 10. In LPDDR2/LPDDR3, there is a dedicated bit for autoprecharge in the CA bus and hence column bit 10 is used. Programming Mode: Static
7:5	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
4:0	RW	0x00	addrmap_col_b10 Full bus width mode: Selects the HIF address bit used as column address bit 11 (10 in LPDDR2/LPDDR3 mode). Half bus width mode: Selects the HIF address bit used as column address bit 13 (11 in LPDDR2/LPDDR3 mode). Valid Range: 0 to 7, and 31. Internal Base: 10 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 31 and then this column address bit is set to 0. Note: Per JEDEC DDR2/3/mDDR specification, column address bit 10 is reserved for indicating auto-precharge, and hence no source address bit can be mapped to column address bit 10. In LPDDR2/LPDDR3, there is a dedicated bit for autoprecharge in the CA bus and hence column bit 10 is used. Programming Mode: Static

DDRC_ADDRMAP5

Address: Operational Base + offset (0x0214)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:24	RW	0x0	addrmap_row_b11 Selects the HIF address bit used as row address bit 11. Valid Range: 0 to 11, and 15 Internal Base: 17 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 15 and then row address bit 11 is set to 0. Programming Mode: Static
23:20	RO	0x0	reserved
19:16	RW	0x0	addrmap_row_b2_10 Selects the HIF address bits used as row address bits 2 to 10. Valid Range: 0 to 11, and 15 Internal Base: 8 (for row address bit 2), 9 (for row address bit 3), 10 (for row address bit 4) etc increasing to 16 (for row address bit 10) The selected HIF address bit for each of the row address bits is determined by adding the internal base to the value of this field. When value 15 is used the values of row address bits 2 to 10 are defined by registers ADDRMAP9, ADDRMAP10, ADDRMAP11. Programming Mode: Static
15:12	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
11:8	RW	0x0	addrmap_row_b1 Selects the HIF address bits used as row address bit 1. Valid Range: 0 to 11 Internal Base: 7 The selected HIF address bit for each of the row address bits is determined by adding the internal base to the value of this field. Programming Mode: Static
7:4	RO	0x0	reserved
3:0	RW	0x0	addrmap_row_b0 Selects the HIF address bits used as row address bit 0. Valid Range: 0 to 11 Internal Base: 6 The selected HIF address bit for each of the row address bits is determined by adding the internal base to the value of this field. Programming Mode: Static

DDRC_ADDRMAP6

Address: Operational Base + offset (0x0218)

Bit	Attr	Reset Value	Description
31	RW	0x0	lpddr3_6gb_12gb Set this to 1 if there is an LPDDR3 SDRAM 6Gb or 12Gb device in use. 1 - LPDDR3 SDRAM 6Gb/12Gb device in use. Every address having row[14:13]==2'b11 is considered as invalid 0 - non-LPDDR3 6Gb/12Gb device in use. All addresses are valid Present only in designs configured to support LPDDR3. Programming Mode: Static
30:29	RW	0x0	lpddr4_6gb_12gb_24gb Indicates what type of LPDDR4 SDRAM device is in use. 2'b00: No LPDDR4 SDRAM 6Gb/12Gb/24Gb device in use. All addresses are valid 2'b01: LPDDR4 SDRAM 6Gb device in use. Every address having row[14:13]==2'b11 is considered as invalid 2'b10: LPDDR4 SDRAM 12Gb device in use. Every address having row[15:14]==2'b11 is considered as invalid 2'b11: LPDDR4 SDRAM 24Gb device in use. Unsupported Present only in designs configured to support LPDDR4. Programming Mode: Static
28	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
27:24	RW	0x0	addrmap_row_b15 Selects the HIF address bit used as row address bit 15. Valid Range: 0 to 11, and 15 Internal Base: 21 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 15 and then row address bit 15 is set to 0. Programming Mode: Static
23:20	RO	0x0	reserved
19:16	RW	0x0	addrmap_row_b14 Selects the HIF address bit used as row address bit 14. Valid Range: 0 to 11, and 15 Internal Base: 20 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 15 and then row address bit 14 is set to 0. Programming Mode: Static
15:12	RO	0x0	reserved
11:8	RW	0x0	addrmap_row_b13 Selects the HIF address bit used as row address bit 13. Valid Range: 0 to 11, and 15 Internal Base: 19 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 15 and then row address bit 13 is set to 0. Programming Mode: Static
7:4	RO	0x0	reserved
3:0	RW	0x0	addrmap_row_b12 Selects the HIF address bit used as row address bit 12. Valid Range: 0 to 11, and 15 Internal Base: 18 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 15 and then row address bit 12 is set to 0. Programming Mode: Static

DDRC_ADDRMAP7

Address: Operational Base + offset (0x021c)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved

Bit	Attr	Reset Value	Description
11:8	RW	0x0	addrmap_row_b17 Selects the HIF address bit used as row address bit 17. Valid Range: 0 to 11, and 15 Internal Base: 23 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 15 and then row address bit 17 is set to 0. Programming Mode: Static
7:4	RO	0x0	reserved
3:0	RW	0x0	addrmap_row_b16 Selects the HIF address bit used as row address bit 16. Valid Range: 0 to 11, and 15 Internal Base: 22 The selected HIF address bit is determined by adding the internal base to the value of this field. If unused, set to 15 and then row address bit 16 is set to 0. Programming Mode: Static

DDRC_ADDRMAP8

Address: Operational Base + offset (0x0220)

Bit	Attr	Reset Value	Description
31:14	RO	0x0	reserved
13:8	RW	0x00	addrmap_bg_b1 Selects the HIF address bits used as bank group address bit 1. Valid Range: 0 to 32, and 63 Internal Base: 3 The selected HIF address bit for each of the bank group address bits is determined by adding the internal base to the value of this field. If unused, set to 63 and then bank group address bit 1 is set to 0. Programming Mode: Static
7:6	RO	0x0	reserved
5:0	RW	0x00	addrmap_bg_b0 Selects the HIF address bits used as bank group address bit 0. Valid Range: 0 to 32 and 63 Internal Base: 2 The selected HIF address bit for each of the bank group address bits is determined by adding the internal base to the value of this field. If unused, set to 63 and then bank group address bit 0 is set to 0. Programming Mode: Static

DDRC_ADDRMAP9

Address: Operational Base + offset (0x0224)

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Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:24	RW	0x0	addrmap_row_b5 Selects the HIF address bits used as row address bit 5. Valid Range: 0 to 11 Internal Base: 11 The selected HIF address bit for each of the row address bits is determined by adding the internal base to the value of this field. This register field is used only when ADDRMAP5.addrmap_row_b2_10 is set to value 15. Programming Mode: Static
23:20	RO	0x0	reserved
19:16	RW	0x0	addrmap_row_b4 Selects the HIF address bits used as row address bit 4. Valid Range: 0 to 11 Internal Base: 10 The selected HIF address bit for each of the row address bits is determined by adding the internal base to the value of this field. This register field is used only when ADDRMAP5.addrmap_row_b2_10 is set to value 15. Programming Mode: Static
15:12	RO	0x0	reserved
11:8	RW	0x0	addrmap_row_b3 Selects the HIF address bits used as row address bit 3. Valid Range: 0 to 11 Internal Base: 9 The selected HIF address bit for each of the row address bits is determined by adding the internal base to the value of this field. This register field is used only when ADDRMAP5.addrmap_row_b2_10 is set to value 15. Programming Mode: Static
7:4	RO	0x0	reserved
3:0	RW	0x0	addrmap_row_b2 Selects the HIF address bits used as row address bit 2. Valid Range: 0 to 11 Internal Base: 8 The selected HIF address bit for each of the row address bits is determined by adding the internal base to the value of this field. This register field is used only when ADDRMAP5.addrmap_row_b2_10 is set to value 15. Programming Mode: Static

DDRC_ADDRMAP10

Address: Operational Base + offset (0x0228)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved

Bit	Attr	Reset Value	Description
27:24	RW	0x0	addrmap_row_b9 Selects the HIF address bits used as row address bit 9. Valid Range: 0 to 11 Internal Base: 15 The selected HIF address bit for each of the row address bits is determined by adding the internal base to the value of this field. This register field is used only when ADDRMAP5.addrmap_row_b2_10 is set to value 15. Programming Mode: Static
23:20	RO	0x0	reserved
19:16	RW	0x0	addrmap_row_b8 Selects the HIF address bits used as row address bit 8. Valid Range: 0 to 11 Internal Base: 14 The selected HIF address bit for each of the row address bits is determined by adding the internal base to the value of this field. This register field is used only when ADDRMAP5.addrmap_row_b2_10 is set to value 15. Programming Mode: Static
15:12	RO	0x0	reserved
11:8	RW	0x0	addrmap_row_b7 Selects the HIF address bits used as row address bit 7. Valid Range: 0 to 11 Internal Base: 13 The selected HIF address bit for each of the row address bits is determined by adding the internal base to the value of this field. This register field is used only when ADDRMAP5.addrmap_row_b2_10 is set to value 15. Programming Mode: Static
7:4	RO	0x0	reserved
3:0	RW	0x0	addrmap_row_b6 Selects the HIF address bits used as row address bit 6. Valid Range: 0 to 11 Internal Base: 12 The selected HIF address bit for each of the row address bits is determined by adding the internal base to the value of this field. This register field is used only when ADDRMAP5.addrmap_row_b2_10 is set to value 15. Programming Mode: Static

DDRC_ADDRMAP11

Address: Operational Base + offset (0x022c)

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved

Bit	Attr	Reset Value	Description
3:0	RW	0x0	addrmap_row_b10 Selects the HIF address bits used as row address bit 10. Valid Range: 0 to 11 Internal Base: 16 The selected HIF address bit for each of the row address bits is determined by adding the internal base to the value of this field. This register field is used only when ADDRMAP5.addrmap_row_b2_10 is set to value 15. Programming Mode: Static

DDRC_ODTCFG

Address: Operational Base + offset (0x0240)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:24	RW	0x4	wr_odt_hold DFI PHY clock cycles to hold ODT for a write command. The minimum supported value is 2. Recommended values: DDR2: BL8: 0x5 (DDR2-400/533/667), 0x6 (DDR2-800), 0x7(DDR2-1066); BL4: 0x3 (DDR2-400/533/667), 0x4 (DDR2-800), 0x5 (DDR2-1066) DDR3: BL8: 0x6 DDR4: BL8: 5 + WR_PREAMBLE + CRC_MODE. WR_PREAMBLE = 1 (1tCK write preamble), 2 (2tCK write preamble). CRC_MODE = 0 (not CRC mode), 1 (CRC mode) LPDDR3: BL8: 7 + RU(tODTon(max)/tCK) Programming Mode: Quasi-dynamic Group 1 and Group 4
23:21	RO	0x0	reserved
20:16	RW	0x00	wr_odt_delay The delay, in DFI PHY clock cycles, from issuing a write command to setting ODT values associated with that command. ODT setting must remain constant for the entire time that DQS is driven by the uMCTL2. Recommended values: DDR2: CWL + AL - 3 (DDR2-400/533/667), CWL + AL - 4 (DDR2-800), CWL + AL - 5 (DDR2-1066). If (CWL + AL - 3 < 0), uMCTL2 does not support ODT for write operation. DDR3: 0x0 DDR4: DFITMG1.dfi_t_cmd_lat (to adjust for CAL mode) LPDDR3: WL - 1 - RU(tODTon(max)/tCK)) Programming Mode: Quasi-dynamic Group 1 and Group 4
15:12	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
11:8	RW	0x4	rd_odt_hold DFI PHY clock cycles to hold ODT for a read command. The minimum supported value is 2. Recommended values: DDR2: BL8: 0x6 (not DDR2-1066), 0x7 (DDR2-1066); BL4: 0x4 (not DDR2-1066), 0x5 (DDR2-1066) DDR3: BL8 - 0x6 DDR4: BL8: 5 + RD_PREAMBLE. RD_PREAMBLE = 1 (1tCK write preamble), 2 (2tCKwrite preamble) LPDDR3: BL8: 5 + RU(tDQSCK(max)/tCK) - RD(tDQSCK(min)/tCK) + RU(tODTon(max)/tCK) Programming Mode: Quasi-dynamic Group 1 and Group 4
7	RO	0x0	reserved
6:2	RW	0x00	rd_odt_delay The delay, in DFI PHY clock cycles, from issuing a read command to setting ODT values associated with that command. ODT setting must remain constant for the entire time that DQS is driven by the uMCTL2. Recommended values: DDR2: CL + AL - 4 (not DDR2-1066), CL + AL - 5 (DDR2-1066). If (CL + AL - 4 < 0), uMCTL2 does not support ODT for read operation. DDR3: CL - CWL DDR4: CL - CWL - RD_PREAMBLE + WR_PREAMBLE + DFITMG1.dfi_t_cmd_lat (to adjust for CAL mode). WR_PREAMBLE = 1 (1tCK write preamble), 2 (2tCK write preamble). RD_PREAMBLE = 1 (1tCK write preamble), 2 (2tCK write preamble). If (CL - CWL - RD_PREAMBLE + WR_PREAMBLE) < 0, uMCTL2 does not support ODT for read operation. LPDDR3: RL + RD(tDQSCK(min)/tCK) - 1 - RU(tODTon(max)/tCK) Programming Mode: Quasi-dynamic Group 1 and Group 4
1:0	RO	0x0	reserved

DDRC_ODTMAP

Address: Operational Base + offset (0x0244)

Bit	Attr	Reset Value	Description
31:14	RO	0x0	reserved
13:12	RW	0x2	rank1_rd_odt Indicates which remote ODTs must be turned on during a read from rank 1. Each rank has a remote ODT (in the SDRAM) which can be turned on by setting the appropriate bit here. Rank 0 is controlled by the LSB; rank 1 is controlled by bit next to the LSB, etc. For each rank, set its bit to 1 to enable its ODT. Programming Mode: Static

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Bit	Attr	Reset Value	Description
11:10	RO	0x0	reserved
9:8	RW	0x2	rank1_wr_odt Indicates which remote ODTs must be turned on during a write to rank 1. Each rank has a remote ODT (in the SDRAM) which can be turned on by setting the appropriate bit here. Rank 0 is controlled by the LSB; rank 1 is controlled by bit next to the LSB, etc. For each rank, set its bit to 1 to enable its ODT. Programming Mode: Static
7:6	RO	0x0	reserved
5:4	RW	0x1	rank0_rd_odt Indicates which remote ODTs must be turned on during a read from rank 0. Each rank has a remote ODT (in the SDRAM) which can be turned on by setting the appropriate bit here. Rank 0 is controlled by the LSB; rank 1 is controlled by bit next to the LSB, etc. For each rank, set its bit to 1 to enable its ODT. Programming Mode: Static
3:2	RO	0x0	reserved
1:0	RW	0x1	rank0_wr_odt Indicates which remote ODTs must be turned on during a write to rank 0. Each rank has a remote ODT (in the SDRAM) which can be turned on by setting the appropriate bit here. Rank 0 is controlled by the LSB; rank 1 is controlled by bit next to the LSB, etc. For each rank, set its bit to 1 to enable its ODT. Programming Mode: Static

DDRC_SCHED

Address: Operational Base + offset (0x0250)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x00	rdwr_idle_gap When the preferred transaction store is empty for these many clock cycles, switch to the alternate transaction store if it is non-empty. The read transaction store (both high and low priority) is the default preferred transaction store and the write transaction store is the alternative store. When prefer write over read is set this is reversed. 0x0 is a legal value for this register. When set to 0x0, the transaction store switching will happen immediately when the switching conditions become true. Programming Mode: Static
23:12	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
11:8	RW	0x8	lpr_num_entries Number of entries in the low priority transaction store is this value + 1. (MEMC_NO_OF_ENTRY - (SCHED.lpr_num_entries + 1)) is the number of entries available for the high priority transaction store. Setting this to maximum value allocates all entries to low priority transaction store. Setting this to 0 allocates 1 entry to low priority transaction store and the rest to high priority transaction store. Programming Mode: Static
7:3	RO	0x0	reserved
2	RW	0x1	pageclose If true, bank is kept open only while there are page hit transactions available in the CAM to that bank. The last read or write command in the CAM with a bank and page hit will be executed with auto-precharge if SCHED1.pageclose_timer=0. Even if this register set to 1 and SCHED1.pageclose_timer is set to 0, explicit precharge (and not auto-precharge) may be issued in some cases where there is a mode switch between Write and Read or between LPR and HPR. The Read and Write commands that are executed as part of the ECC scrub requests are also executed without auto-precharge. If false, the bank remains open until there is a need to close it (to open a different page, or for page timeout or refresh timeout) - also known as open page policy. The pageclose feature provids a midway between Open and Close page policies. Programming Mode: Quasi-dynamic Group 3
1:0	RO	0x0	reserved

DDRC_SCHED1

Address: Operational Base + offset (0x0254)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved

Bit	Attr	Reset Value	Description
7:0	RW	0x00	pageclose_timer This field works in conjunction with SCHED.pageclose. It only has meaning if SCHED.pageclose==1. If SCHED.pageclose==1 and pageclose_timer==0, then an auto-precharge may be scheduled for last read or write command in the CAM with a bank and page hit. Note, sometimes an explicit precharge is scheduled instead of the auto-precharge. See SCHED.pageclose for details of when this may happen. If SCHED.pageclose==1 and pageclose_timer>0, then an auto-precharge is not scheduled for last read or write command in the CAM with a bank and page hit. Instead, a timer is started, with pageclose_timer as the initial value. There is a timer on a per bank basis. The timer decrements unless the next read or write in the CAM to a bank is a page hit. It gets reset to pageclose_timer value if the next read or write in the CAM to a bank is a page hit. Once the timer has reached zero, an explcit precharge will be attempted to be scheduled. Programming Mode: Static

DDRC_PERFLPR1

Address: Operational Base + offset (0x0264)

Bit	Attr	Reset Value	Description
31:24	RW	0x0f	lpr_xact_run_length Number of transactions that are serviced once the LPR queue goes critical is the smaller of: (a) This number (b) Number of transactions available. Unit: Transaction. Programming Mode: Quasi-dynamic Group 3
23:16	RO	0x0	reserved
15:0	RW	0x007f	lpr_max_starve Number of DFI clocks that the LPR queue can be starved before it goes critical. The minimum valid functional value for this register is 0x1. Programming it to 0x0 will disable the starvation functionality; during normal operation, this function should not be disabled as it will cause excessive latencies. Programming Mode: Quasi-dynamic Group 3

DDRC_PERFWR1

Address: Operational Base + offset (0x026c)

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Bit	Attr	Reset Value	Description
31:24	RW	0x0f	w_xact_run_length Number of transactions that are serviced once the WR queue goes critical is the smaller of: (a) This number (b) Number of transactions available. Unit: Transaction. Programming Mode: Quasi-dynamic Group 3
23:16	RO	0x0	reserved
15:0	RW	0x007f	w_max_starve Number of DFI clocks that the WR queue can be starved before it goes critical. The minimum valid functional value for this register is 0x1. Programming it to 0x0 will disable the starvation functionality; during normal operation, this function should not be disabled as it will cause excessive latencies. Programming Mode: Quasi-dynamic Group 3

DDRC_DBG0

Address: Operational Base + offset (0x0300)

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4	RW	0x0	dis_collision_page_opt When this is set to '0', auto-precharge is disabled for the flushed command in a collision case. Collision cases are write followed by read to same address, read followed by write to same address, or write followed by write to same address with DBG0.dis_wc bit = 1 (where same address comparisons exclude the two address bits representing critical word). Programming Mode: Static
3:0	RO	0x0	reserved

DDRC_DBG1

Address: Operational Base + offset (0x0304)

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x0	dis_hif When 1, uMCTL2 asserts the HIF command signal hif_cmd_stall. uMCTL2 will ignore the hif_cmd_valid and all other associated request signals. This bit is intended to be switched on-the-fly. Programming Mode: Dynamic

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Bit	Attr	Reset Value	Description
0	RW	0x0	dis_dq When 1, uMCTL2 will not de-queue any transactions from the CAM. Bypass is also disabled. All transactions are queued in the CAM. No reads or writes are issued to SDRAM as long as this is asserted. This bit may be used to prevent reads or writes being issued by the uMCTL2, which makes it safe to modify certain register fields associated with reads and writes (see User Guide for details). After setting this bit, it is strongly recommended to poll DBGCAM.wr_data_pipeline_empty and DBGCAM.rd_data_pipeline_empty, before making changes to any registers which affect reads and writes. This will ensure that the relevant logic in the DDRC is idle. This bit is intended to be switched on-the-fly. Programming Mode: Dynamic

DDRC_DBGCAM

Address: Operational Base + offset (0x0308)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29	RO	0x0	wr_data_pipeline_empty When 1, indicates that the write data pipeline on the DFI interface is empty. This register is intended to be polled at least twice after setting DBG1.dis_dq, to ensure that all remaining commands/data have completed. Programming Mode: Dynamic
28	RO	0x0	rd_data_pipeline_empty When 1，indicates that the read data pipeline on the DFI interface is empty. This register is intended to be polled at least twice after setting DBG1.dis_dq, to ensure that all remaining commands/data have completed. Programming Mode: Dynamic
27	RO	0x0	reserved
26	RO	0x0	dbg_wr_q_empty When 1, all the Write command queues and Write data buffers inside DDRC are empty. This register is to be used for debug purpose. An example use-case scenario: When Controller enters SelfRefresh using the Low-Power entry sequence, Controller is expected to have executed all the commands in its queues and the write and read data drained. Hence this register should be 1 at that time. Programming Mode: Dynamic

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Bit	Attr	Reset Value	Description
25	RO	0x0	dbg_rd_q_empty When 1, all the Read command queues and Read data buffers inside DDRC are empty. This register is to be used for debug purpose. An example use-case scenario: When Controller enters SelfRefresh using the Low-Power entry sequence, Controller is expected to have executed all the commands in its queues and the write and read data drained. Hence this register should be 1 at that time. Programming Mode: Dynamic
24	RO	0x0	dbg_stall Stall Programming Mode: Dynamic
23:20	RO	0x0	reserved
19:16	RO	0x0	dbg_w_q_depth Write queue depth The last entry of WR queue is reserved for ECC SCRUB operation. This entry is not included in the calculation of the queue depth. Programming Mode: Dynamic
15:12	RO	0x0	reserved
11:8	RO	0x0	dbg_lpr_q_depth Low priority read queue depth. The last entry of Lpr queue is reserved for ECC SCRUB operation. This entry is not included in the calculation of the queue depth. Programming Mode: Dynamic
7:0	RO	0x0	reserved

DDRC_DBGCMD

Address: Operational Base + offset (0x030c)

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5	RW	0x0	ctrlupd Setting this register bit to 1 indicates to the uMCTL2 to issue a dfi_ctrlupd_req to the PHY. When this request is stored in the uMCTL2, the bit is automatically cleared. This operation must only be performed when DFIUPD0.dis_auto_ctrlupd=1. Programming Mode: Dynamic

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Bit	Attr	Reset Value	Description
4	RW	0x0	zq_calib_short Setting this register bit to 1 indicates to the uMCTL2 to issue a ZQCS (ZQ calibration short)/MPC(ZQ calibration) command to the SDRAM. When this request is stored in the uMCTL2, the bit is automatically cleared. This operation can be performed only when ZQCTL0.dis_auto_zq=1. It is recommended NOT to set this register bit if in Init operating mode. This register bit is ignored when in SelfRefresh(except LPDDR4) and SR-Powerdown(LPDDR4) and Deep power-down operating modes and Maximum Power Saving Mode. Programming Mode: Dynamic
3:2	RO	0x0	reserved
1	RW	0x0	rank1_refresh Setting this register bit to 1 indicates to the uMCTL2 to issue a refresh to rank 1. Writing to this bit causes DBGSTAT.rank1_refresh_busy to be set. When DBGSTAT.rank1_refresh_busy is cleared, the command has been stored in uMCTL2. This operation can be performed only when RFSHCTL3.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Deep power-down operating modes or Maximum Power Saving Mode. Programming Mode: Dynamic
0	RW	0x0	rank0_refresh Setting this register bit to 1 indicates to the uMCTL2 to issue a refresh to rank 0. Writing to this bit causes DBGSTAT.rank0_refresh_busy to be set. When DBGSTAT.rank0_refresh_busy is cleared, the command has been stored in uMCTL2. This operation can be performed only when RFSHCTL3.dis_auto_refresh=1. It is recommended NOT to set this register bit if in Init or Deep power-down operating modes or Maximum Power Saving Mode. Programming Mode: Dynamic

DDRC_DBGSTAT

Address: Operational Base + offset (0x0310)

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
5	RO	0x0	ctrlupd_busy SoC core may initiate a ctrlupd operation only if this signal is low. This signal goes high in the clock after the uMCTL2 accepts the ctrlupd request. It goes low when the ctrlupd operation is initiated in the uMCTL2. It is recommended not to perform ctrlupd operations when this signal is high. 0 - Indicates that the SoC core can initiate a ctrlupd operation 1 - Indicates that ctrlupd operation has not been initiated yet in the uMCTL2 Programming Mode: Dynamic
4	RO	0x0	zq_calib_short_busy SoC core may initiate a ZQCS (ZQ calibration short) operation only if this signal is low. This signal goes high in the clock after the uMCTL2 accepts the ZQCS request. It goes low when the ZQCS operation is initiated in the uMCTL2. It is recommended not to perform ZQCS operations when this signal is high. 0 - Indicates that the SoC core can initiate a ZQCS operation 1 - Indicates that ZQCS operation has not been initiated yet in the uMCTL2 Programming Mode: Dynamic
3:2	RO	0x0	reserved
1	RO	0x0	rank1_refresh_busy SoC core may initiate a rank1_refresh operation (refresh operation to rank 1) only if this signal is low. This signal goes high in the clock after DBGCMD.rank1_refresh is set to one. It goes low when the rank1_refresh operation is stored in the uMCTL2. It is recommended not to perform rank1_refresh operations when this signal is high. 0 - Indicates that the SoC core can initiate a rank1_refresh operation 1 - Indicates that rank1_refresh operation has not been stored yet in the uMCTL2 Programming Mode: Dynamic
0	RO	0x0	rank0_refresh_busy SoC core may initiate a rank0_refresh operation (refresh operation to rank 0) only if this signal is low. This signal goes high in the clock after DBGCMD.rank0_refresh is set to one. It goes low when the rank0_refresh operation is stored in the uMCTL2. It is recommended not to perform rank0_refresh operations when this signal is high. 0 - Indicates that the SoC core can initiate a rank0_refresh operation 1 - Indicates that rank0_refresh operation has not been stored yet in the uMCTL2 Programming Mode: Dynamic

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DDRC_SWCTL

Address: Operational Base + offset (0x0320)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x1	sw_done Enable quasi-dynamic register programming outside reset. Program register to 0 to enable quasi-dynamic programming. Set back register to 1 once programming is done. Programming Mode: Dynamic

DDRC_SWSTAT

Address: Operational Base + offset (0x0324)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RO	0x1	sw_done_ack Register programming done. This register is the echo of SWCTL.sw_done. Wait for sw_done value 1 to propagate to sw_done_ack at the end of the programming sequence to ensure that the correct registers values are propagated to the destination clock domains. Programming Mode: Static

DDRC_POISONCFG

Address: Operational Base + offset (0x036c)

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24	RW	0x0	rd_poison_intr_clr Interrupt clear for read transaction poisoning. Allow 2/3 clock cycles for correct value to propagate to core logic and clear the interrupts. Programming Mode: Dynamic
23:21	RO	0x0	reserved
20	RW	0x1	rd_poison_intr_en If set to 1, enables interrupts for read transaction poisoning Programming Mode: Dynamic
19:17	RO	0x0	reserved
16	RW	0x1	rd_poison_slverr_en If set to 1, enables SLVERR response for read transaction poisoning Programming Mode: Dynamic
15:9	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
8	W1C	0x0	wr_poison_intr_clr Interrupt clear for write transaction poisoning. Allow 2/3 clock cycles for correct value to propagate to core logic and clear the interrupts. Programming Mode: Dynamic
7:5	RO	0x0	reserved
4	RW	0x1	wr_poison_intr_en If set to 1, enables interrupts for write transaction poisoning Programming Mode: Dynamic
3:1	RO	0x0	reserved
0	RW	0x1	wr_poison_slverr_en If set to 1, enables SLVERR response for write transaction poisoning Programming Mode: Dynamic

DDRC_POISONSTAT

Address: Operational Base + offset (0x0370)

Bit	Attr	Reset Value	Description
31:17	RO	0x0	reserved
16	RO	0x0	rd_poison_intr_0 Read transaction poisoning error interrupt for port 0. This register is a APB clock copy (double register synchronizer) of the interrupt asserted when a transaction is poisoned on the corresponding AXI port's read address channel. Bit 0 corresponds to Port 0, and so on. Interrupt is cleared by register rd_poison_intr_clr, then value propagated to APB clock. Programming Mode: Dynamic
15:1	RO	0x0	reserved
0	RO	0x0	wr_poison_intr_0 Write transaction poisoning error interrupt for port 0. This register is a APB clock copy (double register synchronizer) of the interrupt asserted when a transaction is poisoned on the corresponding AXI port's write address channel. Bit 0 corresponds to Port 0, and so on. Interrupt is cleared by register wr_poison_intr_clr, then value propagated to APB clock. Programming Mode: Dynamic

DDRC_PSTAT

Address: Operational Base + offset (0x03fc)

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Bit	Attr	Reset Value	Description
31:17	RO	0x0	reserved
16	RO	0x0	wr_port_busy_0 Indicates if there are outstanding writes for AXI port 0. Programming Mode: Dynamic
15:1	RO	0x0	reserved
0	RO	0x0	rd_port_busy_0 Indicates if there are outstanding reads for AXI port 0. Programming Mode: Dynamic

DDRC_PCCFG

Address: Operational Base + offset (0x0400)

Bit	Attr	Reset Value	Description
31:9	RO	0x0	reserved
8	RW	0x0	bl_exp_mode Burst length expansion mode. By default (i.e. bl_exp_mode==0) XPI expands every AXI burst into multiple HIF commands, using the memory burst length as a unit. If set to 1, then XPI will use half of the memory burst length as a unit. This applies to both reads and writes. When MSTR.data_bus_width==00, setting bl_exp_mode to 1 has no effect. This can be used in cases where Partial Writes is enabled (UMCTL2_PARTIAL_WR=1), in order to avoid or minimize t_ccd_l penalty in DDR4 and t_ccd_mw penalty in LPDDR4. Hence, bl_exp_mode=1 is only recommended if DDR4 or LPDDR4. Note that if DBICTL.dm_en=0, functionality is not supported in the following cases: UMCTL2_PARTIAL_WR=0 UMCTL2_PARTIAL_WR=1, MSTR.data_bus_width=01, MEMC_BURST_LENGTH=8 and MSTR.burst_rdwr=1000 (LPDDR4 only) UMCTL2_PARTIAL_WR=1, MSTR.data_bus_width=01, MEMC_BURST_LENGTH=4 and MSTR.burst_rdwr=0100 (DDR4 only), with either MSTR.burstchop=0 or CRCPARCTL1.crc_enable=1 Programming Mode: Static
7:5	RO	0x0	reserved
4	RW	0x0	pagematch_limit Page match four limit. If set to 1, limits the number of consecutive same page DDRC transactions that can be granted by the Port Arbiter to four when Page Match feature is enabled. If set to 0, there is no limit imposed on number of consecutive same page DDRC transactions. Programming Mode: Static
3:1	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
0	RW	0x0	go2critical_en If set to 1 (enabled), sets co_gs_go2critical_wr and co_gs_go2critical_lpr / co_gs_go2critical_hpr signals going to DDRC based on urgent input (awurgent, arurgent) coming from AXI master. If set to 0 (disabled), co_gs_go2critical_wr and co_gs_go2critical_lpr / co_gs_go2critical_hpr signals at DDRC are driven to 1b'0. Programming Mode: Static

DDRC_PCFGR_0

Address: Operational Base + offset (0x0404)

Bit	Attr	Reset Value	Description
31:15	RO	0x0	reserved
14	RW	0x0	rd_port_pagematch_en If set to 1, enables the Page Match feature. If enabled, once a requesting port is granted, the port is continued to be granted if the following immediate commands are to the same memory page (same bank and same row). See also related PCCFG.pagematch_limit register. Programming Mode: Static
13	RW	0x0	rd_port_urgent_en If set to 1, enables the AXI urgent sideband signal (arurgent). When enabled and arurgent is asserted by the master, that port becomes the highest priority and co_gs_go2critical_lpr/co_gs_go2critical_hpr signal to DDRC is asserted if enabled in PCCFG.go2critical_en register. Note that arurgent signal can be asserted anytime and as long as required which is independent of address handshaking (it is not associated with any particular command). Programming Mode: Static
12	RW	0x0	rd_port_aging_en If set to 1, enables aging function for the read channel of the port. Programming Mode: Static
11:10	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
9:0	RW	0x000	rd_port_priority Determines the initial load value of read aging counters. These counters will be parallel loaded after reset, or after each grant to the corresponding port. The aging counters down-count every clock cycle where the port is requesting but not granted. The higher significant 5-bits of the read aging counter sets the priority of the read channel of a given port. Port's priority will increase as the higher significant 5-bits of the counter starts to decrease. When the aging counter becomes 0, the corresponding port channel will have the highest priority level (timeout condition -Priority0). For single port configurations, the aging counters are only used when they timeout (become 0) to force read-write direction switching. In this case, external dynamic priority input, arqos (for reads only) can still be used to set the DDRC read priority (2 priority levels: low priority read - LPR, high priority read - HPR) on a command by command basis. Note: The two LSBs of this register field are tied internally to 2'b00. Programming Mode: Static

DDRC_PCFGW_0

Address: Operational Base + offset (0x0408)

Bit	Attr	Reset Value	Description
31:15	RO	0x0	reserved
14	RW	0x1	wr_port_pagematch_en If set to 1, enables the Page Match feature. If enabled, once a requesting port is granted, the port is continued to be granted if the following immediate commands are to the same memory page (same bank and same row). See also related PCCFG.pagematch_limit register. Programming Mode: Static
13	RW	0x0	wr_port_urgent_en If set to 1, enables the AXI urgent sideband signal (awurgent). When enabled and awurgent is asserted by the master, that port becomes the highest priority and co_gs_go2critical_wr signal to DDRC is asserted if enabled in PCCFG.go2critical_en register. Note that awurgent signal can be asserted anytime and as long as required which is independent of address handshaking (it is not associated with any particular command). Programming Mode: Static
12	RW	0x0	wr_port_aging_en If set to 1, enables aging function for the write channel of the port. Programming Mode: Static
11:10	RO	0x0	reserved

Bit	Attr	Reset Value	Description
9:0	RW	0x000	wr_port_priority Determines the initial load value of write aging counters. These counters will be parallel loaded after reset, or after each grant to the corresponding port. The aging counters down-count every clock cycle where the port is requesting but not granted. The higher significant 5-bits of the write aging counter sets the initial priority of the write channel of a given port. Port's priority will increase as the higher significant 5-bits of the counter starts to decrease. When the aging counter becomes 0, the corresponding port channel will have the highest priority level. For single port configurations, the aging counters are only used when they timeout (become 0) to force read-write direction switching. Note: The two LSBs of this register field are tied internally to 2'b00. Programming Mode: Static

DDRC_PCTRL_0

Address: Operational Base + offset (0x0490)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	port_en Enables AXI port 0. Programming Mode: Dynamic

DDRPHY_REG0

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x0	channel select 4'b0011: DQ 16bit 4'b1111: DQ 32bit
3	RW	0x1	soft reset 1, active low
2	RW	0x1	soft reset 0, active low
1	RW	0x1	
0	RW	0x1	

DDRPHY_REG1

Address: Operational Base + offset (0x0004)

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Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4	RW	0x0	Read ODT bypass mode enable signal, High active. Releated register REG03 and REG04
3	RW	0x1	PHY burst type select: 1: burst8
2:0	RW	0x0	PHY working condition select 0x0: ddr2 PHY mode 0x1: lpddr2 PHY mode 0x2: ddr3 PHY mode 0x3: lpddr3 PHY mode 0x4: ddr4 PHY mode

DDRPHY_REG2

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:6	RW	0x0	Write leveling CS select signal 2'b00: select CS0 and CS1 2'b01: select CS1 2'b10: select CS0
5:4	RW	0x0	DQS gating calibration CS select signal 2'b00: select CS0 and CS1 2'b01: select CS1 2'b10: select CS0
3	RW	0x0	Write leveling calibration bypass mode, active high
2	RW	0x0	Write leveling calibration control, active high
1	RW	0x0	DQS gating calibration bypass mode, active high
0	RW	0x0	DQS gating calibration control, active high

DDRPHY_REG3

Address: Operational Base + offset (0x000c)

Bit	Attr	Reset Value	Description
31:7	RO	0x0	reserved
6:4	RW	0x2	right channel A read ODT delay by read odt configure bypass mode
3	RO	0x0	reserved
2:0	RW	0x2	left channel A read ODT delay by read odt configure bypass mode

DDRPHY_REG4

Address: Operational Base + offset (0x0010)

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Bit	Attr	Reset Value	Description
31:7	RO	0x0	reserved
6:4	RW	0x2	right channel B read ODT delay by read odt configure bypass mode
3	RO	0x0	reserved
2:0	RW	0x2	left channel B read ODT delay by read odt configure bypass mode

DDRPHY_REG5

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x00	Write leveling load mode[7:0]

DDRPHY_REG6

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:6	RW	0x0	Write leveling load mode select[1:0]
5:0	RW	0x02	Write leveling load mode[13:8]

DDRPHY_REG9

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:7	RO	0x0	reserved
6	RW	0x0	0: Normal mode; 1: Bypass
5:0	RO	0x0	reserved

DDRPHY_REGA

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5:0	RW	0x00	DDR2 /DDR3/DDR4 CAS Latency; LPDDR2/3 RL value

DDRPHY_REGB

Address: Operational Base + offset (0x002c)

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4:0	RW	0x00	DDR2/DDR3/DDR4 additive latency

DDRPHY_REGC

Address: Operational Base + offset (0x0030)

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Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4:0	RW	0x00	DDR2/DDR3/DDR4 WRITE CAS Latency; LPDDR2/3 WL value

DDRPHY_REG11

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4:0	RW	0x14	CMD NRCOMP, except for CK/CKB. The larger the value, the stronger the drive strength

DDRPHY_REG12

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:3	RW	0x14	CMD PRCOMP, except for CK/CKB. The larger the value, the stronger the driver strength
2	RO	0x0	reserved
1	RW	0x1	CMD weak pull up enable, active low
0	RW	0x0	CMD weak pull down enable, active high

DDRPHY_REG13

Address: Operational Base + offset (0x004c)

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4	RW	0x0	CMD DLL clock phase select in bypass mode 0: no delay 1: 90°delay
3	RW	0x1	CMD DLL enable 0: disable 1: enable
2:0	RW	0x4	CMD AND ADDRESS DLL delay 0: no delay 1: 22.5°delay 2: 45°delay 3: 67.5°delay 4: 90°delay 5: 112.5°delay 6: 135°delay 7: 157.5°delay

DDRPHY_REG14

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3	RW	0x1	CK DLL clock phase select in bypass mode 0: no delay 1: 90°delay

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Bit	Attr	Reset Value	Description
2:0	RW	0x0	CK DLL delay 0: no delay 1: 22.5°delay 2: 45°delay 3: 67.5°delay 4: 90°delay 5: 112.5°delay 6: 135°delay 7: 157.5°delay

DDRPHY_REG15

Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x00	

DDRPHY_REG16

Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4:0	RW	0x14	CK/CKB NRCOMP. The larger the value, the stronger the drive strength

DDRPHY_REG17

Address: Operational Base + offset (0x005c)

Bit	Attr	Reset Value	Description
31:7	RO	0x0	reserved
6:4	RW	0x4	CMD/CK falling edge slew rate control, larger value means larger falling slew rate
3	RO	0x0	reserved
2:0	RW	0x4	CMD/CK rising edge slew rate control, larger vale means larger rising slew rate

DDRPHY_REG18

Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4:0	RW	0x14	CK/CKB PRCOMP. The larger the value, the stronger the drive strength

DDRPHY_REG1B

Address: Operational Base + offset (0x006c)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x00	

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DDRPHY_REG1F

Address: Operational Base + offset (0x007c)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x3	The response timing when detect the dfi_lp_req is high. Unit: dfi_clk1x
3:0	RW	0x0	The response timing when high the dfi_lp_ack. Unit: dfi_clk1x

DDRPHY_REG20

Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4:0	RW	0x14	Left channel A NRCOMP. The larger the value, the stronger the drive strength in the scope from A_DQ0 to A_DQ7

DDRPHY_REG21

Address: Operational Base + offset (0x0084)

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4:0	RW	0x04	Left channel A read pull-up ODT. The larger the value, the smaller the pull-up resistance in the scope from A_DQ0 to A_DQ7

DDRPHY_REG22

Address: Operational Base + offset (0x0088)

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x1	Left channel A DQ weak pull up enable, active low
0	RW	0x0	Left channel A DQ weak pull down enable, active high

DDRPHY_REG26

Address: Operational Base + offset (0x0098)

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4	RW	0x0	Left channel A write DQ DLL phase select in bypass mode. 0: no delay 1: 90°delay
3	RW	0x1	Left channel A write DQ DLL enable, active HIGH
2:0	RW	0x4	Left channel A write DQ DLL delay 0: no delay 1: 22.5°delay 2: 45°delay 3: 67.5°delay 4: 90°delay 5: 112.5°delay 6: 135°delay 7: 157.5°delay

DDRPHY_REG27

Address: Operational Base + offset (0x009c)

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Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3	RW	0x0	Left channel A write DQS DLL phase select in bypass mode. 0: no delay 1: 90°delay
2:0	RW	0x0	Left channel A write DQS DLL delay 0: no delay 1: 22.5°delay 2: 45°delay 3: 67.5°delay 4: 90°delay 5: 112.5°delay 6: 135°delay 7: 157.5°delay

DDRPHY_REG28

Address: Operational Base + offset (0x00a0)

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1:0	RW	0x1	Left channel A read DQS DLL delay 0: no delay 1: 22.5°delay 2: 45°delay 3: 67.5°delay

DDRPHY_REG29

Address: Operational Base + offset (0x00a4)

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x1	Weak pull up of the A_DQS[0]
0	RW	0x0	Weak pull down of the A_DQS[0]. REG29[1:0]=2'b00. Pull Up REG29[1:0]=2'b01. Middle Level REG29[1:0]=2'b10. High-Z REG29[1:0]=2'b11. Pull Down

DDRPHY_REG2B

Address: Operational Base + offset (0x00ac)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:5	RW	0x4	Left channel A falling edge slew rate control, larger value means larger falling slew rate
4:2	RW	0x0	Left channel A rising edge slew rate control, larger value means larger rising slew rate
1:0	RW	0x1	

DDRPHY_REG2C

Address: Operational Base + offset (0x00b0)

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Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:5	RW	0x0	Write the cyclesel configure low 8bit of A channel when in calibartion bypass mode for CS0. Related register REG02[1]
4:3	RW	0x0	Write the ophsel configure low 8bit of A channel when in calibartion bypass mode for CS0. Related register REG02[1]
2:0	RW	0x0	Write the dll configure low 8bit of A channel when in calibartion bypass mode for CS0. Related register REG02[1]

DDRPHY_REG2D

Address: Operational Base + offset (0x00b4)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:5	RW	0x0	Write the cyclesel configure low 8bit of A channel when in calibartion bypass mode for CS1. Related register REG02[1]
4:3	RW	0x0	Write the ophsel configure low 8bit of A channel when in calibartion bypass mode for CS1. Related register REG02[1]
2:0	RW	0x0	Write the dll configure low 8bit of A channel when in calibartion bypass mode for CS1. Related register REG02[1]

DDRPHY_REG2E

Address: Operational Base + offset (0x00b8)

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4:0	RW	0x04	Left channel A read pull-up ODT. The larger the value, the smaller the pull-up resistance in the scope from A_DQ0 to A_DQ7

DDRPHY_REG2F

Address: Operational Base + offset (0x00bc)

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4:0	RW	0x14	Left channel A PRCOMP. The larger the value, the stronger the drive strength in the scope from A_DQ0 to A_DQ7

DDRPHY_REG30

Address: Operational Base + offset (0x00c0)

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4:0	RW	0x14	Right channel A NRCOMP. The larger the value, the stronger the drive strength in the scope from A_DQ8 to A_DQ15

DDRPHY_REG31

Address: Operational Base + offset (0x00c4)

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Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4:0	RW	0x04	Right channel A read pull-down ODT. The larger the value, the smaller the pull-down resistance in the scope from A_DQ8 to A_DQ15

DDRPHY_REG32

Address: Operational Base + offset (0x00c8)

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x1	Right channel A DQ weak pull up enable, active low
0	RW	0x0	Right channel A DQ weak pull down enable, active high

DDRPHY_REG36

Address: Operational Base + offset (0x00d8)

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4	RW	0x0	Right channel A write DQ DLL phase select in bypass mode 0: no delay 1: 90°delay
3	RW	0x0	Right channel A write DQ DLL enable, active high
2:0	RW	0x4	Right channel A write DQ DLL delay 0: no delay 1: 22.5°delay 2: 45°delay 3: 67.5°delay 4: 90°delay 5: 112.5°delay 6: 135°delay 7: 157.5°delay

DDRPHY_REG37

Address: Operational Base + offset (0x00dc)

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3	RW	0x0	Right channel A write DQS DLL phase select in bypass mode. 0: no delay 1: 90°delay
2:0	RW	0x0	Right channel A write DQS DLL delay 0: no delay 1: 22.5°delay 2: 45°delay 3: 67.5°delay 4: 90°delay 5: 112.5°delay 6: 135°delay 7: 157.5°delay

DDRPHY_REG38

Address: Operational Base + offset (0x00e0)

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Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1:0	RW	0x1	Right channel A read DQS DLL delay 0: no delay 1: 22.5°delay 2: 45°delay 3: 67.5°delay

DDRPHY_REG39

Address: Operational Base + offset (0x00e4)

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x1	Weak pull up of the A_DQS[1]
0	RW	0x0	Weak pull down of the A_DQS[1]. REG39[1:0] = 2'b00. Pull Up. REG39[1:0] =2'b01. Middle level. REG39[1:0] = 2'b10. High-Z. REG39[1:0] = 2'b11. Pull Down

DDRPHY_REG3A

Address: Operational Base + offset (0x00e8)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x01	

DDRPHY_REG3B

Address: Operational Base + offset (0x00ec)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:5	RW	0x4	Right channel A falling edge slew rate control, larger value means larger falling slew rate
4:2	RW	0x0	Right channel A rising edge slew rate control, larger value means larger rising slew rate
1:0	RW	0x1	

DDRPHY_REG3C

Address: Operational Base + offset (0x00f0)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:5	RW	0x0	Write the cyclesel configure high 8bit of A channel when in calibration bypass mode for CS0. Related register REG02[1]
4:3	RW	0x0	Write the ophsel configure high 8bit of A channel when in calibration bypass mode for CS0. Related register REG02[1]
2:0	RW	0x0	Write the dll configure high 8bit of A channel when in calibration bypass mode for CS0. Related register REG02[1]

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DDRPHY_REG3D

Address: Operational Base + offset (0x00f4)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:5	RW	0x0	Write the cyclesel configure high 8bit of A channel when in calibration bypass mode for CS1. Related register REG02[1]
4:3	RW	0x0	Write the ophsel configure high 8bit of A channel when in calibration bypass mode for CS1. Related register REG02[1]
2:0	RW	0x0	Write the dll configure high 8bit of A channel when in calibration bypass mode for CS1. Related register REG02[1]

DDRPHY_REG3E

Address: Operational Base + offset (0x00f8)

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4:0	RW	0x04	Right channel A read pull-up ODT. The larger the value, the smaller the pull-up resistance in the scope from A_DQ8 to A_DQ15

DDRPHY_REG3F

Address: Operational Base + offset (0x00fc)

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4:0	RW	0x14	Right channel A PRCOMP. The larger the value, the stronger the drive strength in the scope from A_DQ8 to A_DQ15

DDRPHY_REG40

Address: Operational Base + offset (0x0100)

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4:0	RW	0x14	Left channel B NRCOMP. The larger the value, the stronger the drive strength in the scope from B_DQ0 to B_DQ7

DDRPHY_REG41

Address: Operational Base + offset (0x0104)

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4:0	RW	0x04	Left channel B read pull-down ODT. The larger the value, the smaller the pull-down resistance in the scope from B_DQ0 to B_DQ7

DDRPHY_REG42

Address: Operational Base + offset (0x0108)

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Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x0	Left channel B DQ weak pull up enable, active low
0	RW	0x0	Left channel B DQ weak pull down enable, active high

DDRPHY_REG46

Address: Operational Base + offset (0x0118)

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4	RW	0x0	Left channel B write DQ DLL phase select in bypass mode. 0: no delay 1: 90°delay
3	RW	0x1	Left channel B write DQ DLL enable, active HIGH
2:0	RW	0x4	Left channel B write DQ DLL delay 0: no delay 1: 22.5°delay 2: 45°delay 3: 67.5°delay 4: 90°delay 5: 112.5°delay 6: 135°delay 7: 157.5°delay

DDRPHY_REG47

Address: Operational Base + offset (0x011c)

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3	RW	0x0	Left channel B write DQS DLL phase select in bypass mode. 0: no delay 1: 90°delay
2:0	RW	0x0	Left channel B write DQS DLL delay 0: no delay 1: 22.5°delay 2: 45°delay 3: 67.5°delay 4: 90°delay 5: 112.5°delay 6: 135°delay 7: 157.5°delay

DDRPHY_REG48

Address: Operational Base + offset (0x0120)

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1:0	RW	0x1	Left channel B read DQS DLL delay 0: no delay 1: 22.5°delay 2: 45°delay 3: 67.5°delay

DDRPHY_REG49

Address: Operational Base + offset (0x0124)

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x1	Weak pull up of the B_DQS[0]

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Bit	Attr	Reset Value	Description
0	RW	0x0	Weak pull down of the B_DQS[0]. REG49[1:0] = 2'b00. Pull Up. REG49[1:0] =2'b01. Middle level. REG49[1:0] = 2'b10. High-Z. REG49[1:0] = 2'b11. Pull Down

DDRPHY_REG4A

Address: Operational Base + offset (0x0128)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x01	

DDRPHY_REG4B

Address: Operational Base + offset (0x012c)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:5	RW	0x4	Left channel B falling edge slew rate control, larger value means larger falling slew rate
4:2	RW	0x4	Left channel B rising edge slew rate control, larger value means larger rising slew rate
1:0	RW	0x1	

DDRPHY_REG4C

Address: Operational Base + offset (0x0130)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:5	RW	0x0	Write the cyclesel configure low 8bit of B channel when in calibration bypass mode for CS0. Related register REG02[1]
4:3	RW	0x0	Write the ophsel configure low 8bit of B channel when in calibration bypass mode for CS0. Related register REG02[1]
2:0	RW	0x0	Write the dll configure low 8bit of B channel when in calibration bypass mode for CS0. Related register REG02[1]

DDRPHY_REG4D

Address: Operational Base + offset (0x0134)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:5	RW	0x0	Write the cyclesel configure low 8bit of B channel when in calibration bypass mode for CS1. Related register REG02[1]
4:3	RW	0x0	Write the ophsel configure low 8bit of B channel when in calibration bypass mode for CS1. Related register REG02[1]
2:0	RW	0x0	Write the dll configure low 8bit of B channel when in calibration bypass mode for CS1. Related register REG02[1]

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DDRPHY_REG4E

Address: Operational Base + offset (0x0138)

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4:0	RW	0x04	Left channel B read pull-up ODT. The larger the value, the smaller the pull-up resistance in the scope from B_DQ0 to B_DQ7

DDRPHY_REG4F

Address: Operational Base + offset (0x013c)

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4:0	RW	0x14	Left channel B PRCOMP. The larger the value, the stronger the drive strength in the scope from B_DQ0 to B_DQ7

DDRPHY_REG50

Address: Operational Base + offset (0x0140)

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4:0	RW	0x14	Right channel B NRCOMP. The larger the value, the stronger the drive strength in the scope from B_DQ8 to B_DQ15

DDRPHY_REG51

Address: Operational Base + offset (0x0144)

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4:0	RW	0x04	Right channel B read pull-down ODT. The larger the value, the smaller the pull-down resistance in the scope from B_DQ8 to B_DQ15

DDRPHY_REG52

Address: Operational Base + offset (0x0148)

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x1	Right channel B DQ weak pull up enable, active low
0	RW	0x0	Right channel B DQ weak pull down enable, active high

DDRPHY_REG56

Address: Operational Base + offset (0x0158)

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4	RW	0x0	Right channel B write DQ DLL phase select in bypass mode. 0: no delay 1: 90°delay
3	RW	0x1	Right channel B write DQ DLL enable, active HIGH

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Bit	Attr	Reset Value	Description
2:0	RW	0x4	Right channel B write DQ DLL delay 0: no delay 1: 22.5°delay 2: 45°delay 3: 67.5°delay 4: 90°delay 5: 112.5°delay 6: 135°delay 7: 157.5°delay

DDRPHY_REG57

Address: Operational Base + offset (0x015c)

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3	RW	0x0	Right channel B write DQS DLL phase select in bypass mode. 0: no delay 1: 90°delay
2:0	RW	0x0	Right channel B write DQS DLL delay 0: no delay 1: 22.5°delay 2: 45°delay 3: 67.5°delay 4: 90°delay 5: 112.5°delay 6: 135°delay 7: 157.5°delay

DDRPHY_REG58

Address: Operational Base + offset (0x0160)

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1:0	RW	0x1	Right channel B read DQS DLL delay 0: no delay 1: 22.5°delay 2: 45°delay 3: 67.5°delay

DDRPHY_REG59

Address: Operational Base + offset (0x0164)

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x1	Weak pull up of the B_DQS[1]
0	RW	0x0	Weak pull down of the B_DQS[1]. REG59[1:0] = 2'b00. Pull Up. REG59[1:0] =2'b01. Middle level. REG59[1:0] = 2'b10. High-Z. REG59[1:0] = 2'b11. Pull Down

DDRPHY_REG5A

Address: Operational Base + offset (0x0168)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x01	

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DDRPHY_REG5B

Address: Operational Base + offset (0x016c)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:5	RW	0x4	Right channel B falling edge slew rate control, larger value means larger falling slew rate
4:2	RW	0x4	Right channel B rising edge slew rate control, larger value means larger rising slew rate
1:0	RW	0x1	

DDRPHY_REG5C

Address: Operational Base + offset (0x0170)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:5	RW	0x0	Write the cyclesel configure high 8bit of B channel when in calibration bypass mode for CS0. Related register REG02[1]
4:3	RW	0x0	Write the ophsel configure high 8bit of B channel when in calibration bypass mode for CS0. Related register REG02[1]
2:0	RW	0x0	Write the dll configure high 8bit of B channel when in calibration bypass mode for CS0. Related register REG02[1]

DDRPHY_REG5D

Address: Operational Base + offset (0x0174)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:5	RW	0x0	Write the cyclesel configure high 8bit of B channel when in calibration bypass mode for CS1. Related register REG02[1]
4:3	RW	0x0	Write the ophsel configure high 8bit of B channel when in calibration bypass mode for CS1. Related register REG02[1]
2:0	RW	0x0	Write the dll configure high 8bit of B channel when in calibration bypass mode for CS1. Related register REG02[1]

DDRPHY_REG5E

Address: Operational Base + offset (0x0178)

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4:0	RW	0x04	Right channel B read pull-up ODT. The larger the value, the smaller the pull-up resistance in the scope from B_DQ8 to B_DQ15

DDRPHY_REG5F

Address: Operational Base + offset (0x017c)

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Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4:0	RW	0x14	Right channel B PRCOMP. The larger the value, the stronger the drive strength in the scope from B_DQ8 to B_DQ15

DDRPHY_REG70

Address: Operational Base + offset (0x01c0)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x7	CS0 A_DM0 RX de-skew
3:0	RW	0x7	CS0 A_DM0 TX de-skew

DDRPHY_REG71

Address: Operational Base + offset (0x01c4)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x7	CS0 A_DQ0 RX de-skew
3:0	RW	0x7	CS0 A_DQ0 TX de-skew

DDRPHY_REG72

Address: Operational Base + offset (0x01c8)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x7	CS0 A_DQ1 RX de-skew
3:0	RW	0x7	CS0 A_DQ1 TX de-skew

DDRPHY_REG73

Address: Operational Base + offset (0x01cc)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x7	CS0 A_DQ2 RX de-skew
3:0	RW	0x7	CS0 A_DQ2 TX de-skew

DDRPHY_REG74

Address: Operational Base + offset (0x01d0)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x7	CS0 A_DQ3 RX de-skew
3:0	RW	0x7	CS0 A_DQ3 TX de-skew

DDRPHY_REG75

Address: Operational Base + offset (0x01d4)

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Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x7	CS0 A_DQ4 RX de-skew
3:0	RW	0x7	CS0 A_DQ4 TX de-skew

DDRPHY_REG76

Address: Operational Base + offset (0x01d8)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x7	CS0 A_DQ5 RX de-skew
3:0	RW	0x7	CS0 A_DQ5 TX de-skew

DDRPHY_REG77

Address: Operational Base + offset (0x01dc)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x7	CS0 A_DQ6 RX de-skew
3:0	RW	0x7	CS0 A_DQ6 TX de-skew

DDRPHY_REG78

Address: Operational Base + offset (0x01e0)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x7	CS0 A_DQ7 RX de-skew
3:0	RW	0x7	CS0 A_DQ7 TX de-skew

DDRPHY_REG79

Address: Operational Base + offset (0x01e4)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x7	CS0 A_DQS0 RX de-skew
3:0	RW	0x7	CS0 A_DQS0 TX de-skew

DDRPHY_REG7A

Address: Operational Base + offset (0x01e8)

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3:0	RW	0x7	CS0 A_DQSB0 TX de-skew

DDRPHY_REG7B

Address: Operational Base + offset (0x01ec)

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Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x7	CS0 A_DM1 RX de-skew
3:0	RW	0x7	CS0 A_DM1 TX de-skew

DDRPHY_REG7C

Address: Operational Base + offset (0x01f0)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x7	CS0 A_DQ8 RX de-skew
3:0	RW	0x7	CS0 A_DQ8 TX de-skew

DDRPHY_REG7D

Address: Operational Base + offset (0x01f4)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x7	CS0 A_DQ9 RX de-skew
3:0	RW	0x7	CS0 A_DQ9 TX de-skew

DDRPHY_REG7E

Address: Operational Base + offset (0x01f8)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x7	CS0 A_DQ10 RX de-skew
3:0	RW	0x7	CS0 A_DQ10 TX de-skew

DDRPHY_REG7F

Address: Operational Base + offset (0x01fc)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x7	CS0 A_DQ11 RX de-skew
3:0	RW	0x7	CS0 A_DQ11 TX de-skew

DDRPHY_REG80

Address: Operational Base + offset (0x0200)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x7	CS0 A_DQ12 RX de-skew
3:0	RW	0x7	CS0 A_DQ12 TX de-skew

DDRPHY_REG81

Address: Operational Base + offset (0x0204)

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Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x7	CS0 A_DQ13 RX de-skew
3:0	RW	0x7	CS0 A_DQ13 TX de-skew

DDRPHY_REG82

Address: Operational Base + offset (0x0208)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x7	CS0 A_DQ14 RX de-skew
3:0	RW	0x7	CS0 A_DQ14 TX de-skew

DDRPHY_REG83

Address: Operational Base + offset (0x020c)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x7	CS0_A_DQ15 RX de-skew
3:0	RW	0x7	CS0 A_DQ15 TX de-skew

DDRPHY_REG84

Address: Operational Base + offset (0x0210)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x7	CS0 A_DQS1 RX de-skew
3:0	RW	0x7	CS0 A_DQS1 TX de-skew

DDRPHY_REG85

Address: Operational Base + offset (0x0214)

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3:0	RW	0x7	CS0 A_DQSB1 TX de-ske

DDRPHY_REG86

Address: Operational Base + offset (0x0218)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x7	CS0 B_DM0 RX de-skew
3:0	RW	0x7	CS0 B_DM0 TX de-skew

DDRPHY_REG87

Address: Operational Base + offset (0x021c)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x7	CS0 B_DQ0 RX de-skew
3:0	RW	0x7	CS0 B_DQ0 TX de-skew

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DDRPHY_REG88

Address: Operational Base + offset (0x0220)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x7	CS0 B_DQ1 RX de-skew
3:0	RW	0x7	CS0 B_DQ1 TX de-skew

DDRPHY_REG89

Address: Operational Base + offset (0x0224)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x7	CS0 B_DQ2 RX de-skew
3:0	RW	0x7	FCS0 B_DQ2 TX de-skew

DDRPHY_REG8A

Address: Operational Base + offset (0x0228)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x7	CS0 B_DQ3 RX de-skew
3:0	RW	0x7	CS0 B_DQ3 TX de-skew

DDRPHY_REG8B

Address: Operational Base + offset (0x022c)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x7	CS0 B_DQ4 RX de-skew
3:0	RW	0x7	CS0 B_DQ4 TX de-skew

DDRPHY_REG8C

Address: Operational Base + offset (0x0230)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x7	CS0 B_DQ5 RX de-skew
3:0	RW	0x7	CS0 B_DQ5 TX de-skew

DDRPHY_REG8D

Address: Operational Base + offset (0x0234)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x7	CS0 B_DQ6 RX de-skew
3:0	RW	0x7	CS0 B_DQ6 TX de-skew

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DDRPHY_REG8E
Address: Operational Base + offset (0x0238)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x7	CS0 B_DQ7 RX de-skew
3:0	RW	0x7	CS0 B_DQ7 TX de-skew

DDRPHY_REG8F
Address: Operational Base + offset (0x023c)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x7	CS0 B_DQS0 RX de-skew
3:0	RW	0x7	CS0 B_DQS0 TX de-skew

DDRPHY_REG90
Address: Operational Base + offset (0x0240)

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3:0	RW	0x7	CS0 B_DQSB0 TX de-skew

DDRPHY_REG91
Address: Operational Base + offset (0x0244)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x7	CS0 B_DM1 RX de-skew
3:0	RW	0x7	CS0 B_DM1 TX de-skew

DDRPHY_REG92
Address: Operational Base + offset (0x0248)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x7	CS0 B_DQ8 RX de-skew
3:0	RW	0x7	CS0 B_DQ8 TX de-skew

DDRPHY_REG93
Address: Operational Base + offset (0x024c)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x7	CS0 B_DQ9 RX de-skew
3:0	RW	0x7	CS0 B_DQ9 TX de-skew

DDRPHY_REG94
Address: Operational Base + offset (0x0250)

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Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x7	CS0 B_DQ10 RX de-skew
3:0	RW	0x7	CS0 B_DQ10 TX de-skew

DDRPHY_REG95

Address: Operational Base + offset (0x0254)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x7	CS0 B_DQ11 RX de-skew
3:0	RW	0x7	CS0 B_DQ11 TX de-skew

DDRPHY_REG96

Address: Operational Base + offset (0x0258)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x7	CS0 B_DQ12 RX de-skew
3:0	RW	0x7	CS0 B_DQ12 TX de-skew

DDRPHY_REG97

Address: Operational Base + offset (0x025c)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x7	CS0 B_DQ13 RX de-skew
3:0	RW	0x7	CS0 B_DQ13 TX de-skew

DDRPHY_REG98

Address: Operational Base + offset (0x0260)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x7	CS0 B_DQ14 RX de-skew
3:0	RW	0x7	CS0 B_DQ14 TX de-skew

DDRPHY_REG99

Address: Operational Base + offset (0x0264)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x7	CS0 B_DQ15 RX de-skew
3:0	RW	0x7	CS0 B_DQ15 TX de-skew

DDRPHY_REG9A

Address: Operational Base + offset (0x0268)

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Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x7	CS0 B_DQS1 RX de-skew
3:0	RW	0x7	

DDRPHY_REG9B

Address: Operational Base + offset (0x026c)

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3:0	RW	0x7	CS0 B_DQSB1 TX de-skew

DDRPHY_REGA3

Address: Operational Base + offset (0x028c)

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5	RW	0x1	Channel A 16bit DQ VREF select 1: internal mode; 0: external mode
4:0	RW	0x10	Channel A 16bit DQ VREF value. VREF value=(reg_value/32)*VDDQ

DDRPHY_REGAE

Address: Operational Base + offset (0x02b8)

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5	RW	0x0	Channel B 16bit DQ VREF select. 1: internal mode 0: external mode
4:0	RW	0x00	Channel B 16bit DQ VREF value VREF value=(reg_value/32)*VDDQ

DDRPHY_REGB0

Address: Operational Base + offset (0x02c0)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x7	A1 de-skew
3:0	RW	0x7	A0 de-skew

DDRPHY_REGB1

Address: Operational Base + offset (0x02c4)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x7	A3 de-skew
3:0	RW	0x7	A2 de-skew

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DDRPHY_REGB2

Address: Operational Base + offset (0x02c8)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x7	A5 de-skew
3:0	RW	0x7	A4 de-skew

DDRPHY_REGB3

Address: Operational Base + offset (0x02cc)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x7	A7 de-skew
3:0	RW	0x7	A6 de-skew

DDRPHY_REGB4

Address: Operational Base + offset (0x02d0)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x7	A9 de-skew
3:0	RW	0x7	A8 de-skew

DDRPHY_REGB5

Address: Operational Base + offset (0x02d4)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x7	A11 de-skew
3:0	RW	0x7	A10 de-skew

DDRPHY_REGB6

Address: Operational Base + offset (0x02d8)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x7	A13 de-skew
3:0	RW	0x7	A12 de-skew

DDRPHY_REGB7

Address: Operational Base + offset (0x02dc)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x7	A15 de-skew
3:0	RW	0x7	A14 de-skew

DDRPHY_REGB8

Address: Operational Base + offset (0x02e0)

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Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x7	B1 de-skew
3:0	RW	0x7	B0 de-skew

DDRPHY_REGB9

Address: Operational Base + offset (0x02e4)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x7	RAS# de-skew
3:0	RW	0x7	B2 de-skew

DDRPHY_REGBA

Address: Operational Base + offset (0x02e8)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x7	WE# de-skew
3:0	RW	0x7	CAS# de-skew

DDRPHY_REGBB

Address: Operational Base + offset (0x02ec)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x7	CKB de-skew
3:0	RW	0x7	CK de-skew

DDRPHY_REGBC

Address: Operational Base + offset (0x02f0)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x7	CKE de-skew
3:0	RW	0x7	ODT0 de-skew

DDRPHY_REGBD

Address: Operational Base + offset (0x02f4)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x7	CSB0 de-skew
3:0	RW	0x7	RESETN de-skew

DDRPHY_REGBE

Address: Operational Base + offset (0x02f8)

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Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x7	CSB1 de-skew
3:0	RW	0x7	ODT1 de-skew

DDRPHY_REGC0

Address: Operational Base + offset (0x0300)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x7	CS1 A_DM0 RX de-skew
3:0	RW	0x7	CS1 A_DM0 TX de-skew

DDRPHY_REGC1

Address: Operational Base + offset (0x0304)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x7	CS1 A_DQ0 RX de-skew
3:0	RW	0x7	CS1 A_DQ0 TX de-skew

DDRPHY_REGC2

Address: Operational Base + offset (0x0308)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x7	CS1 A_DQ1 RX de-skew
3:0	RW	0x7	CS1 A_DQ1 TX de-skew

DDRPHY_REGC3

Address: Operational Base + offset (0x030c)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x7	CS1 A_DQ2 RX de-skew
3:0	RW	0x7	CS1 A_DQ2 TX de-skew

DDRPHY_REGC4

Address: Operational Base + offset (0x0310)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x7	CS1 A_DQ3 RX de-skew
3:0	RW	0x7	CS1 A_DQ3 TX de-skew

DDRPHY_REGC5

Address: Operational Base + offset (0x0314)

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Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x7	CS1 A_DQ4 RX de-skew
3:0	RW	0x7	CS1 A_DQ4 TX de-skew

DDRPHY_REGC6

Address: Operational Base + offset (0x0318)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x7	CS1 A_DQ5 RX de-skew
3:0	RW	0x7	CS1 A_DQ5 TX de-skew

DDRPHY_REGC7

Address: Operational Base + offset (0x031c)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x7	CS1 A_DQ6 RX de-skew
3:0	RW	0x7	CS1 A_DQ6 TX de-skew

DDRPHY_REGC8

Address: Operational Base + offset (0x0320)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x7	CS1 A_DQ7 RX de-skew
3:0	RW	0x7	CS1 A_DQ7 TX de-skew

DDRPHY_REGC9

Address: Operational Base + offset (0x0324)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x7	CS1 A_DQS0 RX de-skew
3:0	RW	0x7	CS1 A_DQS0 TX de-skew

DDRPHY_REGCA

Address: Operational Base + offset (0x0328)

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3:0	RW	0x7	CS1 A_DQSB0 TX de-skew

DDRPHY_REGCB

Address: Operational Base + offset (0x032c)

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Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x7	CS1 A_DM1 RX de-skew
3:0	RW	0x7	CS1 A_DM1 TX de-skew

DDRPHY_REGCC

Address: Operational Base + offset (0x0330)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x7	CS1 A_DQ8 RX de-skew
3:0	RW	0x7	CS1 A_DQ8 TX de-skew

DDRPHY_REGCD

Address: Operational Base + offset (0x0334)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x7	CS1 A_DQ9 RX de-skew
3:0	RW	0x7	CS1 A_DQ9 TX de-skew

DDRPHY_REGCE

Address: Operational Base + offset (0x0338)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x7	CS1 A_DQ10 RX de-skew
3:0	RW	0x7	CS1 A_DQ10 TX de-skew

DDRPHY_REGCF

Address: Operational Base + offset (0x033c)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x7	CS1 A_DQ11 RX de-skew
3:0	RW	0x7	CS1 A_DQ11 TX de-skew

DDRPHY_REGD0

Address: Operational Base + offset (0x0340)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x7	CS1 A_DQ12 RX de-skew
3:0	RW	0x7	CS1 A_DQ12 TX de-skew

DDRPHY_REGD1

Address: Operational Base + offset (0x0344)

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Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x7	CS1 A_DQ13 RX de-skew
3:0	RW	0x7	CS1 A_DQ13 TX de-skew

DDRPHY_REGD2

Address: Operational Base + offset (0x0348)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x7	CS1 A_DQ14 RX de-skew
3:0	RW	0x7	CS1 A_DQ14 TX de-skew

DDRPHY_REGD3

Address: Operational Base + offset (0x034c)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x7	A_DQ15 RX de-skew
3:0	RW	0x7	CS1 A_DQ15 TX de-skew

DDRPHY_REGD4

Address: Operational Base + offset (0x0350)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x7	CS1 A_DQS1 RX de-skew
3:0	RW	0x7	CS1 A_DQS1 TX de-skew

DDRPHY_REGD5

Address: Operational Base + offset (0x0354)

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3:0	RW	0x7	CS1 A_DQSB1 TX de-skew

DDRPHY_REGD6

Address: Operational Base + offset (0x0358)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x7	CS1 B_DM0 RX de-skew
3:0	RW	0x7	CS1 B_DM0 TX de-skew

DDRPHY_REGD7

Address: Operational Base + offset (0x035c)

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Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x7	CS1 B_DQ0 RX de-skew
3:0	RW	0x7	CS1 B_DQ0 TX de-skew

DDRPHY_REGD8

Address: Operational Base + offset (0x0360)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x7	CS1 B_DQ1 RX de-skew
3:0	RW	0x7	CS1 B_DQ1 TX de-skew

DDRPHY_REGD9

Address: Operational Base + offset (0x0364)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x7	CS1 B_DQ2 RX de-skew
3:0	RW	0x7	CS1 B_DQ2 TX de-skew

DDRPHY_REGDA

Address: Operational Base + offset (0x0368)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x7	CS1 B_DQ3 RX de-skew
3:0	RW	0x7	CS1 B_DQ3 TX de-skew

DDRPHY_REGDB

Address: Operational Base + offset (0x036c)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x7	CS1 B_DQ4 RX de-skew
3:0	RW	0x7	CS1 B_DQ4 TX de-skew

DDRPHY_REGDC

Address: Operational Base + offset (0x0370)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x7	CS1 B_DQ5 RX de-skew
3:0	RW	0x7	CS1 B_DQ5 TX de-skew

DDRPHY_REGDD

Address: Operational Base + offset (0x0374)

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Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x7	CS1 B_DQ6 RX de-skew
3:0	RW	0x7	CS1 B_DQ6 TX de-skew

DDRPHY_REGDE

Address: Operational Base + offset (0x0378)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x7	CS1 B_DQ7 RX de-skew
3:0	RW	0x0	CS1 B_DQ7 TX de-skew

DDRPHY_REGDF

Address: Operational Base + offset (0x037c)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x7	CS1 B_DQS0 RX de-skew
3:0	RW	0x7	CS1 B_DQS0 TX de-skew

DDRPHY_REGE0

Address: Operational Base + offset (0x0380)

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3:0	RW	0x7	CS1 B_DQSB0 TX de-skew

DDRPHY_REGE1

Address: Operational Base + offset (0x0384)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x7	CS1 B_DM1 RX de-skew
3:0	RW	0x7	CS1 B_DM1 TX de-skew

DDRPHY_REGE2

Address: Operational Base + offset (0x0388)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x7	CS1 B_DQ8 RX de-skew
3:0	RW	0x7	CS1 B_DQ8 TX de-skew

DDRPHY_REGE3

Address: Operational Base + offset (0x038c)

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Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x7	CS1 B_DQ9 RX de-skew
3:0	RW	0x7	CS1 B_DQ9 TX de-skew

DDRPHY_REGE4

Address: Operational Base + offset (0x0390)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x7	CS1 B_DQ10 RX de-skew
3:0	RW	0x7	CS1 B_DQ10 TX de-skew

DDRPHY_REGE5

Address: Operational Base + offset (0x0394)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x7	CS1 B_DQ11 RX de-skew
3:0	RW	0x7	CS1 B_DQ11 TX de-ske

DDRPHY_REGE6

Address: Operational Base + offset (0x0398)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x7	CS1 B_DQ12 RX de-skew
3:0	RW	0x7	CS1 B_DQ12 TX de-skew

DDRPHY_REGE7

Address: Operational Base + offset (0x039c)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x7	CS1 B_DQ13 RX de-skew
3:0	RW	0x7	CS1 B_DQ13 TX de-skew

DDRPHY_REGE8

Address: Operational Base + offset (0x03a0)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x7	CS1 B_DQ14 RX de-skew
3:0	RW	0x7	CS1 B_DQ14 TX de-skew

DDRPHY_REGE9

Address: Operational Base + offset (0x03a4)

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Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x7	CS1 B_DQ15 RX de-skew
3:0	RW	0x7	CS1 B_DQ15 TX de-skew

DDRPHY_REGEA

Address: Operational Base + offset (0x03a8)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x7	CS1 B_DQS1 RX de-skew
3:0	RW	0x7	CS1 B_DQS1 TX de-skew

DDRPHY_REGEB

Address: Operational Base + offset (0x03ac)

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3:0	RW	0x7	CS1 B_DQSB1 TX de-skew

DDRPHY_REGEC

Address: Operational Base + offset (0x03b0)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x00	

DDRPHY_REGF0

Address: Operational Base + offset (0x03c0)

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3	RO	0x0	Channel B High 8bit write leveling done
2	RO	0x0	Channel B Low 8bit write leveling done
1	RO	0x0	Channel A High 8bit write leveling done
0	RO	0x0	Channel A Low 8bit write leveling done

DDRPHY_REGF1

Address: Operational Base + offset (0x03c4)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RO	0x0	Channel A High 8bit write leveling dqs value
3:0	RO	0x0	Channel A Low 8bit write leveling dqs value

DDRPHY_REGF2

Address: Operational Base + offset (0x03c8)

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Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RO	0x0	Channel B High 8bit write leveling dqs value
3:0	RO	0x0	Channel B Low 8bit write leveling dqs value

DDRPHY_REGF3

Address: Operational Base + offset (0x03cc)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RO	0x0	Channel A High 8bit write leveling dqs value for CS1
3:0	RO	0x0	Channel A Low 8bit write leveling dqs value for CS1

DDRPHY_REGF4

Address: Operational Base + offset (0x03d0)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RO	0x0	Channel B High 8bit write leveling dqs value for CS1
3:0	RO	0x0	Channel B Low 8bit write leveling dqs value for CS1

DDRPHY_REGFA

Address: Operational Base + offset (0x03e8)

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3	RO	0x0	Channel B High 8bit dqs gate sample dqs value(idqs) (3)
2	RO	0x0	Channel B Low 8bit dqs gate sample dqs value(idqs) (3)
1	RO	0x0	Channel A High 8bit dqs gate sample dqs value(idqs) (3)
0	RO	0x0	Channel A Low 8bit dqs gate sample dqs value(idqs) (3)

DDRPHY_REGFB

Address: Operational Base + offset (0x03ec)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:5	RO	0x0	Calibration get the dll configure channel A low 8bit(3)
4:3	RO	0x0	Calibration get the ophsel configure channel A low 8bit(3)
2:0	RO	0x0	Calibration get the cyclesel configure channel A low 8bit(3)

DDRPHY_REGFC

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Address: Operational Base + offset (0x03f0)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:5	RO	0x0	Calibration get the dll configure channel A high 8bit(3)
4:3	RO	0x0	Calibration get the ophsel configure channel A high 8bit(3)
2:0	RO	0x0	Calibration get the cyclesel configure channel A high 8bit(3)

DDRPHY_REGFD

Address: Operational Base + offset (0x03f4)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:5	RO	0x0	Calibration get the dll configure channel B low 8bit(3)
4:3	RO	0x0	Calibration get the ophsel configure channel B low 8bit(3)
2:0	RO	0x0	Calibration get the cyclesel configure channel B low 8bit(3)

DDRPHY_REGFE

Address: Operational Base + offset (0x03f8)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:5	RO	0x0	Calibration get the dll configure channel B high 8bit(3)
4:3	RO	0x0	Calibration get the ophsel configure channel B high 8bit(3)
2:0	RO	0x0	Calibration get the cyclesel configure channel B high 8bit(3)

DDRPHY_REGFF

Address: Operational Base + offset (0x03fc)

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3	RO	0x0	Channel B High 8bit Calibration done
2	RO	0x0	Channel B Low 8bit Calibration done
1	RO	0x0	Channel A High 8bit Calibration done
0	RO	0x0	Channel A Low 8bit Calibration done

2.5 Interface Description

DDR IOs are listed as following Table.

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Table 2-1DDR IO description

Pin Name	Description
CK	Positive differential clock
CKB	Negative differential clock
CKE	Active-high clock enable signal for two chip select.
CSBi (i=0,1)	Active-low chip select signal. There are two chip select.
RASB	Active-low row address strobe
CASB	Active-low column address strobe
WEB	Active-low write enable strobe
BA[2:0]	Bank address signal
A[15:0]	Address signal
DQ[31:0]	Bidirectional data line
DQS[3:0]	Positive differential bidirectional data strobes
DQSB[3:0]	Negative differential bidirectional data strobes.
DM[3:0]	Active-low data mask signal.
ODTi (i=0,1)	On-Die Termination output signal for two chip select.
RESETN	Reset signal.

The DDR4 Interface of DDR PHY is reused with DDR3/DDR3L, so the mapping relation between the DDR4 and DDR3/DDR3L show in the following table

Table 2-2DDR4 IO Mapping Table

DDR4	DDR3/DDR3L
A0	A9
A1	A14
A2	A13
A3	A11
A4	A2
A5	A4
A6	A3
A7	A6
A8	A5
A9	A1
A10	A0
A11	A7
A12	CASB
A13	A8
WEB/A14	ODT0
CASB/A15	BA1
RASB/A16	CKE
BA0	BA2
BA1	A12
BG0	BA0
CK	CK
CKB	CKB
CKE	RASB
CSB0	A10
ODT0	A15
ACTN	CSB0
RESETN	RESETN
ODT1	ODT1
CSB1	CSB1
BG1	WEB

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2.6 Application Notes

2.6.1 Initialization

PCTL & DDR PHY Initialization

1. Assert the resets (presentn, core_ddrc_rstn and aresetn_0 of PCTL)
2. Configure PLL of DDR PHY and wait PLL lock.
3. De-assert presetn if clocks are active and stable.
4. Initial PCTL register and PHY Register
5. Start PHY initialization with DFIMIS[5] register of PCTL
6. De-assert the remaining resets (core_ddrc_rstn and aresetn_0 of PCTL)
7. Wait PCTL initialization done (STAT.operation_mode==normal)
8. Start PHY dqs calibration with PHYREG02 register and wait calibration finish with PHYREGFF register.
9. (optional) After dqs calibration, start write leveling training with PHYREG02 register and wait write leveling training finish with PHYJREGF0 register.
10. Start Write and Read.

DDR3/DDR3L Initialization Sequence

The initialization steps for DDR3/DDR3L SDRAMs are as follows:
1. Power-up.
2. Maintain dfi_reset_n low for duration specified by INIT1.dram_rstn_x1024. Specification requires at least 200 us with stable power.
3. Issue NOP/deselect for duration specified by INIT0.pre_cke_x1024. Specification requires at least 500 us.
4. Assert CKE and issue NOP/deselect for INIT0.post_cke_x1024 (specification requires at least tXPR).
5. Issue MRS (mode register set) command to load MR2 with INIT4.emr2 value followed by NOP/deselect for duration of DRAMTMG3.t_mrd.
6. Issue MRS command to load MR3 with INIT4.emr3 followed by NOP/deselect for duration of DRAMTMG3.t_mrd.
7. Issue MRS command to load MR1 with INIT4.emr followed by NOP/deselect for duration of DRAMTMG3.t_mrd.
8. Issue MRS command to load MR0 with INIT3.mr followed by NOP/deselect for duration of DRAMTMG3.t_mod.
9. Issue ZQCL command to start ZQ calibration and wait for INIT5.dev_zqinit_x32.
10. Wait for INIT5.dev_zqinit_x32 counting to finish. Ensure wait from step 8 is larger than tDLLK.
11. The PCTL controller is now ready for normal operation.

DDR4 Initialization Sequence

The initialization steps for DDR4 SDRAMs are as follows:
1. Power-up.
2. Maintain dfi_reset_n low for duration specified by INIT1.dram_rstn_x1024. Specification requires at least 200 us with stable power.
3. Issue NOP/deselect for duration specified by INIT0.pre_cke_x1024. Specification requires at least 500 us.
4. Assert CKE and issue NOP/deselect for INIT0.post_cke_x1024 (specification requires at least tXPR).
5. Issue MRS (mode register set) command to load MR3 with INIT4.emr3 value followed by NOP/deselect for duration of DRAMTMG3.t_mrd.
6. Issue MRS (mode register set) command to load MR6 with INIT7.mr6 value followed by NOP/deselect for duration of DRAMTMG3.t_mrd.
7. Issue MRS (mode register set) command to load MR5 with INIT6.mr5 value followed by NOP/deselect for duration of DRAMTMG3.t_mrd.
8. Issue MRS (mode register set) command to load MR4 with INIT7.mr4 value followed by

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NOP/deselect for duration of DRAMTMG3.t_mrd.
9. Issue MRS command to load MR2 with INIT4.emr2 followed by NOP/deselect for duration of DRAMTMG3.t_mrd.
10. Issue MRS command to load MR1 with INIT4.emr followed by NOP/deselect for duration of DRAMTMG3.t_mrd.
11. Issue MRS command to load MR0 with INIT3.mr followed by NOP/deselect for duration of DRAMTMG3.t_mod.
12. Issue ZQCL command to start ZQ calibration and wait for INIT5.dev_zqinit_x32.
13. Wait for INIT5.dev_zqinit_x32 counting to finish. Ensure wait from step 8 is larger than tDLLK.
14. The PCTL controller is now ready for normal operation.

LPDDR2/3 Initialization Sequence

The initialization steps for LPDDR2/3 SDRAMs are as follows:
1. Power-up.
2. CKE is held low for a duration specified by INIT0.pre_cke_x1024. The clock is checked to be stable for duration specified by INIT2.min_stable_clock_x1 (minimum of 5 clock cycles) prior to the first low to high transition of CKE.
3. Assert CKE for INIT0.post_cke_x1024 (specification requires at least 200 us).
4. A MRW (Reset) command is issued to MRW63 register. Values of MA<7:0> = 3FH and OP<7:0> =00H is used for this command. The MRW reset command brings the device to the device auto initialization (resetting) state in the power-on initialization sequence.
5. Issue NOP/deselect for duration specified by INIT2.idle_after_reset_x32 (specification requires 1 us minimum) and INIT5.max_auto_init_x1024 (specification requires maximum time of 10 us).
6. An MRW ZQ initialization calibration command is issued to the memory to register MR10 to initiate the ZQ calibration. Values of MA<7:0> = 0AH and OP<7:0> = FFH is used for this command.
7. Issue NOP/deselect for duration specified by INIT5.dev_zqinit_x32 (specification requires a minimum time of 1us).
8. Program MR2 register by setting MR2 register to INIT3.emr followed by a NOP/deselect for a duration specified by DRAMTMG3.t_mrw (typical value of 5 clock cycles).
9. Program MR1 register by setting MR1 register to INIT3.mr followed by a NOP/deselect for a duration specified by DRAMTMG3.t_mrw (typical value of 5 clock cycles).
10. Program MR3 register by setting MR3 register to INIT4.emr2 followed by a NOP/deselect for a duration specified by DRAMTMG3.t_mrw (typical value of 5 clock cycles).
11. Schedule multiple all bank refresh.
12. The PCTL controller is now ready for normal operation.

2.6.2 TX DLLs

All high speed IO signals' phase can be adjusted by TX DLLs. See the following table.

Table 2-3DDR PHY TX DLLs Delay Step

Offset	Bit	Control Signal Phase	Default	Description
0x4c	2~0	CMD	0x4	CMD DLL delay step
0x50	2~0	CK	0x0	CK DLL delay step
0x98	2~0	A_DM0, A_DQ7~A_DQ0	0x4	DM and DQ DLL Signal delay step
0xd8	2~0	A_DM1, A_DQ15~A_DQ8	0x4	
0x118	2~0	B_DM0, B_DQ7~B_DQ0	0x4	
0x158	2~0	B_DM1, B_DQ15~B_DQ8	0x4	
0x9c	2~0	A_DQS0, A_DQSB0	0x0	TX DQS DLL Signal delay step
0xdc	2~0	A_DQS1, A_DQSB1	0x0	
0x11c	2~0	B_DQS0, B_DQSB0	0x0	
0x15c	2~0	B_DQS1, B_DQSB1	0x0	

Step 0x0 values means no phase delay, and 0x4 increases delay phase to 90 deg, 0x7 values corresponds to maximum phase delay. All DLLs having 8 delay steps which can get

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90 deg phase delay by setting 0x4.

2.6.3 RX DLLs

The RX DLLs are used for sample RX DQS signals with proper phase delay and pulse edges. The DQS squelch (Rx Squelch) signal opens a window for passing RX DQS pulses, both RX DQS and DQS squelch signal phase can be adjusted by corresponding DLLs.

Table 2-4DDR PHY RX DQS Delay Step

Offset	Bit	Control Signal Phase	Default	Description
0x0a0	1~0	A_DQS0,A_DQSB0	0x1	Read DQS DLL delay phase
0x0e0	1~0	A_DQS1,A_DQSB1	0x1	
0x120	1~0	A_DQS0,A_DQSB0	0x1	
0x160	1~0	A_DQS1,A_DQSB1	0x1	
0x0b0	7~5	left channel A DQS gating	0x1	CS0 DQS gating delay, unit x1 clock cycle
0x0f0	7~5	right channel A DQS gating	0x1	
0x130	7~5	left channel B DQS gating	0x1	
0x170	7~5	reft channel B DQS gating	0x1	
0x0b4	7~5	left channel A DQS gating	0x1	CS1 DQS gating delay, unit x1 clock cycle
0x0f4	7~5	right channel A DQS gating	0x1	
0x134	7~5	left channel B DQS gating	0x1	
0x174	7~5	reft channel B DQS gating	0x1	
0x0b0	4~3	left channel A DQS gating	0x1	CS0 additive and accumulative DQS gating delay, unit 4x clock cycle
0x0f0	4~3	right channel A DQS gating	0x1	
0x130	4~3	left channel B DQS gating	0x1	
0x170	4~3	reft channel B DQS gating	0x1	
0x0b4	4~3	left channel A DQS gating	0x1	CS1 additive and accumulative DQS gating delay, unit 4x clock cycle
0x0f4	4~3	right channel A DQS gating	0x1	
0x134	4~3	left channel B DQS gating	0x1	
0x174	4~3	reft channel B DQS gating	0x1	
0x0b0	2~0	left channel A DQS gating	0x4	CS0 additive and accumulative DQS gating delay, unit per DLL step
0x0f0	2~0	right channel A DQS gating	0x4	
0x130	2~0	left channel B DQS gating	0x4	
0x170	2~0	reft channel B DQS gating	0x4	
0x0b4	2~0	left channel A DQS gating	0x4	CS1 additive and accumulative DQS gating delay, unit per DLL step
0x0f4	2~0	right channel A DQS gating	0x4	
0x134	2~0	left channel B DQS gating	0x4	
0x174	2~0	reft channel B DQS gating	0x4	

2.6.4 High Speed IO Drive Strength

The tuning rage of driver resistance is 19.6ohm to to +∞. By default, 0x14 is 37.6ohm for DDR3 DQ and CMD driver. When the control bit is set to be larger, the drive strength becomes stronger.

Table 2-5CK/CMD Driver output resistance

Offset	Bit	Default	Description
0x44	4~0	0x14	adjustable CMD pull-down resistance
0x48	7~3	0x14	adjustable CMD pull-up resistance
0x58	4~0	0x14	adjustable CK pull-down resistance
0x60	4~0	0x14	adjustable CK pull-up resistance
0x5c	6~4	0x04	Adjust CMD/CK falling edge slew rate
0x5c	2~0	0x04	Adjust CMD/CK rising edge slew rate

Table 2-6DM, DQ Signal Drive Strength Register

Offset	Bit	Default	Description

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0x80	4~0	0x14	pull-down driving resistance for A_DQ0~A_DQ7
0xbc	4~0	0x14	pull-up driving resistance for A_DQ0~A_DQ7
0xc0	4~0	0x14	pull-down driving resistance for A_DQ8~A_DQ15
0xfc	4~0	0x14	pull-up driving resistance for A_DQ8~A_DQ15
0x100	4~0	0x14	pull-down driving resistance for B_DQ0~B_DQ7
0x13c	4~0	0x14	pull-up driving resistance for B_DQ0~B_DQ7
0x140	4~0	0x14	pull-down driving resistance for B_DQ8~B_DQ15
0x17c	4~0	0x14	pull-up driving resistance for B_DQ8~B_DQ15
0x0ac	7~5	0x4	Falling edge slew rate control for A_DQ0~A_DQ7
	4~2	0x4	Rising edge slew rate control for A_DQ0~A_DQ7
0x0ec	7~5	0x4	Falling edge slew rate control for A_DQ8~A_DQ15
	4~2	0x4	Rising edge slew rate control for A_DQ8~A_DQ15
0x12c	7~5	0x4	Falling edge slew rate control for B_DQ0~B_DQ7
	4~2	0x4	Rising edge slew rate control for B_DQ0~B_DQ7
0x16c	7~5	0x4	Falling edge slew rate control for B_DQ8~B_DQ15
	4~2	0x4	Rising edge slew rate control for B_DQ8~B_DQ15
0x084	4~0	0x4	pull-down ODT resistance for A_DQ0~A_DQ7
0x0b8	4~0	0x4	pull-up ODT resistance for A_DQ0~A_DQ7
0x0c4	4~0	0x4	pull-down ODT resistance for A_DQ8~A_DQ15
0x0f8	4~0	0x4	pull-up ODT resistance for A_DQ8~A_DQ15
0x104	4~0	0x4	pull-down ODT resistance for B_DQ0~B_DQ7
0x138	4~0	0x4	pull-up ODT resistance for B_DQ0~B_DQ7
0x144	4~0	0x4	pull-down ODT resistance for B_DQ8~B_DQ15
0x178	4~0	0x4	pull-up ODT resistance for B_DQ8~B_DQ15

The value is larger, the drive strength is stronger.

DDR3 1.5V DQ/DQS/CMD driver and ODT strength table

Table 2-7DDR3 1.5V DQ/DQS/CMD Driver and ODT resistance

Control bit	**5'b00000**	**5'b00001**	**5'b00010**	**5'b00011**
Pull-up/down	+∞	451.6ohm	225.8ohm	150.5ohm
Control bit	**5'b00100**	**5'b00101**	**5'b00110**	**5'b00111**
Pull-up/down	112.9ohm	90.3ohm	75.3ohm	64.5ohm
Control bit	**5'b01000**	**5'b01001**	**5'b01010**	**5'b01011**
Pull-up/down	56.5ohm	50.2ohm	45.2ohm	41.1ohm
Control bit	**5'b01100**	**5'b01101**	**5'b01110**	**5'b01111**
Pull-up/down	37.6ohm	34.7ohm	33.3ohm	30.1ohm
Control bit	**5'b10000**	**5'b10001**	**5'b10010**	**5'b10011**
Pull-up/down	56.5ohm	50.2ohm	45.2ohm	41.1ohm
Control bit	**5'b10100**	**5'b10101**	**5'b10110**	**5'b10111**
Pull-up/down	37.6ohm	34.7ohm	33.3ohm	30.1ohm
Control bit	**5'b11000**	**5'b11001**	**5'b11010**	**5'b11011**
Pull-up/down	28.2ohm	26.6ohm	25.1ohm	23.8ohm
Control bit	**5'b11100**	**5'b11101**	**5'b11110**	**5'b11111**
Pull-up/down	22.6ohm	21.5ohm	20.5ohm	19.6ohm

Table 2-8DDR4/LPDDR2/3 1.2V DQ/DQS/CMD driver and ODT resistance

Control bit	**5'b00000**	**5'b00001**	**5'b00010**	**5'b00011**
Pull-up/down	+∞	480.4ohm	240.2ohm	160.1ohm
Control bit	**5'b00100**	**5'b00101**	**5'b00110**	**5'b00111**
Pull-up/down	120.1ohm	96.1ohm	80.1ohm	68.6ohm
Control bit	**5'b01000**	**5'b01001**	**5'b01010**	**5'b01011**
Pull-up/down	60.0ohm	53.4ohm	48.0ohm	43.7ohm
Control bit	**5'b01100**	**5'b01101**	**5'b01110**	**5'b01111**

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Pull-up/down	40.0ohm	37.0ohm	34.3ohm	32.0ohm
Control bit	**5'b10000**	**5'b10001**	**5'b10010**	**5'b10011**
Pull-up/down	60.0ohm	53.4ohm	48.0ohm	43.7ohm
Control bit	**5'b10100**	**5'b10101**	**5'b10110**	**5'b10111**
Pull-up/down	40.0ohm	37.0ohm	34.3ohm	32.0ohm
Control bit	**5'b11000**	**5'b11001**	**5'b11010**	**5'b11011**
Pull-up/down	30.0ohm	28.3ohm	26.7ohm	25.3ohm
Control bit	**5'b11100**	**5'b11101**	**5'b11110**	**5'b11111**
Pull-up/down	24.0ohm	22.9ohm	21.8ohm	20.9ohm

2.6.5 PHY Low Speed Mode (200MHz)

DDR PHY supports low speed to high speed DDR3 by using two operating mode: normal delay line mode up to 800Mbps or more, low power mode where we support any speed up to 533Mbps. If all TX DLLs are bypassed, the PHY will enter low power state.
The DDR PHY entries low power mode when setting DLLs into Bypass mode. The following table illustrates related register settings.

Table 2-9Low Power DLL Setting

Offset	Bit	Default	Low power Setting	Description
0x290	4	0x0	0x1	right channel B TX DQ DLL in bypass mode
	3	0x0	0x1	left channel B TX DQ DLL in bypass mode
	2	0x0	0x1	right channel A TX DQ DLL in bypass mode
	1	0x0	0x1	left channel A TX DQ DLL in bypass mode
	0	0x0	0x1	CMD/CK DLL in bypass mode
0x4c	4	0x0	0x1	CMD DLL phase select
0x50	3	0x0	0x0	CK DLL phase select
0x98	4	0x0	0x1	A_DQ0~A_DQ7 TX DLL phase select
0x9c	3	0x0	0x0	A_DQS0/A_DQSB0 TX DLL phase select
0xd8	4	0x0	0x1	A_DQ8~A_DQ15 TX DLL phase select
0xdc	3	0x0	0x0	A_DQS1/A_DQSB1 TX DLL phase select
0x118	4	0x1	0x1	B_DQ0~B_DQ7 TX DLL phase select
0x11c	3	0x0	0x0	B_DQS0/B_DQSB0 TX DLL phase select
0x158	4	0x1	0x1	B_DQ8~B_DQ15 TX DLL phase select
0x15c	3	0x0	0x0	B_DQS1/B_DQSB1 TX DLL phase select

2.6.6 Per bit de-skew tuning

Per-bit de-skew is designed for compensating PCB trace mismatch, DDR PHY support skew individually adjustable for all PHY signals. There are eight steps for each bit de-skew adjusting, and the adjust resolution under different corners is shown below:

Table 2-10per-bit de-skew tuning resolution

	ff	tt	ss
de-skew resolution	15ps	20ps	32ps

Pre-bit de-skew is realized with inverter chain delay, per-bit de-skew control signals select how much inverters are connected to data path, the minimum resolution is determined by the two inverters minimum delay.
TX path deskew and RX path deskew employ same delay line, and they have same deskew tuning resolution. Minimum RX deskew tuning resolution can be about 28ps with SMIC55ll tt corner process, and we can re-design tuning resolution according to system and customer requirement.

2.6.7 DDR PHY Calibration

DDR PHY auto dqs calibration function has been implemented in the PHY. The entire training

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processes only need to configure the register to start andwait for finish.
The entire training process is as follows:
1. PHY’s register is reset, the setup is complete.
2. Send the initial command to dram and complete dram initialization.
3. Set the PHY's register beginning calibration.

Offset	Bit	Default	Description
0x8	5~4	0x0	DQS gating calibration CS select signal 2’b00: select CS0 and CS1 2’b01: select CS1 2’b10: select CS0
	1	0x0	set calibration bypass mode(1:bypass mode; 0:nomal)
	0	0x0	set calibration start (1: start; 0: stop)

4. Wait for the calibration finish by PHYREGFF.
5. Normal read and writes operation can begin.

2.6.8 DDR PHY Write Leveling Training

DDR PHY auto write leveling training function has been implemented in the PHY. The entire training processes only need to configure the register to start and wait for finish。
The entire training process is as follows:
1. PHY’s register is reset, the setup is complete.
2. Send the initial command to dram and complete dram initialization.
3. Set the PHYREG05 and PHYREG06 to configure the dram mode register which used to enable dram write leveling training function.
4. Set the PHY's register to begin training.

Offset	Bit	Default	Description
0x8	7~6	0x0	Write leveling CS select signal 2’b00: select CS0 and CS1 2’b01: select CS1 2’b10: select CS0
	3	0x0	Write leveling calibration bypass mode, active high
	2	0x0	Write leveling calibration control, active high

5. Wait for the calibration finish by PHYREGF0.
6. Normal read and writes operation can begin.

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Chapter 3 Mobile Storage Host Controller

3.1 Overview

The Mobile Storage Host Controller is designed to support Secure Digital memory (SD-max version 3.01) with 1 bits or 4 bits data width, Multimedia Card(MMC-max version 4.51) with 1 bits or 4 bits or 8 bits data width.
The Host Controller is instantiated for SDMMC, SDIO and EMMC. The interface difference between these instances is shown in "Interface Description".
The Host Controller supports following features:

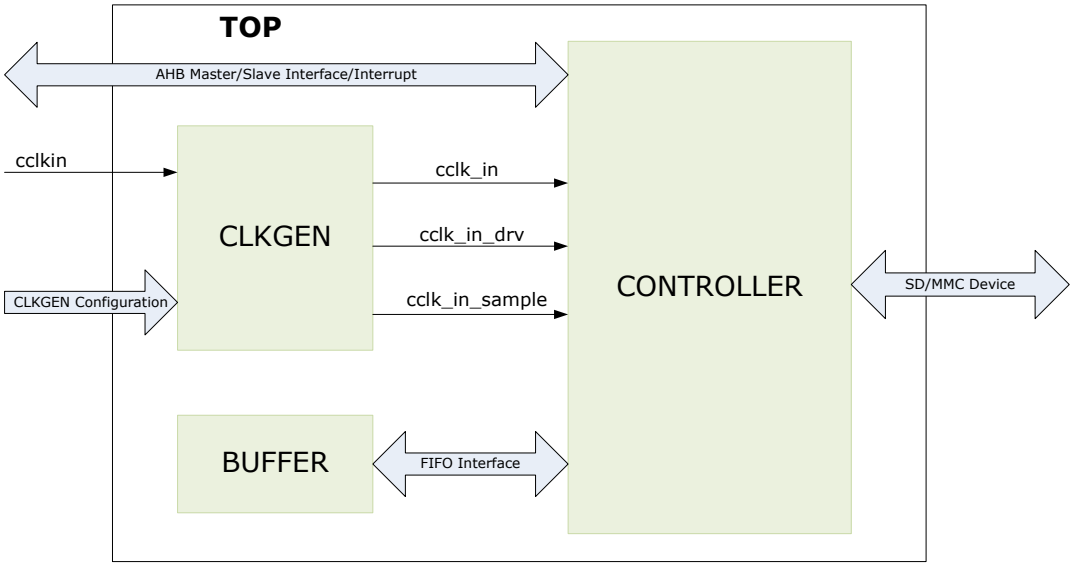
- Bus Interface Features:
  - Support AMBA AHB interface for master and slave
  - Supports internal DMA interface(IDMAC)
    - Supports 16/32-bit data transfers
    - Single-channel; single engine used for Transmit and Receive, which are mutually exclusive
    - Dual-buffer and chained descriptor linked list
    - Each descriptor can transfer up to 4KB of data in chained mode and 8KB of data in dual-buffer mode
    - Programmable burst size for optimal host bus utilization
  - Support combined single FIFO for both transmit and receive operations
  - Support FIFO size of 256x32
  - Support FIFO over-run and under-run prevention by stopping card clock
- Card Interface Features:
  - Support Secure Digital memory protocol commands
  - Support Secure Digital I/O protocol commands
  - Support Multimedia Card protocol commands
  - Support Command Completion Signal and interrupts to host
  - Support CRC generation and error detection
  - Support programmable baud rate
  - Support power management and power switch
  - Support card detection
  - Support write protection
  - Support hardware reset
  - Support SDIO interrupts in 1-bit and 4-bit modes
  - Support 4-bit mode in SDIO3.0
  - Support SDIO suspend and resume operation
  - Support SDIO read wait
  - Support block size of 1 to 65,535 bytes
  - Support 1-bit, 4-bit and 8-bit SDR modes
  - Support boot in 1-bit, 4-bit and 8-bit SDR modes
  - Support Packed Commands, CMD21, CMD49
- Clock Interface Features:
  - Support 0/90/180/270-degree phase shift operation for sample clock (cclk_in_sample) and drive clock(cclk_in_drv) relative to function clock(cclk_in) respectively

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- Support phase tuning using delay line for sample clock(cclk_in_sample) and drive clock(cclk_in_drv) relative to function clock (cclk_in) respectively. The max number of delay element number is 256

3.2 Block Diagram

The Host Controller consists of the following main functional blocks.



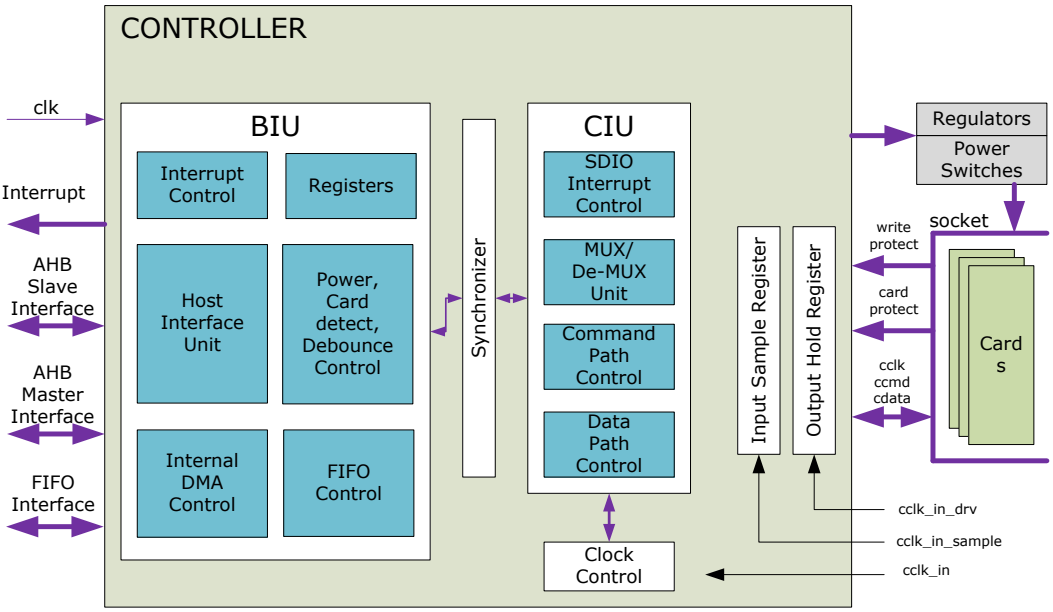


Fig. 3-1 Host Controller Block Diagram

- Clock Generate Unit(CLKGEN): generates card interface clock cclk_in/ cclk_sample/cclk_drv based on cclkin and configuration information.
- Asynchronous dual-port memory(BUFFER): Uses a two-clock synchronous read and synchronous write dual-port RAM. One of the ports is connected to the host clock, and the second port is connected to the card clock.
- Bus Interface Unit (BIU): Provides AMBA AHB interfaces for register and data read/writes.
- Card Interface Unit (CIU): Takes care of the SD/MMC protocols and provides clock management.

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3.3 Function Description

3.3.1 Bus Interface Unit

The Bus Interface Unit provides the following functions:

- Host interface
- Interrupt control
- Register access
- External FIFO access
- Power control and card detection

1. Host Interface Unit

The Host Interface Unit is an AHB slave interface, which provides the interface between the SD/MMC card and the host bus.

2. Register Unit

The register unit is part of the bus interface unit; it provides read and write access to the registers.

All registers reside in the Bus Interface Unit clock domain. When a command is sent to a card by setting the start_bit, which is bit[31] of the SDMMC_CMD register, all relevant registers needed for the CIU operation are transferred to the CIU block. During this time, the registers that are transferred from the BIU to the CIU should not be written. The software should wait for the hardware to clear the start bit before writing to these registers again. The register unit has a hardware locking feature to prevent illegal writes to registers. The lock is necessary in order to avoid metastability violations, both because the host and card clock domains are different and to prevent illegal software operations.

Once a command start is issued by setting the start_bit of the SDMMC_CMD register, the following registers cannot be reprogrammed until the command is accepted by the card interface unit:

- SDMMC_CMD – Command
- SDMMC_CMDARG – Command Argument
- SDMMC_BYTCNT – Byte Count
- SDMMC_BLKSIZ – Block Size
- SDMMC_CLKDIV – Clock Divider
- SDMMC_CLKENA – Clock Enable
- SDMMC_CLKSRC – Clock Source
- SDMMC_TMOUT – Timeout
- SDMMC_CTYPE – Card Type

The hardware resets the start_bit once the CIU accepts the command. If a host write to any of these registers is attempted during this locked time, then the write is ignored and the hardware lock error bit is set in the raw interrupt status register. Additionally, if the interrupt is enabled and not masked for a hardware lock error, then an interrupt is sent to the host.

When the Card Interface Unit is in an idle state, it typically takes the following number of clocks for the command handshake, where clk is the BIU clock and cclk_in is the CIU clock:

3 (clk) + 3 (cclk_in)

Once a command is accepted, you can send another command to the CIU-which has a one-deep command queue-under the following conditions:

- If the previous command was not a data transfer command, the new command is sent to the SD/MMC card once the previous command completes.
- If the previous command is a data transfer command and if wait_prvdata_complete (bit[13]) of the Command register is set for the new command, the new command is sent to the SD/MMC card only when the data transfer completes.
- If the wait_prvdata_complete is 0, then the new command is sent to the SD/MMC card as soon as the previous command is sent. Typically, you should use this only to stop or abort a previous data transfer or query the card status in the middle of a data transfer.

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3. Interrupt Controller Unit

The interrupt controller unit generates an interrupt that depends on the controller raw interrupt status, the interrupt-mask register, and the global interrupt-enable register bit. Once an interrupt condition is detected, it sets the corresponding interrupt bit in the raw interrupt status register. The raw interrupt status bit stays on until the software clears the bit by writing a 1 to the interrupt bit; a 0 leaves the bit untouched.

The interrupt port, int, is an active-high, level-sensitive interrupt. The interrupt port is active only when any bit in the raw interrupt status register is active, the corresponding interrupt mask bit is 1, and the global interrupt enable bit is 1. The interrupt port is registered in order to avoid any combinational glitches.

The int_enable is reset to 0 on power-on, and the interrupt mask bits are set to 32'h0, which masks all the interrupts.

Notes:

Before enabling the interrupt, it is always recommended that you write 32'hffff_ffff to the raw interrupt status register in order to clear any pending unserviced interrupts. When clearing interrupts during normal operation, ensure that you clear only the interrupt bits that you serviced.

The SDIO Interrupts, Receive FIFO Data Request (RXDR), and Transmit FIFO Data Request (TXDR) are set by level-sensitive interrupt sources. Therefore, the interrupt source should be first cleared before you can clear the interrupt bit of the Raw Interrupt register. For example, on seeing the Receive FIFO Data Request (RXDR) interrupt, the FIFO should be emptied so that the "FIFO count greater than the RX-Watermark" condition, which triggers the interrupt, becomes inactive. The rest of the interrupts are triggered by a single clock-pulse-width source.

Table 3-1 Bits in Interrupt Status Register

Bits	Interrupt	Description
24	sdio_interrupt	Interrupt from SDIO card. In MMC-Ver3.3-only mode, these bits are always 0
16	Card no-busy	If card exit busy status, the interrupt happened
15	End Bit Error (read) /Write no CRC (EBE)	Error in end-bit during read operation, or no data CRC received during write operation. For MMC CMD19, there may be no CRC status returned by the card. Hence, EBE is set for CMD19. The application should not treat this as an error.
14	Auto Command Done (ACD)	Stop/abort commands automatically sent by card unit and not initiated by host; similar to Command Done (CD) interrupt. Recommendation: Software typically need not enable this for non CE-ATA accesses; Data Transfer Over (DTO) interrupt that comes after this interrupt determines whether data transfer has correctly competed.
13	Start Bit Error (SBE)	Error in data start bit when data is read from a card. In 4-bit mode, if DAT[0] line indicates start bit-that is, 0-and any of the other data bits do not have start bit, then this error is set. Busy Complete Interrupt when data is written to the card. This interrupt is generated after completion of busy driven by the card after the last data block is written into the card.
12	Hardware Locked write Error (HLE)	During hardware-lock period, write attempted to one of locked registers. When software sets the start_cmd bit in the SDMMC_CMD register, the Host Controller tries to load the command. If the command buffer is already filled with a command, this error is raised. The software then has to reload the command.
11	FIFO Underrun/ Overrun Error (FRUN)	Host tried to push data when FIFO was full, or host tried to read data when FIFO was empty. Typically this should not happen, except due to error in software.

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Bits	Interrupt	Description
		Card unit never pushes data into FIFO when FIFO is full, and pop data when FIFO is empty. If IDMAC is enabled, FIFO underrun/overrun can occur due to a programming error on MSIZE and watermark values in SDMMC_FIFOTH register.
10	Data Starvation by Host Timeout (HTO)	To avoid data loss, card clock out is stopped if FIFO is empty when writing to card, or FIFO is full when reading from card. Whenever card clock is stopped to avoid data loss, data-starvation timeout counter is started with data-timeout value. This interrupt is set if host does not fill data into FIFO during write to card, or does not read from FIFO during read from card before timeout period. Even after timeout, card clock stays in stopped state, with CIU state machines waiting. It is responsibility of host to push or pop data into FIFO upon interrupt, which automatically restarts cclk_out and card state machines. Even if host wants to send stop/abort command, it still needs to ensure it has to push or pop FIFO so that clock starts in order for stop/abort command to send on cmd signal along with data that is sent or received on data line.
9	Data Read Timeout (DRTO)	In Normal functioning mode: Data read timeout (DRTO) Data timeout occurred. Data Transfer Over (DTO) also set if data timeout occurs. In Boot Mode: Boot Data Start (BDS) When set, indicates that Host Controller has started to receive boot data from the card. A write to this register with a value of 1 clears this interrupt.
8	Response Timeout (RTO)	In normal functioning mode: Response timeout (RTO) Response timeout occurred. Command Done (CD) also set if response timeout occurs. If command involves data transfer and when response times out, no data transfer is attempted by Host Controller. In Boot Mode: Boot Ack Received (BAR) When expect_boot_ack is set, on reception of a boot acknowledge pattern—0-1-0—this interrupt is asserted. A write to this register with a value of 1 clears this interrupt.
7	Data CRC Error (DCRC)	Received Data CRC does not match with locally-generated CRC in CIU. Can also occur if the Write CRC status is incorrectly sampled by the Host.
6	Response CRC Error (RCRC)	Response CRC does not match with locally-generated CRC in CIU.
5	Receive FIFO Data Request (RXDR)	Interrupt set during read operation from card when FIFO level is greater than Receive-Threshold level. Recommendation: In DMA modes, this interrupt should not be enabled. In non-DMA mode: pop RX_WMark + 1 data from FIFO.
4	Transmit FIFO Data Request (TXDR)	Interrupt set during write operation to card when FIFO level reaches less than or equal to Transmit-Threshold level.

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Bits	Interrupt	Description

		Recommendation:
		In DMA modes, this interrupt should not be enabled.
		In non-DMA mode:
		if (pending_bytes > (FIFO_DEPTH - TX_WMark))
		push (FIFO_DEPTH - TX_WMark) data into FIFO
		else
		push pending_bytes data into FIFO

3	Data Transfer Over (DTO)	Indicates Data transfer completed. Though on detection of errors-Start Bit Error, Data CRC error, and so on, DTO may or may not be set; the application must issue CMD12, which ensures that DTO is set. Recommendation: In non-DMA mode, when data is read from card, on seeing interrupt, host should read any pending data from FIFO. In DMA mode, DMA controllers guarantee FIFO is flushed before interrupt. DTO bit is set at the end of the last data block, even if the device asserts MMC busy after the last data block.
2	Command Done(CD)	Command sent to card and got response from card, even if Response Error or CRC error occurs.
1	Response Error (RE)	Error in received response set if one of following occurs: ● Transmission bit != 0 ● Command index mismatch ● End-bit != 1
0	Card-Detect (CDT)	When one or more cards inserted or removed, this interrupt occurs. Software should read card-detect register to determine current card status. Recommendation: After power-on and before enabling interrupts, software should read card detect register and store it in memory. When interrupt occurs, it should read card detect register and compare it with value stored in memory to determine which card(s) were removed/inserted. Before exiting ISR, software should update memory with new card-detect value.

4. FIFO Controller Unit

The FIFO controller interfaces the external FIFO to the host interface and the card controller unit. When FIFO overrun and under-run conditions occur, the card clock stops in order to avoid data loss.

The FIFO uses a two-clock synchronous read and synchronous write dual-port RAM. One of the ports is connected to the host clock, clk, and the second port is connected to the card clock, cclk_in.

Notes: The FIFO controller does not support simultaneous read/write access from the same port. For debugging purposes, the software may try to write into the FIFO and read back the data; results are indeterminate, since the design does not support read/write access from the same port.

5. Power Control and Card Detection Unit

The register unit has registers that control the power. Power to each card can be selectively turned on or off.

The card detection unit looks for any changes in the card-detect signals for card insertion or card removal. It filters out the debounces associated with mechanical insertion or removal, and generates one interrupt to the host. You can program the debounce filter value.

On power-on, the controller should read in the card_detect port and store the value in the memory. Upon receiving a card-detect interrupt, it should again read the card_detect port and XOR with the previous card-detect status to find out which card has interrupted. If more than one card is simultaneously removed or inserted, there is only one card-detect

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interrupt; the XOR value indicates which cards have been disturbed. The memory should be updated with the new card-detect value.

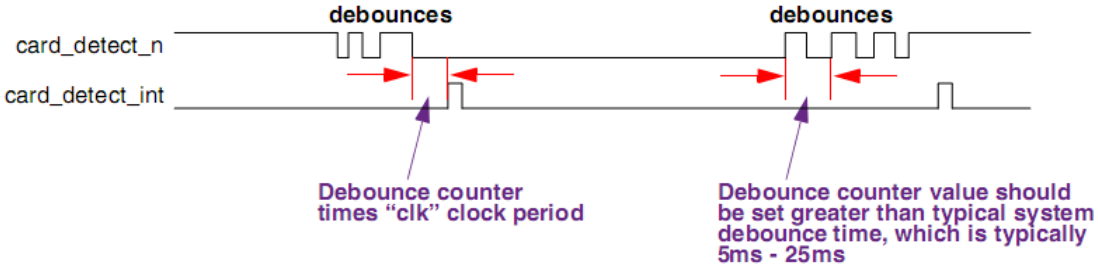


Fig. 3-2 SD/MMC Card-Detect Signal

6. DMA Interface Unit

DMA signals interface the Host Controller to an external DMA controller to reduce the software overhead during FIFO data transfers. The DMA request/acknowledge handshake is used for only data transfers. The DMA interface provides a connection to the DMA Controller. On seeing the DMA request, the DMA controller initiates accesses through the host interface to read or write into the data FIFO. The Host Controller has FIFO transmit/receive watermark registers that you can set, depending on system latency. The DMA interface asserts the request in the following cases:

- Read from a card when the data FIFO word count exceeds the Rx-Watermark level
- Write to a card when the FIFO word count is less than or equal to the Tx-Watermark level

When the DMA interface is enabled, you can use normal host read/write to access the data FIFO.

3.3.2 Card Interface Unit

The Card Interface Unit (CIU) interfaces with the Bus Interface Unit (BIU) and the devices. The host writes command parameters to the BIU control registers, and these parameters are then passed to the CIU. Depending on control register values, the CIU generates SD/MMC command and data traffic on a selected card bus according to SD/MMC protocol. The Host Controller accordingly controls the command and data path.

The following software restrictions should be met for proper CIU operation:

- Only one data transfer command can be issued at a time.
- During an open-ended card write operation, if the card clock is stopped because the FIFO is empty, the software must first fill the data into the FIFO and start the card clock. It can then issue only a stop/abort command to the card.
- When issuing card reset commands (CMD0, CMD15 or CMD52_reset) while a card data transfer is in progress, the software must set the stop_abort_cmd bit in the Command register so that the Host Controller can stop the data transfer after issuing the card reset command.
- When the data end bit error is set in the SDMMC_RINTSTS register, the Host Controller does not guarantee SDIO interrupts. The software should ignore the SDIO interrupts and issue the stop/abort command to the card, so that the card stops sending the read data.
- If the card clock is stopped because the FIFO is full during a card read, the software should read at least two FIFO locations to start the card clock.

The CIU block consists of the following primary functional blocks:

- Command path
- Data path
- SDIO interrupt control
- Clock control
- Mux/demux unit

1. Command Path

The command path performs the following functions:

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- Loads clock parameters
- Loads card command parameters
- Sends commands to card bus (ccmd_out line)
- Receives responses from card bus (ccmd_in line)
- Sends responses to BIU
- Drives the P-bit on command line

A new command is issued to the Host Controller by programming the BIU registers and setting the start_cmd bit in the Command register. The BIU asserts start_cmd, which indicates that a new command is issued to the SD/MMC device. The command path loads this new command (command, command argument, timeout) and sends acknowledge to the BIU by asserting cmd_taken.
Once the new command is loaded, the command path state machine sends a command to the device bus-including the internally generated CRC7-and receives a response, if any. The state machine then sends the received response and signals to the BIU that the command is done, and then waits for eight clocks before loading a new command.

Load Command Parameters

One of the following commands or responses is loaded in the command path:

- New command from BIU – When start_cmd is asserted, then the start_cmd bit is set in the Command register.
- Internally-generated auto-stop command – When the data path ends, the stop command request is loaded.
- IRQ response with RCA 0x000 – When the command path is waiting for an IRQ response from the MMC card and a "send irq response" request is signaled by the BIU, then the send_irq_response bit is set in the control register.

Loading a new command from the BIU in the command path depends on the following Command register bit settings:

- update_clock_registers_only – If this bit is set in the Command register, the command path updates only the clock enable, clock divider, and clock source registers. If this bit is not set, the command path loads the command, command argument, and timeout registers; it then starts processing the new command.
- wait_prvdata_complete – If this bit is set, the command path loads the new command under one of the following conditions:
  - Immediately, if the data path is free (that is, there is no data transfer in progress), or if an open-ended data transfer is in progress (byte_count = 0).
  - After completion of the current data transfer, if a predefined data transfer is in progress.

Send Command and Receive Response

Once a new command is loaded in the command path, update_clock_registers_only bit is unset – the command path state machine sends out a command on the device bus; the command path state machine is illustrated in following figure.

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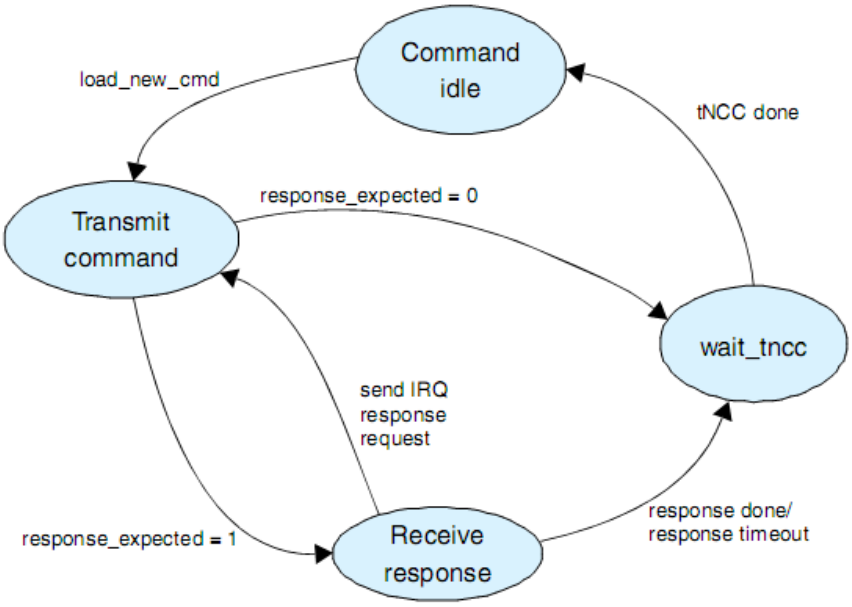


Fig. 3-3 Host Controller Command Path State Machine

The command path state machine performs the following functions, according to Command register bit values:

- send_initialization – Initialization sequence of 80 clocks is sent before sending the command.
- response_expected – Response is expected for the command. After the command is sent out, the command path state machine receives a 48-bit or 136-bit response and sends it to the BIU. If the start bit of the card response is not received within the number of clocks programmed in the timeout register, then the response timeout and command done bit is set in the Raw Interrupt Status register as a signal to the BIU. If the response-expected bit is not set, the command path sends out a command and signals a response done to the BIU; that is, the command done bit is set in the Raw Interrupt Status register.
- response_length – If this bit is set, a 136-bit response is received; if it is not set, a 48-bit response is received.
- check_response_crc – If this bit is set, the command path compares CRC7 received in the response with the internally-generated CRC7. If the two do not match, the response CRC error is signaled to the BIU; that is, the response CRC error bit is set in the Raw Interrupt Status register.

Send Response to BIU

If the response_expected bit is set in the Command register, the received response is sent to the BIU. The Response0 register is updated for a short response, and the Response3, Response2, Response1, and Response0 registers are updated on a long response, after which the Command Done bit is set. If the response is for an auto_stop command sent by the CIU, the response is saved in the Response1 register, after which the Auto Command Done bit is set.

Additionally, the command path checks for the following:

- Transmission bit = 0
- Command index matches command index of the sent command
- End bit = 1 in received card response

The command index is not checked for a 136-bit response or if the check_response_crc bit is unset. For a 136-bit response and reserved CRC 48-bit responses, the command index is reserved-that is, 111111.

Polling Command Completion Signal

The device generates the Command Completion Signal in order to notify the host controller

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of the normal command completion or command termination.

Command Completion Signal Detection and Interrupt to Host Processor

If the ccs_expected bit is set in the Command register, the Command Completion Signal (CCS) from the device is indicated by setting the Data Transfer Over (DTO) bit in the SDMMC_RINTSTS register. The Host Controller generates a Data Transfer Over (DTO) interrupt if this interrupt is not masked.

Command Completion Signal Timeout

If the command expects a CCS from the device—if the ccs_expected bit is set in the Command register—the command state machine waits for the CCS and remains in a wait_CCSS state. If the device fails to send out the CCS, the host software should implement a timeout mechanism to free the command and data path. The host controller does not implement a hardware timer; it is the responsibility of the host software to maintain a software timer.

In the event of a CCS timeout, the host should issue a CCSD by setting the send_ccsd bit in the CTRL register. The host controller command state machine sends the CCSD to the device and exits to an idle state. After sending the CCSD, the host should also send a CMD12 to the device in order to abort the outstanding command.

Send Command Completion Signal Disable

If the send_ccsd bit is set in the CTRL register, the host sends a Command Completion Signal Disable (CCSD) pattern on the CMD line. The host can send the CCSD while waiting for the CCS or after a CCS timeout happens.

After sending the CCSD pattern, the host sets the Command Done (CD) bit in SDMMC_RINTSTS and also generates an interrupt to the host if the Command Done interrupt is not masked.

2. Data Path

The data path block pops the data FIFO and transmits data on cdata_out during a write data transfer, or it receives data on cdata_in and pushes it into the FIFO during a read data transfer. The data path loads new data parameters—that is, data expected, read/write data transfer, stream/block transfer, block size, byte count, card type, timeout registers—whenever a data transfer command is not in progress.

If the data_expected bit is set in the Command register, the new command is a data transfer command and the data path starts one of the following:

- Transmit data if the read/write bit = 1
- Data receive if read/write bit = 0

Data Transmit

The data transmit state machine, illustrated in following figure, starts data transmission two clocks after a response for the data write command is received; this occurs even if the command path detects a response error or response CRC error. If a response is not received from the card because of a response timeout, data is not transmitted. Depending upon the value of the transfer_mode bit in the Command register, the data transmit state machine puts data on the card data bus in a stream or in block(s).

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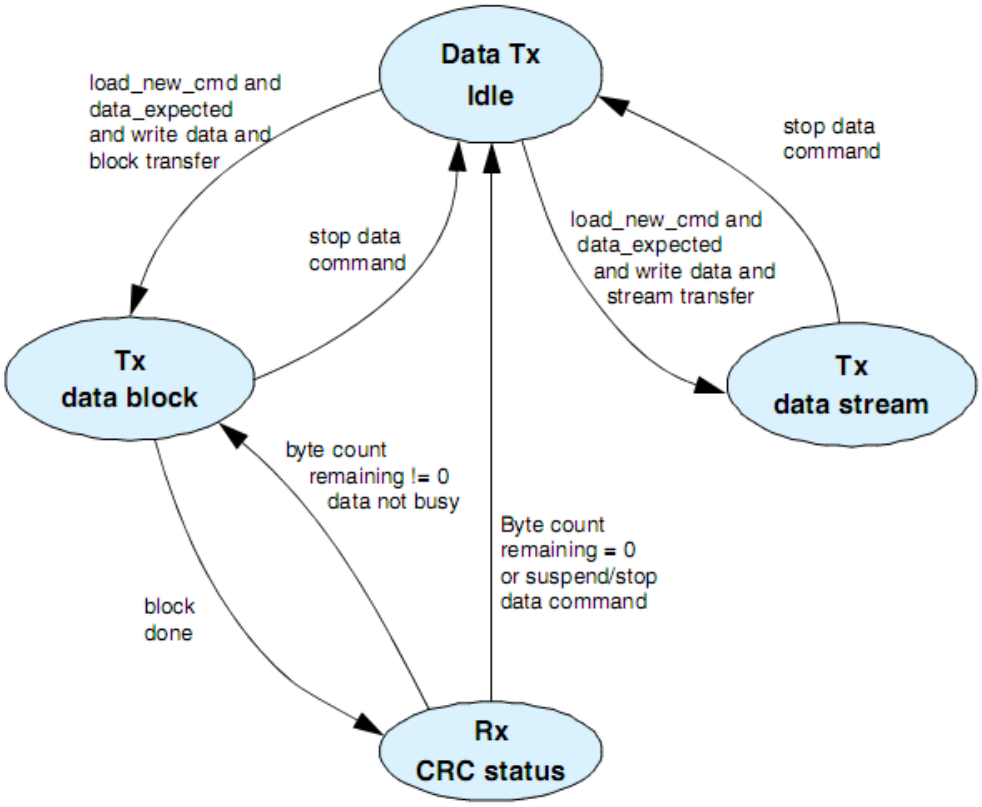


Fig. 3-4 Host Controller Data Transmit State Machine

Stream Data Transmit

If the transfer_mode bit in the Command register is set to 1, it is a stream-write data transfer. The data path pops the FIFO from the BIU and transmits in a stream to the card data bus. If the FIFO becomes empty, the card clock is stopped and restarted once data is available in the FIFO.

If the byte_count register is programmed to 0, it is an open-ended stream-write data transfer. During this data transfer, the data path continuously transmits data in a stream until the host software issues a stop command. A stream data transfer is terminated when the end bit of the stop command and end bit of the data match over two clocks.

If the byte_count register is programmed with a non-zero value and the send_auto_stop bit is set in the Command register, the stop command is internally generated and loaded in the command path when the end bit of the stop command occurs after the last byte of the stream write transfer matches.

This data transfer can also terminate if the host issues a stop command before all the data bytes are transferred to the card bus.

Single Block Data

If the transfer_mode bit in the Command register is set to 0 and the byte_count register value is equal to the value of the block_size register, a single-block write-data transfer occurs. The data transmit state machine sends data in a single block, where the number of bytes equals the block size, including the internally-generated CRC16.

If the SDMMC_CTYPE register bit for the selected card – indicated by the card_num value in the Command register – is set for a 1-bit, 4-bit, or 8-bit data transfer, the data is transmitted on 1, 4, or 8 data lines, respectively, and CRC16 is separately generated and transmitted for 1, 4, or 8 data lines, respectively.

After a single data block is transmitted, the data transmit state machine receives the CRC status from the card and signals a data transfer to the BIU; this happens when the data-transfer-over bit is set in the SDMMC_RINTSTS register.

If a negative CRC status is received from the card, the data path signals a data CRC error to the BIU by setting the data CRC error bit in the SDMMC_RINTSTS register.

Additionally, if the start bit of the CRC status is not received by two clocks after the end of the data block, a CRC status start bit error is signaled to the BIU by setting the write-no-CRC bit in the SDMMC_RINTSTS register.

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Multiple Block Data

A multiple-block write-data transfer occurs if the transfer_mode bit in the Command register is set to 0 and the value in the byte_count register is not equal to the value of the block_size register. The data transmit state machine sends data in blocks, where the number of bytes in a block equals the block size, including the internally-generated CRC16.

If the SDMMC_CTYPE register bit for the selected card – indicated by the card_num value in the Command register – is set to 1-bit, 4-bit, or 8-bit data transfer, the data is transmitted on 1, 4, or 8 data lines, respectively, and CRC16 is separately generated and transmitted on 1, 4, or 8 data lines, respectively.

After one data block is transmitted, the data transmit state machine receives the CRC status from the card. If the remaining byte_count becomes 0, the data path signals to the BIU that the data transfer is done; this happens when the data-transfer-over bit is set in the SDMMC_RINTSTS register.

If the remaining data bytes are greater than 0, the data path state machine starts to transmit another data block.

If a negative CRC status is received from the card, the data path signals a data CRC error to the BIU by setting the data CRC error bit in the SDMMC_RINTSTS register, and continues further data transmission until all the bytes are transmitted.

Additionally, if the CRC status start bit is not received by two clocks after the end of a data block, a CRC status start bit error is signaled to the BIU by setting the write-no-CRC bit in the SDMMC_RINTSTS register; further data transfer is terminated.

If the send_auto_stop bit is set in the Command register, the stop command is internally generated during the transfer of the last data block, where no extra bytes are transferred to the card. The end bit of the stop command may not exactly match the end bit of the CRC status in the last data block.

If the block size is less than 4, 16, or 32 for card data widths of 1 bit, 4 bits, or 8 bits, respectively, the data transmit state machine terminates the data transfer when all the data is transferred, at which time the internally generated stop command is loaded in the command path.

If the byte_count is 0 – the block size must be greater than 0 – it is an open-ended block transfer. The data transmit state machine for this type of data transfer continues the block-write data transfer until the host software issues a stop or abort command.

Data Receive

The data-receive state machine, illustrated in following figure, receives data two clock cycles after the end bit of a data read command, even if the command path detects a response error or response CRC error. If a response is not received from the card because a response timeout occurs, the BIU does not receive a signal that the data transfer is complete; this happens if the command sent by the Host Controller is an illegal operation for the card, which keeps the card from starting a read data transfer.

If data is not received before the data timeout, the data path signals a data timeout to the BIU and an end to the data transfer done. Based on the value of the transfer_mode bit in the Command register, the data-receive state machine gets data from the card data bus in a stream or block(s).

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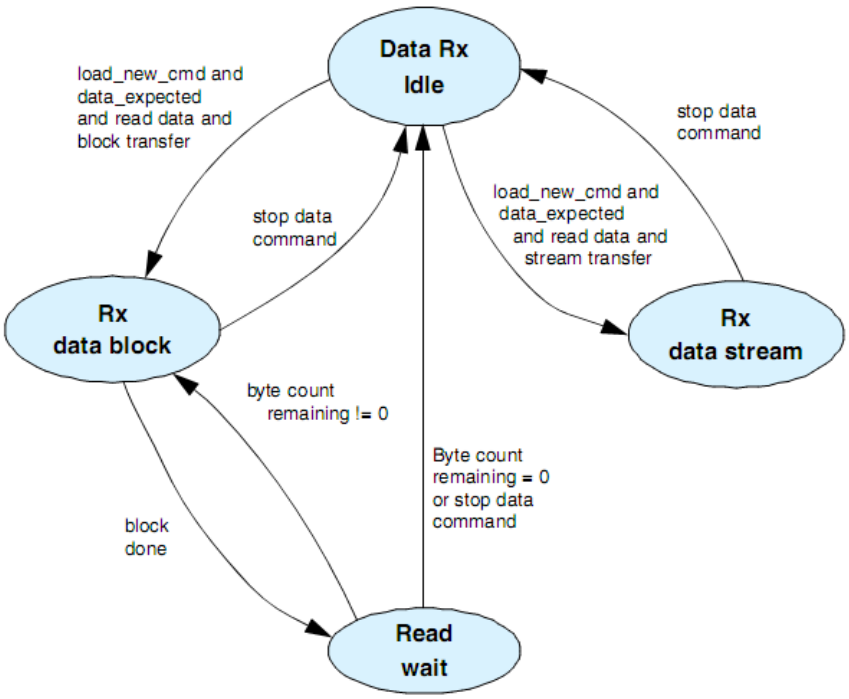


Fig. 3-5 Host Controller Data Receive State Machine

Stream Data Read

A stream-read data transfer occurs if the transfer_mode bit in the Command register equals 1, at which time the data path receives data from the card and pushes it to the FIFO. If the FIFO becomes full, the card clock stops and restarts once the FIFO is no longer full.

An open-ended stream-read data transfer occurs if the byte_count register equals 0. During this type of data transfer, the data path continuously receives data in a stream until the host software issues a stop command. A stream data transfer terminates two clock cycles after the end bit of the stop command.

If the byte_count register contains a non-zero value and the send_auto_stop bit is set in the Command register, a stop command is internally generated and loaded into the command path, where the end bit of the stop command occurs after the last byte of the stream data transfer is received. This data transfer can terminate if the host issues a stop or abort command before all the data bytes are received from the card.

Single-Block Data Read

A single-block read-data transfer occurs if the transfer_mode bit in the Command register is set to 0 and the value of the byte_count register is equal to the value of the block_size register. When a start bit is received before the data times out, data bytes equal to the block size and CRC16 are received and checked with the internally-generated CRC16.

If the SDMMC_CTYPE register bit for the selected card – indicated by the card_num value in the Command register – is set to a 1-bit, 4-bit, or 8-bit data transfer, data is received from 1, 4, or 8 data lines, respectively, and CRC16 is separately generated and checked for 1, 4, or 8 data lines, respectively. If there is a CRC16 mismatch, the data path signals a data CRC error to the BIU. If the received end bit is not 1, the BIU receives an end-bit error.

Multiple-Block Data Read

If the transfer_mode bit in the Command register is set to 0 and the value of the byte_count register is not equal to the value of the block_size register, it is a multiple-block read-data transfer. The data-receive state machine receives data in blocks, where the number of bytes in a block is equal to the block size, including the internally-generated CRC16.

If the SDMMC_CTYPE register bit for the selected card – indicated by the card_num value in the Command register – is set to a 1-bit, 4-bit, or 8-bit data transfer, data is received from 1, 4, or 8 data lines, respectively, and CRC16 is separately generated and checked for 1, 4, or 8 data lines, respectively.

After a data block is received, if the remaining byte_count becomes 0, the data path signals a data transfer to the BIU.

If the remaining data bytes are greater than 0, the data path state machine causes another

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data block to be received. If CRC16 of a received data block does not match the internally-generated CRC16, a data CRC error to the BIU and data reception continue further data transmission until all bytes are transmitted.
Additionally, if the end of a received data block is not 1, data on the data path signals terminate the bit error to the CIU and the data-receive state machine terminates data reception, waits for data timeout, and signals to the BIU that the data transfer is complete.
If the send_auto_stop bit is set in the Command register, the stop command is internally generated when the last data block is transferred, where no extra bytes are transferred from the card; the end bit of the stop command may not exactly match the end bit of the last data block.
If the requested block size for data transfers to cards is less than 4, 16, or 32 bytes for 1-bit, 4-bit, or 8-bit data transfer modes, respectively, the data-transmit state machine terminates the data transfer when all data is transferred, at which point the internally-generated stop command is loaded in the command path. Data received from the card after that are then ignored by the data path.
If the byte_count is 0—the block size must be greater than 0—it is an open-ended block transfer. For this type of data transfer, the data-receive state machine continues the block-read data transfer until the host software issues a stop or abort command.

Auto-Stop

The Host Controller internally generates a stop command and is loaded in the command path when the send_auto_stop bit is set in the Command register.
The software should set the send_auto_stop bit according to details listed in following table.

Table 3-2 Auto-Stop Generation

Card type	Transfer type	Byte Count	send_auto_stop bit set	Comments
MMC	Stream read	0	No	Open-ended stream
MMC	Stream read	>0	Yes	Auto-stop after all bytes transfer
MMC	Stream write	0	No	Open-ended stream
MMC	Stream write	>0	Yes	Auto-stop after all bytes transfer
MMC	Single-block read	>0	No	Byte count =0 is illegal
MMC	Single-block write	>0	No	Byte count =0 is illegal
MMC	Multiple-block read	0	No	Open-ended multiple block
MMC	Multiple-block read	>0	Yes①	Pre-defined multiple block
MMC	Multiple-block write	0	No	Open-ended multiple block
MMC	Multiple-block write	>0	Yes①	Pre-defined multiple block
SDMEM	Single-block read	>0	No	Byte count =0 is illegal
SDMEM	Single-block write	>0	No	Byte count =0 illegal
SDMEM	Multiple-block read	0	No	Open-ended multiple block
SDMEM	Multiple-block read	>0	Yes	Auto-stop after all bytes transfer
SDMEM	Multiple-block write	0	No	Open-ended multiple block
SDMEM	Multiple-block write	>0	Yes	Auto-stop after all bytes transfer
SDIO	Single-block read	>0	No	Byte count =0 is illegal
SDIO	Single-block write	>0	No	Byte count =0 illegal
SDIO	Multiple-block read	0	No	Open-ended multiple block
SDIO	Multiple-block read	>0	No	Pre-defined multiple block
SDIO	Multiple-block	0	No	Open-ended multiple block

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Card type	Transfer type	Byte Count	send_auto_stop bit set	Comments
	write			
SDIO	Multiple-block write	>0	No	Pre-defined multiple block

①:*The condition under which the transfer mode is set to block transfer and byte_count is equal to block size is treated as a single-block data transfer command for both MMC and SD cards. If byte_count = n*block_size (n = 2, 3, …), the condition is treated as a predefined multiple-block data transfer command. In the case of an MMC card, the host software can perform a predefined data transfer in two ways: 1) Issue the CMD23 command before issuing CMD18/CMD25 commands to the card – in this case, issue MD18/CMD25 commands without setting the send_auto_stop bit. 2) Issue CMD18/CMD25 commands without issuing CMD23 command to the card, with the send_auto_stop bit set. In this case, the multiple-block data transfer is terminated by an internally-generated auto-stop command after the programmed byte count.*

The following list conditions for the auto-stop command.

- Stream read for MMC card with byte count greater than 0 – The Host Controller generates an internal stop command and loads it into the command path so that the end bit of the stop command is sent out when the last byte of data is read from the card and no extra data byte is received. If the byte count is less than 6 (48 bits), a few extra data bytes are received from the card before the end bit of the stop command is sent.
- Stream write for MMC card with byte count greater than 0 - The Host Controller generates an internal stop command and loads it into the command path so that the end bit of the stop command is sent when the last byte of data is transmitted on the card bus and no extra data byte is transmitted. If the byte count is less than 6 (48 bits), the data path transmits the data last in order to meet the above condition.
- Multiple-block read memory for SD card with byte count greater than 0 – If the block size is less than 4 (single-bit data bus), 16 (4-bit data bus), or 32 (8-bit data bus), the auto-stop command is loaded in the command path after all the bytes are read. Otherwise, the top command is loaded in the command path so that the end bit of the stop command is sent after the last data block is received.
- Multiple-block write memory for SD card with byte count greater than 0 – If the block size is less than 3 (single-bit data bus), 12 (4-bit data bus), or 24 (8-bit data bus), the auto-stop command is loaded in the command path after all data blocks are transmitted. Otherwise, the stop command is loaded in the command path so that the end bit of the stop command is sent after the end bit of the CRC status is received.
- Precaution for host software during auto-stop – Whenever an auto-stop command is issued, the host software should not issue a new command to the SD/MMC device until the auto-stop is sent by the Host Controller and the data transfer is complete. If the host issues a new command during a data transfer with the auto-stop in progress, an auto-stop command may be sent after the new command is sent and its response is received; this can delay sending the stop command, which transfers extra data bytes. For a stream write, extra data bytes are erroneous data that can corrupt the card data. If the host wants to terminate the data transfer before the data transfer is complete, it can issue a stop or abort command, in which case the Host Controller does not generate an auto-stop command.

3. Non-Data Transfer Commands that Use Data Path

Some non-data transfer commands (non-read/write commands) also use the data path. Following table lists the commands and register programming requirements for them.

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Table 3-3 Non-data Transfer Commands and Requirements

Base Address [12:8]	CMD 27	CMD 30	CMD 42	ACMD 13	ACMD 22	ACMD 51
Command register programming						
cmd_index	6'h1B	6'h1E	6'h2A	6'h0D	6'h16	6'h33
response_expect	1	1	1	1	1	1
rResponse_length	0	0	0	0	0	0
check_response_crc	1	1	1	1	1	1
data_expected	1	1	1	1	1	1
read/write	1	0	1	0	0	0
transfer_mode	0	0	0	0	0	0
send_auto_stop	0	0	0	0	0	0
wait_prevdata_complete	0	0	0	0	0	0
stop_abort_cmd	0	0	0	0	0	0
Command Argument register programming						
	stuff bits	32-bit write protect data address	stuff bits	stuff bits	stuff bits	stuff bits
Block Size register programming						
	16	4	Num_bytes①	64	4	8
Byte Count register programming						
	16	4	Num_bytes①	64	4	8

①: *Num_bytes = No. of bytes specified as per the lock card data structure (Refer to the SD specification and the MMC specification)*

4. SDIO Interrupt Control

Interrupts for SD cards are reported to the BIU by asserting an interrupt signal for two clock cycles. SDIO cards signal an interrupt by asserting cdata_in low during the interrupt period; an interrupt period for the selected card is determined by the interrupt control state machine. An interrupt period is always valid for non-active or non-selected cards, and 1-bit data mode for the selected card. An interrupt period for a wide-bus active or selected card is valid for the following conditions:

- Card is idle
- Non-data transfer command in progress
- Third clock after end bit of data block between two data blocks
- From two clocks after end bit of last data until end bit of next data transfer command

Bear in mind that, in the following situations, the controller does not sample the SDIO interrupt of the selected card when the card data width is 4 bits. Since the SDIO interrupt is level-triggered, it is sampled in a further interrupt period and the host does not lose any SDIO interrupt from the card.

- Read/Write Resume – The CIU treats the resume command as a normal data transfer command. SDIO interrupts during the resume command are handled similarly to other data commands. According to the SDIO specification, for the normal data command the interrupt period ends after the command end bit of the data command; for the resume command, it ends after the response end bit. In the case of the resume command, the Controller stops the interrupt sampling period after the resume command end bit, instead of stopping after the response end bit of the resume command.
- Suspend during read transfer – If the read data transfer is suspended by the host, the host sets the abort_read_data bit in the controller to reset the data state machine. In the CIU, the SDIO interrupts are handled such that the interrupt sampling starts after the abort_read_data bit is set by the host. In this case the controller does not sample

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SDIO interrupts between the period from response of the suspend command to setting the abort_read_data bit, and starts sampling after setting the abort_read_data bit.

5. Clock Control

The clock control block provides different clock frequencies required for SD/MMC cards. The cclk_in signal is the source clock (cclk_in >= card max operating frequency) for clock divider of the clock control block. This source clock (cclk_in) is used to generate different card clock frequencies (cclk_out). The card clock can have different clock frequencies, since the card can be a low-speed card or a full-speed card. The Host Controller provides one clock signal (cclk_out).

The clock frequency of a card depends on the following clock control registers:

- Clock Divider register – Internal clock dividers are used to generate different clock frequencies required for card. The division factor for each clock divider can be programmed by writing to the Clock Divider register. The clock divider is an 8-bit value that provides a clock division factor from 1 to 510; a value of 0 represents a clock-divider bypass, a value of 1 represents a divide by 2, a value of 2 represents a divide by 4, and so on.
- Clock Control register – cclk_out can be enabled or disabled for each card under the following conditions:
  - clk_enable – cclk_out for a card is enabled if the clk_enable bit for a card in the Clock Control register is programmed (set to 1) or disabled (set to 0).
  - Low-power mode – Low-power mode of a card can be enabled by setting the low-power mode bit of the Clock Control register to 1. If low-power mode is enabled to save card power, the cclk_out is disabled when the card is idle for at least 8 card clock cycles. It is enabled when a new command is loaded and the command path goes to a non-idle state.

Additionally, cclk_out is disabled when an internal FIFO is full – card read (no more data can be received from card) – or when the FIFO is empty – card write (no data is available for transmission). This helps to avoid FIFO overrun and underrun conditions. It is used by the command and data path to qualify cclk_in for driving outputs and sampling inputs at the programmed clock frequency for the selected card, according to the Clock Divider and Clock Source register values.

Under the following conditions, the card clock is stopped or disabled, along with the active clk_en, for the selected card:

- Clock can be disabled by writing to Clock Enable register (clk_en bit = 1).
- If low-power mode is selected and card is idle, or not selected for 8 clocks.
- FIFO is full and data path cannot accept more data from the card and data transfer is incomplete –to avoid FIFO overrun.
- FIFO is empty and data path cannot transmit more data to the card and data transfer is incomplete – to avoid FIFO underrun.

6. Error Detection

- Response
  - Response timeout – Response expected with response start bit is not received within programmed number of clocks in timeout register.
  - Response CRC error – Response is expected and check response CRC requested; response CRC7 does not match with the internally-generated CRC7.
  - Response error – Response transmission bit is not 0, command index does not match with the command index of the send command, or response end bit is not 1.
- Data transmit

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- No CRC status – During a write data transfer, if the CRC status start bit is not received two clocks after the end bit of the data block is sent out, the data path does the following:
  - Signals no CRC status error to the BIU
  - Terminates further data transfer
  - Signals data transfer done to the BIU
- Negative CRC – If the CRC status received after the write data block is negative (that is, not 010), a data CRC error is signaled to the BIU and further data transfer is continued.
- Data starvation due to empty FIFO – If the FIFO becomes empty during a write data transmission, or if the card clock is stopped and the FIFO remains empty for data timeout clocks, then a data-starvation error is signaled to the BIU and the data path continues to wait for data in the FIFO.

- Data receive
  - Data timeout – During a read-data transfer, if the data start bit is not received before the number of clocks that were programmed in the timeout register, the data path does the following:
    - Signals data-timeout error to the BIU
    - Terminates further data transfer
    - Signals data transfer done to BIU
  - Data start bit error – During a 4-bit or 8-bit read-data transfer, if the all-bit data line does not have a start bit, the data path signals a data start bit error to the BIU and waits for a data timeout, after which it signals that the data transfer is done.
  - Data CRC error – During a read-data-block transfer, if the CRC16 received does not match with the internally generated CRC16, the data path signals a data CRC error to the BIU and continues further data transfer.
  - Data end-bit error – During a read-data transfer, if the end bit of the received data is not 1, the data path signals an end-bit error to the BIU, terminates further data transfer, and signals to the BIU that the data transfer is done.
  - Data starvation due to FIFO full – During a read data transmission and when the FIFO becomes full, the card clock is stopped. If the FIFO remains full for data timeout clocks, a data starvation error is signaled to the BIU (Data Starvation by Host Timeout bit is set in SDMMC_RINTSTS register) and the data path continues to wait for the FIFO to start to empty.

3.3.3 Internal Direct Memory Access Controller (IDMAC)

The Internal Direct Memory Access Controller (IDMAC) has a Control and Status Register (CSR) and a single Transmit/Receive engine, which transfers data from host memory to the device port and vice versa. The controller utilizes a descriptor to efficiently move data from source to destination with minimal Host CPU intervention. You can program the controller to interrupt the Host CPU in situations such as data Transmit and Receive transfer completion from the card, as well as other normal or error conditions.
The IDMAC and the Host driver communicate through a single data structure. CSR addresses 0x80 to 0x98 are reserved for host programming.
The IDMAC transfers the data received from the card to the Data Buffer in the Host memory, and it transfers Transmit data from the Data Buffer in the Host memory to the FIFO. Descriptors that reside in the Host memory act as pointers to these buffers.
A data buffer resides in physical memory space of the Host and consists of complete data or partial data. Buffers contain only data, while buffer status is maintained in the descriptor. Data chaining refers to data that spans multiple data buffers. However, a single descriptor

cannot span multiple data.
A single descriptor is used for both reception and transmission. The base address of the list is written into Descriptor List Base Address Register (SDMMC_DBADDR @0x88). A descriptor list is forward linked. The Last Descriptor can point back to the first entry in order to create a ring structure. The descriptor list resides in the physical memory address space of the Host. Each descriptor can point to a maximum of two data buffers.

1. IDMAC CSR Access

When an IDMAC is introduced, an additional CSR space resides in the IDMAC that controls the IDMAC functionality. The host accesses the new CSR space in addition to the existing control register set in the BIU. The IDMAC CSR primarily contains descriptor information. For a write operation to the CSR, the respective CSR logic of the IDMAC and BIU decodes the address before accepting. For a read operation from the CSR, the appropriate CSR read path is enabled.
You can enable or disable the IDMAC operation by programming bit[25] in the SDMMC_CTRL register of the BIU. This allows the data transfer by accessing the slave interface on the AMBA bus if the IDMAC is present but disabled. When IDMAC is enabled, the FIFO cannot be accessed through the slave interface.

2. Descriptors

- Descriptor structures

The IDMAC uses these types of descriptor structures:

- Dual-Buffer Structure – The distance between two descriptors is determined by the Skip Length value programmed in the Descriptor Skip Length (DSL) field of the Bus Mode Register (SDMMC_BMOD @0x80).

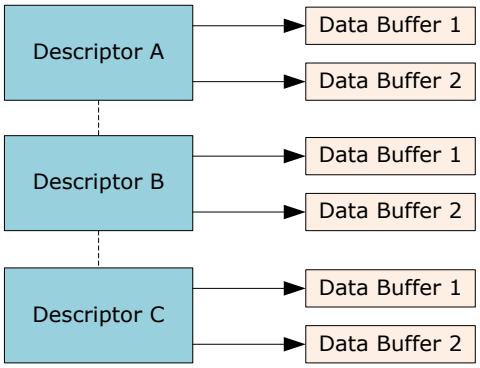


Fig. 3-6 Dual-Buffer Descriptor Structure

- Chain Structure – Each descriptor points to a unique buffer and the next descriptor.

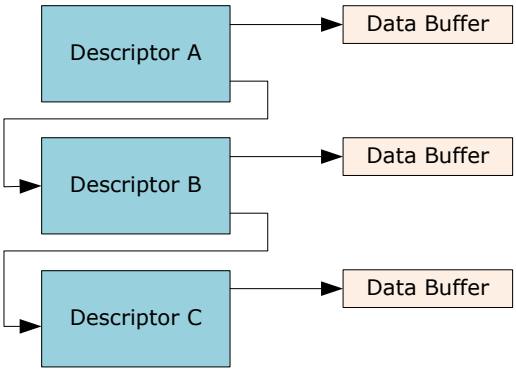


Fig. 3-7 Chain Descriptor Structure

- Descriptor formats

Following figure illustrates the internal formats of a descriptor. The descriptor addresses must be aligned to the bus width used for 32-bit AHB data buses. Each descriptor contains 16 bytes of control and status information. DES0 is a notation used to denote the [31:0] bits, DES1 to denote [63:32] bits, DES2 to denote [95:64] bits, DES3 to denote [127:96]

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bits.

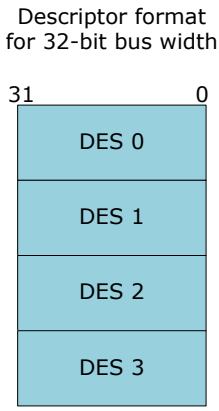


Fig. 3-8 Descriptor Formats for 32-bit AHB Address Bus Width

- The DES0 element in the IDMAC contains control and status information.

Table 3-4 Bits in IDMAC DES0 Element

Bit	Name	Description
31	OWN	When set, this bit indicates that the descriptor is owned by the IDMAC. When this bit is reset, it indicates that the descriptor is owned by the Host. The IDMAC clears this bit when it completes the data transfer.
30	Card Error Summary (CES)	These error bits indicate the status of the transaction to or from the card. These bits are also present in SDMMC_RINTSTS Indicates the logical OR of the following bits: ● EBE: End Bit Error ● RTO: Response Time out ● RCRC: Response CRC ● SBE: Start Bit Error ● DRTO: Data Read Timeout ● DCRC: Data CRC for Receive ● RE: Response Error
29:6	Reserved	-
5	End of Ring (ER)	When set, this bit indicates that the descriptor list reached its final descriptor. The IDMAC returns to the base address of the list, creating a Descriptor Ring. This is meaningful for only a dual-buffer descriptor structure.
4	Second Address Chained (CH)	When set, this bit indicates that the second address in the descriptor is the Next Descriptor address rather than the second buffer address. When this bit is set, BS2 (DES1[25:13]) should be all zeros.
3	First Descriptor (FS)	When set, this bit indicates that this descriptor contains the first buffer of the data. If the size of the first buffer is 0, next Descriptor contains the beginning of the data.
2	Last Descriptor (LD)	This bit is associated with the last block of a DMA transfer. When set, the bit indicates that the buffers pointed to by this descriptor are the last buffers of the data. After this descriptor is completed, the remaining byte count is 0. In other words, after the descriptor with the LD bit set is completed, the remaining byte count should be 0.
1	Disable Interrupt on	When set, this bit will prevent the setting of the TI/RI bit of the IDMAC Status Register (IDSTS) for the data that ends in

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Bit	Name	Description
	Completion (DIC)	the buffer pointed to by this descriptor.
0	Reserved	-

- The DES1 element contains the buffer size.

Table 3-5 Bits in IDMAC DES1 Element

Bit	Name	Description
31:26	Reserved	-
25:13	Buffer 2 Size (BS2)	These bits indicate the second data buffer byte size. The buffer size must be a multiple of 2, 4, or 8, depending upon the bus widths—16, 32, and 64 respectively. In the case where the buffer size is not a multiple of 2, 4, or 8, the resulting behavior is undefined. If this field is 0, the DMA ignores this buffer and proceeds to the next buffer in case of a dual-buffer structure. This field is not valid for chain structure; that is, if DES0[4] is set.
12:0	Buffer 1 Size (BS1)	Indicates the data buffer byte size, which must be a multiple of 2, 4, or 8 bytes, depending upon the bus widths—16, 32, and 64, respectively. In the case where the buffer size is not a multiple of 2, 4, or 8, the resulting behavior is undefined. This field should not be zero. Note: If there is only one buffer to be programmed, you need to use only the Buffer 1, and not Buffer 2.

- The DES2 element contains the address pointer to the data buffer.

Table 3-6 Bits in IDMAC DES2 Element

Bit	Name	Description
31:26	Reserved	
25:13	Buffer 2 Size (BS2)	These bits indicate the second data buffer byte size. The buffer size must be a multiple of 2, 4, or 8, depending upon the bus widths—16, 32, and 64 respectively. In the case where the buffer size is not a multiple of 2, 4, or 8, the resulting behavior is undefined. If this field is 0, the DMA ignores this buffer and proceeds to the next buffer in case of a dual-buffer structure. This field is not valid for chain structure; that is, if DES0[4] is set.
12:0	Buffer 1 Size (BS1)	Indicates the data buffer byte size, which must be a multiple of 2, 4, or 8 bytes, depending upon the bus widths—16, 32, and 64, respectively. In the case where the buffer size is not a multiple of 2, 4, or 8, the resulting behavior is undefined. This field should not be zero. Note: If there is only one buffer to be programmed, you need to use only the Buffer 1, and not Buffer 2.

- The DES3 element contains the address pointer to the next descriptor if the present descriptor is not the last descriptor in a chained descriptor structure or the second buffer address for a dual-buffer structure.

Table 3-7 Bits in IDMAC DES3 Element

Bit	Name	Description
31:0	Buffer Address Pointer 2/ Next Descriptor Address (BAP2)	These bits indicate the physical address of the second buffer when the dual-buffer structure is used. If the Second Address Chained (DES0[4]) bit is set, then this address contains the pointer to the physical memory where the Next Descriptor is present. If this is not the last descriptor, then the Next Descriptor

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Bit	Name	Description
		address pointer must be bus-width aligned.

3. Initialization

IDMAC initialization occurs as follows:

1) Write to IDMAC Bus Mode Register—SDMMC_BMOD to set Host bus access parameters.
2) Write to IDMAC Interrupt Enable Register—SDMMC_IDINTEN to mask unnecessary interrupt causes.
3) The software driver creates either the Transmit or the Receive descriptor list. Then it writes to IDMAC Descriptor List Base Address Register (SDMMC_DBADDR), providing the IDMAC with the starting address of the list.
4) The IDMAC engine attempts to acquire descriptors from the descriptor lists.

- Host Bus Burst Access

The IDMAC attempts to execute fixed-length burst transfers on the AHB Master interface if configured using the FB bit of the IDMAC Bus Mode register. The maximum burst length is indicated and limited by the PBL field. The descriptors are always accessed in the maximum possible burst-size for the 16-bytes to be read— 16*8/bus-width.
The IDMAC initiates a data transfer only when sufficient space to accommodate the configured burst is available in the FIFO or the number of bytes to the end of data, when less than the configured burst-length.
The IDMAC indicates the start address and the number of transfers required to the AHB Master Interface. When the AHB Interface is configured for fixed-length bursts, then it transfers data using the best combination of INCR4/8/16 and SINGLE transactions. Otherwise, in no fixed-length bursts, it transfers data using INCR (undefined length) and SINGLE transactions.

- Host Data Buffer Alignment

The Transmit and Receive data buffers in host memory must be aligned, depending on the data width.

- Buffer Size Calculations

The driver knows the amount of data to transmit or receive. For transmitting to the card, the IDMAC transfers the exact number of bytes to the FIFO, indicated by the buffer size field of DES1.
If a descriptor is not marked as last-LS bit of DES0-then the corresponding buffer(s) of the descriptor are full, and the amount of valid data in a buffer is accurately indicated by its buffer size field. If a descriptor is marked as last, then the buffer cannot be full, as indicated by the buffer size in DES1. The driver is aware of the number of locations that are valid in this case.

- Transmission

IDMAC transmission occurs as follows:

1) The Host sets up the elements (DES0-DES3) for transmission and sets the OWN bit (DES0[31]). The Host also prepares the data buffer.
2) The Host programs the write data command in the SDMMC_CMD register in BIU.
3) The Host will also program the required transmit threshold level (TX_WMark field in SDMMC_FIFOTH register).
4) The IDMAC determines that a write data transfer needs to be done as a consequence of step 2.
5) The IDMAC engine fetches the descriptor and checks the OWN bit. If the OWN bit is not set, it means that the host owns the descriptor. In this case the IDMAC enters suspend state and asserts the Descriptor Unable interrupt in the SDMMC_IDSTS register. In such a case, the host needs to release the IDMAC by writing any value to the poll demand register.

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6) It will then wait for Command Done (CD) bit and no errors from BIU which indicates that a transfer can be done.
7) The IDMAC engine will now wait for a DMA interface request from BIU. This request will be generated based on the programmed transmit threshold value. For the last bytes of data which can't be accessed using a burst, SINGLE transfers are performed on AHB Master Interface.
8) The IDMAC fetches the Transmit data from the data buffer in the Host memory and transfers to the FIFO for transmission to card.
9) When data spans across multiple descriptors, the IDMAC will fetch the next descriptor and continue with its operation with the next descriptor. The Last Descriptor bit in the descriptor indicates whether the data spans multiple descriptors or not.
10) When data transmission is complete, status information is updated in SDMMC_IDSTS register by setting Transmit Interrupt, if enabled. Also, the OWN bit is cleared by the IDMAC by performing a write transaction to DES0.

- Reception

IDMAC reception occurs as follows:

1) The Host sets up the element (DES0-DES3) for reception, sets the OWN (DES0[31]).
2) The Host programs the read data command in the SDMMC_CMD register in BIU.
3) The Host will program the required receive threshold level (RX_WMark field in FIFOTH register).
4) The IDMAC determines that a read data transfer needs to be done as a consequence of step 2.
5) The IDMAC engine fetches the descriptor and checks the OWN bit. If the OWN bit is not set, it means that the host owns the descriptor. In this case the DMA enters suspend state and asserts the Descriptor Unable interrupt in the SDMMC_IDSTS register. In such a case, the host needs to release the IDMAC by writing any value to the poll demand register.
6) It will then wait for Command Done (CD) bit and no errors from BIU which indicates that a transfer can be done.
7) The IDMAC engine will now wait for a DMA interface request from BIU. This request will be generated based on the programmed receive threshold value. For the last bytes of data which can't be accessed using a burst, SINGLE transfers are performed on AHB.
8) The IDMAC fetches the data from the FIFO and transfer to Host memory.
9) When data spans across multiple descriptors, the IDMAC will fetch the next descriptor and continue with its operation with the next descriptor. The Last Descriptor bit in the descriptor indicates whether the data spans multiple descriptors or not.
10) When data reception is complete, status information is updated in SDMMC_IDSTS register by setting Receive Interrupt, if enabled. Also, the OWN bit is cleared by the IDMAC by performing a write transaction to DES0.

- Interrupts

Interrupts can be generated as a result of various events. SDMMC_IDSTS register contains all the bits that might cause an interrupt. SDMMC_IDINTEN register contains an Enable bit for each of the events that can cause an interrupt.
There are two groups of summary interrupts-Normal and Abnormal-as outlined in SDMMC_IDSTS register. Interrupts are cleared by writing a 1 to the corresponding bit position. When all the enabled interrupts within a group are cleared, the corresponding summary bit is cleared. When both the summary bits are cleared, the interrupt signal dmac_intr_o is de-asserted.

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Interrupts are not queued and if the interrupt event occurs before the driver has responded to it, no additional interrupts are generated. For example, Receive Interrupt— SDMMC_IDSTS[1] indicates that one or more data was transferred to the Host buffer.
An interrupt is generated only once for simultaneous, multiple events. The driver must scan SDMMC_IDSTS register for the interrupt cause.

3.4 Register Description

3.4.1 Registers Summary

Name	Offset	Size	Reset Value	Description
SDMMC_CTRL	0x0000	W	0x00000000	Control register
SDMMC_PWREN	0x0004	W	0x00000000	Power-enable register
SDMMC_CLKDIV	0x0008	W	0x00000000	Clock-divider register
SDMMC_CLKSRC	0x000c	W	0x00000000	SD Clock Source Register
SDMMC_CLKENA	0x0010	W	0x00000000	Clock-enable register
SDMMC_TMOUT	0x0014	W	0xffffff40	Time-out register
SDMMC_CTYPE	0x0018	W	0x00000000	Card-type register
SDMMC_BLKSIZ	0x001c	W	0x00000200	Block-size register
SDMMC_BYTCNT	0x0020	W	0x00000200	Byte-count register
SDMMC_INTMASK	0x0024	W	0x00000000	Interrupt-mask register
SDMMC_CMDARG	0x0028	W	0x00000000	Command-argument register
SDMMC_CMD	0x002c	W	0x00000000	Command register
SDMMC_RESP0	0x0030	W	0x00000000	Response-0 register
SDMMC_RESP1	0x0034	W	0x00000000	Response-1 register
SDMMC_RESP2	0x0038	W	0x00000000	Response-2 register
SDMMC_RESP3	0x003c	W	0x00000000	Response-3 register
SDMMC_MINTSTS	0x0040	W	0x00000000	Masked interrupt-status register
SDMMC_RINTSTS	0x0044	W	0x00000000	Raw interrupt-status register
SDMMC_STATUS	0x0048	W	0x00000406	Status register
SDMMC_FIFOTH	0x004c	W	0x00000000	FIFO threshold register
SDMMC_CDETECT	0x0050	W	0x00000000	Card-detect register
SDMMC_WRTPRT	0x0054	W	0x00000000	Write-protect register
SDMMC_TCBCNT	0x005c	W	0x00000000	Transferred CIU card byte count
SDMMC_TBBCNT	0x0060	W	0x00000000	Transferred host/DMA to/from BIU-FIFO byte count
SDMMC_DEBNCE	0x0064	W	0x00ffffff	Card detect debounce register
SDMMC_USRID	0x0068	W	0x07967797	User ID register
SDMMC_VERID	0x006c	W	0x5342270a	Synopsys version ID register
SDMMC_HCON	0x0070	W	0x00000000	Hardware configuration register
SDMMC_UHS_REG	0x0074	W	0x00000000	UHS-1 register
SDMMC_RSTN	0x0078	W	0x00000001	Hardware reset register
SDMMC_BMOD	0x0080	W	0x00000000	Bus mode register
SDMMC_PLDMND	0x0084	W	0x00000000	Poll demand register
SDMMC_DBADDR	0x0088	W	0x00000000	Descriptor list base address register
SDMMC_IDSTS	0x008c	W	0x00000000	Internal DMAC status register

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Name	Offset	Size	Reset Value	Description
SDMMC_IDINTEN	0x0090	W	0x00000000	Internal DMAC interrupt enable register
SDMMC_DSCADDR	0x0094	W	0x00000000	Current host descriptor address register
SDMMC_BUFADDR	0x0098	W	0x00000000	Current buffer descriptor address register
SDMMC_CARDTHRCTL	0x0100	W	0x00000000	Card read threshold enable register
SDMMC_BACK_END_POWER	0x0104	W	0x00000000	Back-end power register
SDMMC_EMMC_DDR_REG	0x010c	W	0x00000000	eMMC 4.5 ddr start bit detection control register
SDMMC_FIFO_BASE	0x0200	W	0x00000000	FIFO base address register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

3.4.2 Detail Register Description

SDMMC_CTRL

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25	RW	0x0	use_internal_dmac Present only for the Internal DMAC configuration; else, it is reserved. 1'b0: The host performs data transfers through the slave interface 1'b1: Internal DMAC used for data transfe
24:12	RO	0x0	reserved
11	RW	0x0	ceata_device_interrupt_status 1'b0: Interrupts not enabled in CE-ATA device 1'b1: Interrupts are enabled in CE-ATA device Software should appropriately write to this bit after power-on reset or any other reset to CE-ATA device. After reset, usually CE-ATA device interrupt is disabled. If the host enables CE-ATA device interrupt, then software should set this bit

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Bit	Attr	Reset Value	Description
10	RW	0x0	send_auto_stop_ccsd 1'b0: Clear bit if DWC_mobile_storage does not reset the bit. 1'b1: Send internally generated STOP after sending CCSD to CE-ATA device. NOTE: Always set send_auto_stop_ccsd and send_ccsd bits together send_auto_stop_ccsd should not be set independent of send_ccsd. When set, the Host Controller automatically sends internally-generated STOP command (CMD12) to CE-ATA device. After sending internally-generated STOP command, Auto Command Done (ACD) bit in SDMMC_RINTSTS is set and generates interrupt to host if Auto Command Done interrupt is not masked. After sending the CCSD, DWC_mobile_storage automatically clears send_auto_stop_ccsd bit
9	RW	0x0	send_ccsd 1'b0: Clear bit if DWC_mobile_storage does not reset the bit 1'b1: Send Command Completion Signal Disable (CCSD) to CE-ATA device When set, DWC_mobile_storage sends CCSD to CE-ATA device. Software sets this bit only if current command is expecting CCS (that is, RW_BLK) and interrupts are enabled in CE-ATA device.Once the CCSD pattern is sent to device, DWC_mobile_storage automatically clears send_ccsd bit. It also sets Command Done (CD) bit in SDMMC_RINTSTS register and generates interrupt to host if Command Done interrupt is not masked. NOTE: Once send_ccsd bit is set, it takes two card clock cycles to drive the CCSD on the CMD line. Due to this, during the boundary conditions it may happen that CCSD is sent to the CE-ATA device, even if the device signalled CCS
8	RW	0x0	abort_read_data 1'b0: no change 1'b1: after suspend command is issued during read-transfer, software polls card to find when suspend happened. Once suspend occurs, software sets bit to reset data state-machine, which is waiting for next block of data. Bit automatically clears once data state machine resets to idle. Used in SDIO card suspend sequence

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Bit	Attr	Reset Value	Description
7	RW	0x0	send_irq_response 1'b0: no change 1'b1: send auto IRQ response Bit automatically clears once response is sent. To wait for MMC card interrupts, host issues CMD40, and SDMMC Controller waits for interrupt response from MMC card(s). In meantime, if host wants SDMMC Controller to exit waiting for interrupt state, it can set this bit, at which time SDMMC Controller command state-machine sends CMD40 response on bus and returns to idle state
6	RW	0x0	read_wait 1'b0: clear read wait 1'b1: assert read wait For sending read-wait to SDIO cards
5	RW	0x0	dma_enable 1'b0: disable DMA transfer mode 1'b1: enable DMA transfer mode Even when DMA mode is enabled, host can still push/pop data into or from FIFO; this should not happen during the normal operation. If there is simultaneous FIFO access from host/DMA, the data coherency is lost. Also, there is no arbitration inside SDMMC Controller to prioritize simultaneous host/DMA access
4	RW	0x0	int_enable Global interrupt enable/disable bit: 1'b0: disable interrupts 1'b1: enable interrupts The int port is 1 only when this bit is 1 and one or more unmasked interrupts are set
3	RO	0x0	reserved
2	RW	0x0	dma_reset 1'b0: no change 1'b1: reset internal DMA interface control logic To reset DMA interface, firmware should set bit to 1. This bit is auto-cleared after two AHB clocks
1	RW	0x0	fifo_reset 1'b0: no change 1'b1: reset to data FIFO To reset FIFO pointers To reset FIFO, firmware should set bit to 1. This bit is auto-cleared after completion of reset operation

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Bit	Attr	Reset Value	Description
0	RW	0x0	controller_reset 1'b0: no change 1'b1: reset SDMMC controller To reset controller, firmware should set bit to 1. This bit is auto-cleared after two AHB and two cclk_in clock cycles. This resets: a. BIU/CIU interface b. CIU and state machines c. abort_read_data, send_irq_response, and read_wait bits of Control register d. start_cmd bit of Command register Does not affect any registers or DMA interface, or FIFO or host interrupts

SDMMC_PWREN

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	power_enable Power on/off switch for the card. Once power is turned on, firmware should wait for regulator/switch ramp-up time before trying to initialize card. 1'b0: power off 1'b1: power on Bit values output to card_power_en port

SDMMC_CLKDIV

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x00	clk_divider0 Clock divider-0 value. Clock division is 2*n. For example, value of 0 means divide by 2*0 = 0 (no division, bypass), value of 1 means divide by 2*1 = 2, and so on

SDMMC_CLKSRC

Address: Operational Base + offset (0x000c)

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Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1:0	RW	0x0	clk_source Clock divider source for up to 16 SD cards supported. Each card has two bits assigned to it. For example, bits[1:0] assigned for card-0, which maps and internally routes clock divider[3:0] outputs to cclk_out[15:0] pins, depending on bit value. 2'b00: clock divider 0

SDMMC_CLKENA

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:17	RO	0x0	reserved
16	RW	0x0	cclk_low_power Low-power control for SD card clock and MMC card clock supported. 1'b0: non-low-power mode 1'b1: low-power mode; stop clock when card in IDLE (should be normally set to only MMC and SD memory cards; for SDIO cards, if interrupts must be detected, clock should not be stopped)
15:1	RO	0x0	reserved
0	RW	0x0	cclk_enable Clock-enable control for SD card clock and MMC card clock supported. 1'b0: clock disabled 1'b1: clock enabled

SDMMC_TMOUT

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:8	RW	0x000000	data_timeout Value for card Data Read Timeout; same value also used for Data Starvation by Host timeout. Value is in number of card output clocks cclk_out of selected card. Note: The software timer should be used if the timeout value is in the order of 100 ms. In this case, read data timeout interrupt needs to be disabled
7:0	RW	0x40	response_timeout Response timeout value. Value is in number of card output clock

SDMMC_CTYPE

Address: Operational Base + offset (0x0018)

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Bit	Attr	Reset Value	Description
31:17	RO	0x0	reserved
16	RW	0x0	card_width_8 Indicates if card is 8-bit. 1'b0: non 8-bit mode 1'b1: 8-bit mode
15:1	RO	0x0	reserved
0	RW	0x0	card_width Indicates if card is 1-bit or 4-bit. 1'b0: 1-bit mode 1'b1: 4-bit mode

SDMMC_BLKSIZ

Address: Operational Base + offset (0x001c)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0000	block_size Block size

SDMMC_BYTCNT

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	byte_count Number of bytes to be transferred; should be integer multiple of Block Size for block transfers. For undefined number of byte transfers, byte count should be set to 0. When byte count is set to 0, it is responsibility of host to explicitly send stop/abort command to terminate data transfer

SDMMC_INTMASK

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24	RW	0x0	sdio_int_mask Mask SDIO interrupts. When masked, SDIO interrupt detection for that card is disabled. A 0 masks an interrupt, and 1 enables an interrupt
23:17	RO	0x0	reserved
16	RW	0x0	data_nobusy_int_mask 1'b0: data no busy interrupt not masked 1'b1: data no busy interrupt masked

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Bit	Attr	Reset Value	Description
15:0	RW	0x0000	int_mask Bits used to mask unwanted interrupts. Value of 0 masks interrupt; value of 1 enables interrupt. bit 15: End-bit error (read)/Write no CRC (EBE) bit 14: Auto command done (ACD) bit 13: Start-bit error (SBE) bit 12: Hardware locked write error (HLE) bit 11: FIFO underrun/overrun error (FRUN) bit 10: Data starvation-by-host timeout (HTO) /Volt_switch_int bit 9: Data read timeout (DRTO) bit 8: Response timeout (RTO) bit 7: Data CRC error (DCRC) bit 6: Response CRC error (RCRC) bit 5: Receive FIFO data request (RXDR) bit 4: Transmit FIFO data request (TXDR) bit 3: Data transfer over (DTO) bit 2: Command done (CD) bit 1: Response error (RE) bit 0: Card detect (CD)

SDMMC_CMDARG

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	cmd_arg Value indicates command argument to be passed to card

SDMMC_CMD

Address: Operational Base + offset (0x002c)

Bit	Attr	Reset Value	Description
31	RW	0x0	start_cmd Start command. Once command is taken by CIU, bit is cleared. When bit is set, host should not attempt to write to any command registers. If write is attempted, hardware lock error is set in raw interrupt register. Once command is sent and response is received from SD_MMC cards, Command Done bit is set in raw interrupt register
30	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
29	RW	0x0	use_hold_reg Use Hold Register. 1'b0: CMD and DATA sent to card bypassing HOLD Register 1'b1: CMD and DATA sent to card through the HOLD Register Note: a. Set to 1'b1 for SDR12 and SDR25 (with non-zero phase-shifted cclk_in_drv); zero phase shift is not allowed in these modes. b. Set to 1'b0 for SDR50, SDR104, and DDR50 (with zero phase-shifted cclk_in_drv) c. Set to 1'b1 for SDR50, SDR104, and DDR50 (with non-zero phase-shifted cclk_in_drv)
28	RW	0x0	volt_switch Voltage switch bit. 1'b0: no voltage switching 1'b1: voltage switching enabled; must be set for CMD11 only
27	RW	0x0	boot_mode Boot Mode. 1'b0: mandatory boot operation 1'b1: alternate boot operation
26	RW	0x0	disable_boot Disable boot. When software sets this bit along with start_cmd, CIU terminates the boot operation. Do NOT set disable_boot and enable_boot together
25	RW	0x0	expect_boot_ack Expect Boot Acknowledge. When Software sets this bit along with enable_boot, CIU expects a boot acknowledge start pattern of 0-1-0 from the selected card
24	RW	0x0	enable_boot Enable Boot. This bit should be set only for mandatory boot mode.When Software sets this bit along with start_cmd, CIU starts the boot sequence for the corresponding card by asserting the CMD line low. Do NOT set disable_boot and enable_boot together
23	RW	0x0	ccs_expected 1'b0: command does not expect CCS from device 1'b1: command expects CCS from device If the command expects Command Completion Signal (CCS) from the CE-ATA device, the software should set this control bit. The Host Controller sets Data Transfer Over (DTO) bit in SDMMC_RINTSTS register and generates interrupt to host if Data Transfer Over interrupt is not masked

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Bit	Attr	Reset Value	Description
22	RW	0x0	read_ceata_device 1'b0: Host is not performing read access (RW_REG or RW_BLK) towards CE-ATA device 1'b1: Host is performing read access (RW_REG or RW_BLK) towards CE-ATA device Software should set this bit to indicate that CE-ATA device is being accessed for read transfer. This bit is used to disable read data timeout indication while performing CE-ATA read transfers. Maximum value of I/O transmission delay can be no less than 10 seconds. DWC_mobile_storage should not indicate read data timeout while waiting for data from CE-ATA device
21	RW	0x0	update_clock_registers_only 1'b0: normal command sequence 1'b1: do not send commands, just update clock register value into card clock domain Following register values transferred into card clock domain: CLKDIV, CLRSRC, CLKENA. Changes card clocks (change frequency, truncate off or on, and set low-frequency mode); provided in order to change clock frequency or stop clock without having to send command to cards. During normal command sequence, when update_clock_registers_only=0, following control registers are transferred from BIU to CIU: CMD, CMDARG, TMOUT, CTYPE, BLKSIZ, BYTCNT. CIU uses new register values for new command sequence to card. When bit is set, there are no Command Done interrupts because no command is sent to SD_MMC_CEATA cards
20:16	RO	0x0	reserved
15	RW	0x0	send_initialization 1'b0: do not send initialization sequence (80 clocks of 1) before sending this command 1'b1: send initialization sequence before sending this command After power on, 80 clocks must be sent to card for initialization before sending any commands to card. Bit should be set while sending first command to card so that controller will initialize clocks before sending command to card. This bit should not be set for either of the boot modes (alternate or mandatory)

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Bit	Attr	Reset Value	Description
14	RW	0x0	stop_abort_cmd 1'b0: neither stop nor abort command to stop current data transfer in progress. If abort is sent to function-number currently selected or not in data-transfer mode, then bit should be set to 0. 1'b1: stop or abort command intended to stop current data transfer in progress. When open-ended or predefined data transfer is in progress, and host issues stop or abort command to stop data transfer, bit should be set so that command/data state-machines of CIU can return correctly to idle state. This is also applicable for Boot mode transfers. To Abort boot mode, this bit should be set along with CMD[26]=disable_boot
13	RW	0x0	wait_prvdata_complete 1'b0: send command at once, even if previous data transfer has not completed 1'b1: wait for previous data transfer completion before sending command The wait_prvdata_complete=0 option typically used to query status of card during data transfer or to stop current data transfer; card_number should be same as in previous command
12	RW	0x0	send_auto_stop 1'b0: no stop command sent at end of data transfer 1'b1: send stop command at end of data transfer When set, SDMMC Controller sends stop command to SD_MMC cards at end of data transfer. a. when send_auto_stop bit should be set, since some data transfers do not need explicit stop commands b. open-ended transfers that software should explicitly send to stop command Additionally, when "resume" is sent to resume-suspended memory access of SD-Combo card -bit should be set correctly if suspended data transfer needs send_auto_stop. Don't care if no data expected from card
11	RW	0x0	transfer_mode 1'b0: block data transfer command 1'b1: stream data transfer command Don't care if no data expected
10	RW	0x0	wr 1'b0: read from card 1'b1: write to card Don't care if no data expected from card
9	RW	0x0	data_expected 1'b0: no data transfer expected (read/write) 1'b1: data transfer expected (read/write)

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Bit	Attr	Reset Value	Description
8	RW	0x0	check_response_crc 1'b0: do not check response CRC 1'b1: check response CRC Some of command responses do not return valid CRC bits. Software should disable CRC checks for those commands in order to disable CRC checking by controller
7	RW	0x0	response_length 1'b0: short response expected from card 1'b1: long response expected from card
6	RW	0x0	response_expect 1'b0: no response expected from card 1'b1: response expected from card
5:0	RW	0x00	cmd_index Command index

SDMMC_RESP0

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	response0 Bit[31:0] of response

SDMMC_RESP1

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	response1 Register represents bit[63:32] of long response. When CIU sends auto-stop command, then response is saved in register. Response for previous command sent by host is still preserved in Response 0 register. Additional auto-stop issued only for data transfer commands, and response type is always "short" for them

SDMMC_RESP2

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	response2 Bit[95:64] of long response

SDMMC_RESP3

Address: Operational Base + offset (0x003c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	response3 Bit[127:96] of long response

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SDMMC_MINTSTS

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24	RW	0x0	sdio_interrupt Interrupt from SDIO card; SDIO interrupt for card enabled only if corresponding sdio_int_mask bit is set in Interrupt mask register (mask bit 1 enables interrupt; 0 masks interrupt). 1'b0: no SDIO interrupt from card 1'b1: SDIO interrupt from card
23:17	RO	0x0	reserved
16	RW	0x0	data_nobusy_int_status Data no busy interrupt status, high active
15:0	RW	0x0000	int_status Interrupt enabled only if corresponding bit in interrupt mask register is set. bit 15: End-bit error (read)/Write no CRC (EBE) bit 14: Auto command done (ACD) bit 13: Start-bit error (SBE) bit 12: Hardware locked write error (HLE) bit 11: FIFO underrun/overrun error (FRUN) bit 10: Data starvation-by-host timeout (HTO) /Volt_switch_int bit 9: Data read timeout (DRTO) bit 8: Response timeout (RTO) bit 7: Data CRC error (DCRC) bit 6: Response CRC error (RCRC) bit 5: Receive FIFO data request (RXDR) bit 4: Transmit FIFO data request (TXDR) bit 3: Data transfer over (DTO) bit 2: Command done (CD) bit 1: Response error (RE) bit 0: Card detect (CD)

SDMMC_RINTSTS

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24	RW	0x0	sdio_interrupt Interrupt from SDIO card; Writes to these bits clear them. Value of 1 clears bit and 0 leaves bit intact. 1'b0: no SDIO interrupt from card 1'b1: SDIO interrupt from card
23:17	RO	0x0	reserved
16	RW	0x0	data_nobusy_int_status Data no busy interrupt status, high active

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Bit	Attr	Reset Value	Description
15:0	RW	0x0000	int_status Writes to bits clear status bit. Value of 1 clears status bit, and value of 0 leaves bit intact. Bits are logged regardless of interrupt mask status. bit 15: End-bit error (read)/Write no CRC (EBE) bit 14: Auto command done (ACD) bit 13: Start-bit error (SBE) bit 12: Hardware locked write error (HLE) bit 11: FIFO underrun/overrun error (FRUN) bit 10: Data starvation-by-host timeout (HTO) /Volt_switch_int bit 9: Data read timeout (DRTO) bit 8: Response timeout (RTO) bit 7: Data CRC error (DCRC) bit 6: Response CRC error (RCRC) bit 5: Receive FIFO data request (RXDR) bit 4: Transmit FIFO data request (TXDR) bit 3: Data transfer over (DTO) bit 2: Command done (CD) bit 1: Response error (RE) bit 0: Card detect (CD)

SDMMC_STATUS

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31	RW	0x0	dma_req DMA request signal state
30	RO	0x0	dma_ack DMA acknowledge signal state
29:17	RO	0x0000	fifo_count Number of filled locations in FIFO
16:11	RO	0x00	response_index Index of previous response, including any auto-stop sent by core
10	RO	0x1	data_state_mc_busy Data transmit or receive state-machine is busy
9	RW	0x0	data_busy Inverted version of raw selected card_data[0]. 1'b0: card data not busy 1'b1: card data busy default value is 1 or 0 depending on cdata_in
8	RW	0x0	data_3_status Raw selected card_data[3]; checks whether card is present. 1'b0: card not present 1'b1: card present default value is 1 or 0 depending on cdata_in

Bit	Attr	Reset Value	Description
7:4	RW	0x0	command_fsm_states Command FSM states: 4'h0: idle 4'h1: send init sequence 4'h2: Tx cmd start bit 4'h3: Tx cmd tx bit 4'h4: Tx cmd index + arg 4'h5: Tx cmd crc7 4'h6: Tx cmd end bit 4'h7: Rx resp start bit 4'h8: Rx resp IRQ response 4'h9: Rx resp tx bit 4'ha: Rx resp cmd idx 4'hb: Rx resp data 4'hc: Rx resp crc7 4'hd: Rx resp end bit 4'he: Cmd path wait NCC 4'hf: Wait; CMD-to-response turnaround The command FSM state is represented using 19 bits. The SDMMC_STATUS Register[7:4] has 4 bits to represent the command FSM states. Using these 4 bits, only 16 states can be represented. Thus three states cannot be represented in the SDMMC_STATUS[7:4] register. The three states that are not represented in the SDMMC_STATUS Register[7:4] are: Bit 16: Wait for CCS Bit 17: Send CCSD Bit 18: Boot Mode Due to this, while command FSM is in "Wait for CCS state" or "Send CCSD" or "Boot Mode", the Status register indicates status as 0 for the bit field [7:4]
3	RO	0x0	fifo_full FIFO is full status
2	RO	0x1	fifo_empty FIFO is empty status
1	RO	0x1	fifo_tx_watermark FIFO reached Transmit watermark level; not qualified with data transfer
0	RO	0x0	fifo_rx_watermark FIFO reached Receive watermark level; not qualified with data transfer

SDMMC_FIFOTH

Address: Operational Base + offset (0x004c)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
30:28	RW	0x0	dma_mutiple_transaction_size Burst size of multiple transaction; should be programmed same as DMA controller multiple-transaction-size SRC/DEST_MSIZE. 3'b000: 1 transfers 3'b001: 4 3'b010: 8 3'b011: 16 3'b100: 32 3'b101: 64 3'b110: 128 3'b111: 256 The unit for transfer is the H_DATA_WIDTH parameter. A single transfer (dw_dma_single assertion in case of Non DW DMA interface) would be signalled based on this value. Value should be sub-multiple of (RX_WMark + 1)* (F_DATA_WIDTH/H_DATA_WIDTH) and (FIFO_DEPTH - TX_WMark)* (F_DATA_WIDTH/ H_DATA_WIDTH) For example, if FIFO_DEPTH = 16, FDATA_WIDTH == H_DATA_WIDTH Allowed combinations for MSize and TX_WMark are: MSize = 1, TX_WMARK = 1-15 MSize = 4, TX_WMark = 8 MSize = 4, TX_WMark = 4 MSize = 4, TX_WMark = 12 MSize = 8, TX_WMark = 8 MSize = 8, TX_WMark = 4 Allowed combinations for MSize and RX_WMark are: MSize = 1, RX_WMARK = 0-14 MSize = 4, RX_WMark = 3 MSize = 4, RX_WMark = 7 MSize = 4, RX_WMark = 11 MSize = 8, RX_WMark = 7 Recommended: MSize = 8, TX_WMark = 8, RX_WMark = 7

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Bit	Attr	Reset Value	Description
27:16	RW	0x000	rx_wmark FIFO threshold watermark level when receiving data to card. When FIFO data count reaches greater than this number, DMA/FIFO request is raised. During end of packet, request is generated regardless of threshold programming in order to complete any remaining data. In non-DMA mode, when receiver FIFO threshold (RXDR) interrupt is enabled, then interrupt is generated instead of DMA request. During end of packet, interrupt is not generated if threshold programming is larger than any remaining data. It is responsibility of host to read remaining bytes on seeing Data Transfer Done interrupt. In DMA mode, at end of packet, even if remaining bytes are less than threshold, DMA request does single transfers to flush out any remaining bytes before Data Transfer Done interrupt is set. 12 bits-1 bit less than FIFO-count of status register, which is 13 bits. Limitation: RX_WMark <= FIFO_DEPTH-2 Recommended: (FIFO_DEPTH/2) - 1; (means greater than (FIFO_DEPTH/2) - 1) NOTE: In DMA mode during CCS time-out, the DMA does not generate the request at the end of packet, even if remaining bytes are less than threshold. In this case, there will be some data left in the FIFO. It is the responsibility of the application to reset the FIFO after the CCS timeout
15:12	RO	0x0	reserved
11:0	RW	0x000	tx_wmark FIFO threshold watermark level when transmitting data to card. When FIFO data count is less than or equal to this number, DMA/FIFO request is raised. If Interrupt is enabled, then interrupt occurs. During end of packet, request or interrupt is generated, regardless of threshold programming. In non-DMA mode, when transmit FIFO threshold (TXDR) interrupt is enabled, then interrupt is generated instead of DMA request. During end of packet, on last interrupt, host is responsible for filling FIFO with only required remaining bytes (not before FIFO is full or after CIU completes data transfers, because FIFO may not be empty). In DMA mode, at end of packet, if last transfer is less than burst size, DMA controller does single cycles until required bytes are transferred. 12 bits -1 bit less than FIFO-count of status register, which is 13 bits. Limitation: TX_WMark >= 1; Recommended: FIFO_DEPTH/2; (means less than or equal to FIFO_DEPTH/2)

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SDMMC_CDETECT

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RO	0x0	card_detect_n Value on card_detect_n input ports; read-only bits. 0 represents presence of card

SDMMC_WRTPRT

Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	write_protect Value on card_write_prt input port. 1 represents write protection

SDMMC_TCBCNT

Address: Operational Base + offset (0x005c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	trans_card_byte_count Number of bytes transferred by CIU unit to card. Both SDMMC_TCBCNT and SDMMC_TBBCNT share same coherency register

SDMMC_TBBCNT

Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	trans_fifo_byte_count Number of bytes transferred between Host/DMA memory and FIFO. Both SDMMC_TCBCNT and SDMMC_TBBCNT share same coherency register

SDMMC_DEBNCE

Address: Operational Base + offset (0x0064)

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:0	RW	0xffffff	debounce_count Number of host clocks (clk) used by debounce filter logic; typical debounce time is 5-25 ms

SDMMC_USRID

Address: Operational Base + offset (0x0068)

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Bit	Attr	Reset Value	Description
31:0	RW	0x07967797	usrid User identification register; value set by user. Default reset value can be picked by user while configuring core before synthesis. Can also be used as scratch pad register by user. The default value is determined by Configuration Value

SDMMC_VERID

Address: Operational Base + offset (0x006c)

Bit	Attr	Reset Value	Description
31:0	RO	0x5342270a	verid Version identification register; register value is hard-wired. Can be read by firmware to support different versions of core

SDMMC_HCON

Address: Operational Base + offset (0x0070)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	HCON Configuration Dependent. Hardware configurations selected by user before synthesizing core. Register values can be used to develop configuration-independent software drivers. [0]: CARD_TYPE 1'b0: MMC_ONLY 1'b1: SD_MMC [5:1]: NUM_CARDS - 1 [6]: H_BUS_TYPE 1'b0: APB 1'b1: AHB [9:7]: H_DATA_WIDTH 3'b000: 16 bits 3'b001: 32 bits 3'b010: 64 bits others: reserved [15:10]: H_ADDR_WIDTH 0 to 7: reserved 6'd8: 9 bits 6'd9: 10 bits … 6'd31: 32 bits 6'd32 to 63: reserved [17:16]: DMA_INTERFACE 2'b00: none 2'b01: DW_DMA 2'b10: GENERIC_DMA 2'b11: NON-DW-DMA [20:18]: GE_DMA_DATA_WIDTH 3'b000: 16 bits 3'b001: 32 bits 3'b010: 64 bits others: reserved [21]: FIFO_RAM_INSIDE 1'b0: outside 1'b1: inside [22]: IMPLEMENT_HOLD_REG 1'b0: no hold register 1'b1: hold register [23]: SET_CLK_FALSE_PATH 1'b0: no false path 1'b1: false path set [25:24]: NUM_CLK_DIVIDER-1 [26]: AREA_OPTIMIZED 1'b0: no area optimization 1'b1: Area optimization

SDMMC_UHS_REG

Address: Operational Base + offset (0x0074)

Bit	Attr	Reset Value	Description
31:17	RO	0x0	reserved
16	RW	0x0	ddr_reg DDR mode. 1'b0: non-DDR mode 1'b1: DDR mode
15:0	RO	0x0	reserved

SDMMC_RSTN

Address: Operational Base + offset (0x0078)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	card_reset Hardware reset. 1'b0: active mode 1'b1: reset

SDMMC_BMOD

Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31:11	RO	0x0	reserved
10:8	RW	0x0	PBL Programmable Burst Length. These bits indicate the maximum number of beats to be performed in one IDMAC transaction. The IDMAC will always attempt to burst as specified in PBL each time it starts a Burst transfer on the host bus. The permissible values are 1, 4, 8, 16, 32, 64, 128 and 256. This value is the mirror of MSIZE of FIFOTH register. In order to change this value, write the required value to FIFOTH register. This is an encode value as follows. 3'b000: 1 transfers 3'b001: 4 transfers 3'b010: 8 transfers 3'b011: 16 transfers 3'b100: 32 transfers 3'b101: 64 transfers 3'b110: 128 transfers 3'b111: 256 transfers Transfer unit is either 16, 32, or 64 bits, based on HDATA_WIDTH. PBL is a read-only value and is applicable only for Data Access; it does not apply to descriptor accesses
7	RW	0x0	DE IDMAC Enable. When set, the IDMAC is enabled

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Bit	Attr	Reset Value	Description
6:2	RW	0x00	DSL Descriptor Skip Length. Specifies the number of HWord/Word/Dword (depending on 16/32/64-bit bus) to skip between two unchained descriptors. This is pplicable only for dual buffer structure
1	RW	0x0	FB Fixed Burst. Controls whether the AHB Master interface performs fixed burst transfers or not. When set, the AHB will use only SINGLE, INCR4, INCR8 or INCR16 during start of normal burst transfers. When reset, the AHB will use SINGLE and INCR burst transfer operations
0	RW	0x0	SWR Software Reset. When set, the DMA Controller resets all its internal registers. It is automatically cleared after 1 clock cycle

SDMMC_PLDMND

Address: Operational Base + offset (0x0084)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	PD Poll Demand. If the OWN bit of a descriptor is not set, the FSM goes to the Suspend state. The host needs to write any value into this register for the IDMAC FSM to resume normal descriptor fetch operation. This is a write only register

SDMMC_DBADDR

Address: Operational Base + offset (0x0088)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	SDL Start of Descriptor List. Contains the base address of the First Descriptor. The LSB bits [0/1/2:0] for 16/32/64-bit bus-width) are ignored and taken as all-zero by the IDMAC internally. Hence these LSB bits are read-only

SDMMC_IDSTS

Address: Operational Base + offset (0x008c)

Bit	Attr	Reset Value	Description
31:17	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
16:13	RW	0x0	FSM DMAC FSM present state. 4'h0: DMA_IDLE 4'h1: DMA_SUSPEND 4'h2: DESC_RD 4'h3: DESC_CHK 4'h4: DMA_RD_REQ_WAI 4'h5: DMA_WR_REQ_WAI 4'h6: DMA_RD 4'h7: DMA_WR 4'h8: DESC_CLOSE
12:10	RW	0x0	EB Error Bits. Indicates the type of error that caused a Bus Error. Valid only with fatal Bus. 3'h1: Host Abort received during transmission 3'h2: Host Abort received during reception Others: Reserved
9	RW	0x0	AIS Abnormal Interrupt Summary. Logical OR of the following: SDMMC_IDSTS[2] Fatal Bus Interrupt SDMMC_IDSTS[4] DU bit Interrupt Only unmasked bits affect this bit. This is a sticky bit and must be cleared each time a corresponding bit that causes AIS to be set is cleared. Writing a 1 clears this bit
8	RW	0x0	NIS Normal Interrupt Summary. Logical OR of the following: SDMMC_IDSTS[0] Transmit Interrupt SDMMC_IDSTS[1] Receive Interrupt Only unmasked bits affect this bit. This is a sticky bit and must be cleared each time a corresponding bit that causes NIS to be set is cleared. Writing a 1 clears this bit
7:6	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
5	RW	0x0	CES Card Error Summary. Indicates the status of the transaction to/from the card; also present in SDMMC_RINTSTS. Indicates the logical OR of the following bits: EBE: End Bit Error RTO: Response Timeout/Boot Ack Timeout RCRC: Response CRC SBE: Start Bit Error DRTO: Data Read Timeout/BDS timeout DCRC: Data CRC for Receive RE: Response Error Writing a 1 clears this bit. The abort condition of the IDMAC depends on the setting of this CES bit. If the CES bit is enabled, then the IDMAC aborts on a "response error"; however, it will not abort if the CES bit is cleared
4	RW	0x0	DU Descriptor Unavailable Interrupt. This bit is set when the descriptor is unavailable due to OWN bit = 0 (DES0[31] =0). Writing a 1 clears this bit
3	RO	0x0	reserved
2	RW	0x0	FBE Fatal Bus Error Interrupt. When this bit is set, the DMA disables all its bus accesses. Writing a 1 clears this bit
1	RW	0x0	RI Receive Interrupt. Indicates the completion of data reception for a descriptor. Writing a 1 clears this bit
0	RW	0x0	TI Transmit Interrupt. Indicates that data transmission is finished for a descriptor. Writing 1 clears this bit

SDMMC_IDINTEN

Address: Operational Base + offset (0x0090)

Bit	Attr	Reset Value	Description
31:10	RO	0x0	reserved

Bit	Attr	Reset Value	Description
9	RW	0x0	AI Abnormal Interrupt Summary Enable. When set, an abnormal interrupt is enabled. This bit enables the following bits: SDMMC_IDINTEN[2] Fatal Bus Error Interrupt SDMMC_IDINTEN[4] DU Interrupt
8	RW	0x0	NI Normal Interrupt Summary Enable. When set, a normal interrupt is enabled. When reset, a normal interrupt is disabled. This bit enables the following bits: SDMMC_IDINTEN[0] Transmit Interrupt SDMMC_IDINTEN[1] Receive Interrup
7:6	RO	0x0	reserved
5	RW	0x0	CES Card Error summary Interrupt Enable. When set, it enables the Card Interrupt summary
4	RW	0x0	DU Descriptor Unavailable Interrupt. When set along with Abnormal Interrupt Summary Enable, the DU interrupt is enabled
3	RO	0x0	reserved
2	RW	0x0	FBE Fatal Bus Error Enable. When set with Abnormal Interrupt Summary Enable, the Fatal Bus Error Interrupt is enabled. When reset, Fatal Bus Error Enable Interrupt is disabled
1	RW	0x0	RI Receive Interrupt Enable. When set with Normal Interrupt Summary Enable, Receive Interrupt is enabled. When reset, Receive Interrupt is disabled
0	RW	0x0	TI Transmit Interrupt Enable. When set with Normal Interrupt Summary Enable, Transmit Interrupt is enabled. When reset, Transmit Interrupt is disabled

SDMMC_DSCADDR

Address: Operational Base + offset (0x0094)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	HDA Host Descriptor Address Pointer. Cleared on reset. Pointer updated by IDMAC during operation. This register points to the start address of the current descriptor read by the IDMAC

SDMMC_BUFADDR

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Address: Operational Base + offset (0x0098)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	HBA Host Buffer Address Pointer. Cleared on Reset. Pointer updated by IDMAC during operation. This register points to the current Data Buffer Address being accessed by the IDMAC

SDMMC_CARDTHRCTL

Address: Operational Base + offset (0x0100)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	CardRdThreshold Card Read Threshold size
15:2	RO	0x0	reserved
1	RW	0x0	BsyClrIntEn Busy Clear Interrupt generation. 1'b0: Busy Clear Interrupt disabled 1'b1: Busy Clear Interrupt enabled Note: The application can disable this feature if it does not want to wait for a Busy Clear Interrupt. For example, in a multi-card scenario, the application can switch to the other card without waiting for a busy to be completed. In such cases, the application can use the polling method to determine the status of busy. By default this feature is disabled and backward-compatible to the legacy drivers where polling is used
0	RW	0x0	CardRdThrEn Card Read Threshold Enable. 1'b0: Card Read Threshold disabled 1'b1: Card Read Threshold enabled. Host Controller initiates Read Transfer only if CardRdThreshold amount of space is available in receive FIFO

SDMMC_BACK_END_POWER

Address: Operational Base + offset (0x0104)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	back_end_power Back end power. 1'b0: Off; Reset 1'b1: Back-end Power supplied to card application

SDMMC_EMMC_DDR_REG

Address: Operational Base + offset (0x010c)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	HALF_START_BIT Control for start bit detection mechanism inside DWC_mobile_storage based on duration of start bit; each bit refers to one slot. For eMMC 4.5, start bit can be: 1'b0: Full cycle (HALF_START_BIT=0) 1'b1: Less than one full cycle (HALF_START_BIT=1) Set HALF_START_BIT=1 for eMMC 4.5 and above; set to 0 for SD applications

SDMMC_FIFO_BASE

Address: Operational Base + offset (0x0200)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	fifo_base_addr Fifo base addr

3.5 Interface Description

The interface and IOMUX setting for SDMMC, SDIO, EMMC are shown as follows.

Table 3-8 SDMMC Interface Description

Module Pin	Direction	Pad Name	IOMUX Setting
sdmmc_cclk	O	IO_SDMMC0clkout_UART4cts_TESTclk0_GPIO1D6vccio2	GRF_GPIO1D_IOMUX_H[11:8] =4'b01
sdmmc_ccmd	I/O	IO_SDMMC0cmd_UART4rts_GPIO1D7vccio2	GRF_GPIO1D_IOMUX_H[15:12]=4'b01
sdmmc_cdata0	I/O	IO_SDMMC0d0_UART2txm0_GPIO1D2vccio2	GRF_GPIO1D_IOMUX_L[11:8] =4'b01
sdmmc_cdata1	I/O	IO_SDMMC0d1_UART2rxm0_GPIO1D3vccio2	GRF_GPIO1D_IOMUX_L[15:12]=4'b01
sdmmc_cdata2	I/O	IO_SDMMC0d2_UART4rx_JTAGtck_GPIO1D4vccio2	GRF_GPIO1D_IOMUX_H[3:0] =4'b01
sdmmc_cdata3	I/O	IO_SDMMC0d3_UART4tx_JTAGtms_GPIO1D5vccio2	GRF_GPIO1D_IOMUX_H[7:4] =4'b01
sdmmc_cdetn	I	IO_SDMMC0detn_GPIO0A3pmuio1	GRF_GPIO0A_IOMUX[7:6] =2'b01

Notes: I=input, O=output, I/O=input/output, bidirectional

Table 3-9 SDIO Interface Description

Module Pin	Direction	Pad Name	IOMUX Setting
sdio_cclk	O	IO_SDMMC1clk_GPIO1C5vccio1	GRF_GPIO1C_IOMUX_H[7:4] =4'b01
sdio_ccmd	I/O	IO_SDMMC1cmd_GPIO1C4vccio1	GRF_GPIO1C_IOMUX_H[3:0] =4'b01
sdio_cdata0	I/O	IO_SDMMC1d0_GPIO1C6vccio1	GRF_GPIO1C_IOMUX_H[11:8] =4'b01
sdio_cdata1	I/O	IO_SDMMC1d1_GPIO1C7vccio1	GRF_GPIO1C_IOMUX_H[15:12]=4'b01

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Module Pin	Direction	Pad Name	IOMUX Setting
sdio_cdata2	I/O	IO_SDMMC1d2_GPIO1D0vccio1	GRF_GPIO1D_IOMUX_L[3:0] =4'b01
sdio_cdata3	I/O	IO_SDMMC1d3_GPIO1D1vccio1	GRF_GPIO1D_IOMUX_L[7:4] =4'b01

Notes: I=input, O=output, I/O=input/output, bidirectional

Table 3-10 EMMC Interface Description

Module Pin	Direction	Pad Name	IOMUX Setting
emmc_cclk	O	IO_FLASHrdy_EMMCclkout_SFCclk_GPIO1B1vccio0	GRF_GPIO1B_IOMUX_L[7:4] =4'b10
emmc_ccmd	I/O	IO_FLASHdqs_EMMCcmd_GPIO1B2vccio0	GRF_GPIO1B_IOMUX_L[11:8] =4'b10
emmc_cdata0	I/O	IO_FLASHd0_EMMCd0_SFCsio0_GPIO1A0vccio0	GRF_GPIO1A_IOMUX_L[3:0] =4'b10
emmc_cdata1	I/O	IO_FLASHd1_EMMCd1_SFCsio1_GPIO1A1vccio0	GRF_GPIO1A_IOMUX_L[7:4] =4'b10
emmc_cdata2	I/O	IO_FLASHd2_EMMCd2_SFCsio2_GPIO1A2vccio0	GRF_GPIO1A_IOMUX_L[11:8] =4'b10
emmc_cdata3	I/O	IO_FLASHd3_EMMCd3_SFCsio3_GPIO1A3vccio0	GRF_GPIO1A_IOMUX_L[15:12]=4'b10
emmc_cdata4	I/O	IO_FLASHd4_EMMCd4_SFCcsn0_GPIO1A4vccio0	GRF_GPIO1A_IOMUX_H[3:0] =4'b10
emmc_cdata5	I/O	IO_FLASHd5_EMMCd5_GPIO1A5vccio0	GRF_GPIO1A_IOMUX_H[7:4] =4'b10
emmc_cdata6	I/O	IO_FLASHd6_EMMCd6_GPIO1A6vccio0	GRF_GPIO1A_IOMUX_H[11:8] =4'b10
emmc_cdata7	I/O	IO_FLASHd7_EMMCd7_GPIO1A7vccio0	GRF_GPIO1A_IOMUX_H[15:12]=4'b10
emmc_pwren	O	IO_FLASHcs0_EMMCpwren_GPIO1B0vccio0	GRF_GPIO1B_IOMUX_L[3:0] =4'b10
emmc_rstn	O	IO_FLASHale_EMMCrstn_GPIO1B3vccio0	GRF_GPIO1B_IOMUX_L[15:12]=4'b10

Notes: I=input, O=output, I/O=input/output, bidirectional

3.6 Application Notes

3.6.1 Card-Detect and Write-Protect Mechanism

Following figure illustrates how the SD/MMC card detection and write-protect signals are connected. Most of the SD/MMC sockets have card-detect pins. When no card is present, card_detect_n is 1 due to the pull-up. When the card is inserted, the card-detect pin is shorted to ground, which makes card_detect_n go to 0. Similarly in SD cards, when the write-protect switch is toward the left, it shorts the write_protect port to ground.

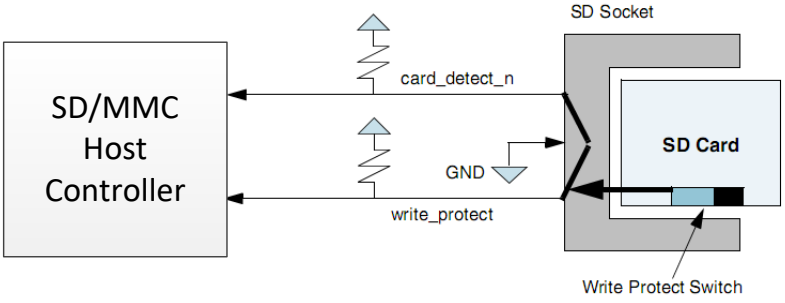


Fig. 3-9 SD/MMC Card-Detect and Write-Protect

3.6.2 SD/MMC Termination Requirement

Following Figure illustrates the SD/MMC termination requirements, which is required to pull up ccmd and cdata lines on the device bus. The recommended specification for pull-up on the ccmd line (Rcmd) is 4.7K - 100K for MMC, and 10K - 100K for an SD. The recommended pull-up on the cdata line (Rdat) is 50K - 100K.

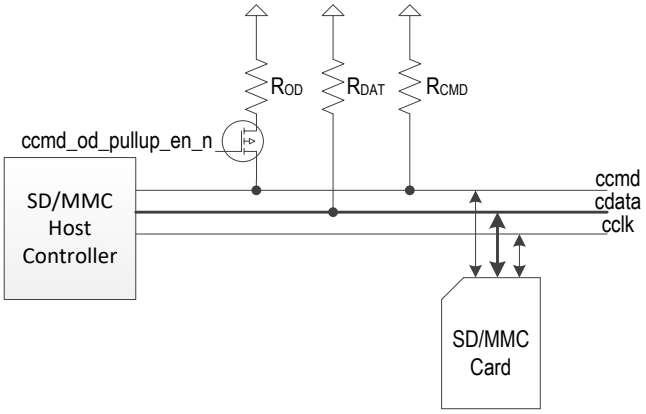


Fig. 3-10 SD/MMC Card Termination

Rcmd and Rod Calculation

The SD/MMC card enumeration happens at a very low frequency – 100-400KHz. Since the MMC bus is a shared bus between multiple cards, during enumeration open-drive mode is used to avoid bus conflict. Cards that drive 0 win over cards that drive "z". The pull-up in the command line pulls the bus to 1 when all cards drive "z". During normal data transfer, the host chooses only one card and the card driver switches to push-pull mode.

For example, if enumeration is done at 400KHz and the total bus capacitance is 200 pf, the pull-up needed during enumeration is:

2.2 RC = rise-time = 1/400KHz

R = 1/(2.2 * C * 100KHz)

= 1/(2.2 x 200 x 10**-12 x 400 x 10**3)

= 1/(17.6 x 10**-5)

= 5.68K

The ROD and RCMD should be adjusted in such a way that the effective pull-up is at the maximum 5.68K during enumeration. If there are only a few cards in the bus, a fixed RCMD resister is sufficient and there is no need for an additional ROD pull-up during enumeration. You should also ensure the effective pull-up will not violate the Iol rating of the drivers.

In SD mode, since each card has a separate bus, the capacitance is less, typically in the order of 20-30pf (host capacitance + card capacitance + trace + socket capacitance). For example, if enumeration is done at 400KHz and the total bus capacitance is 20pf, the pull-up needed during enumeration is:

2.2 RC = rise-time = 1/400KHz

R = 1/(2.2 * C * 100KHz)

= 1/(2.2 x 20 x 10**-12 x 400 x 10**3)

= 1/(1.76 x 10**-5)

= 56.8K

Therefore, a fixed 56.8K permanent Rcmd is sufficient in SD mode to enumerate the cards. The driver of the SD/MMC on the "command" port needs to be only a push-pull driver. During enumeration, the SD/MMC emulates an open-drain driver by driving only a 0 or a"z" by controlling the ccmd_out and ccmd_out_en signals.

3.6.3 Software/Hardware Restriction

Before issuing a new data transfer command, the software should ensure that the card is not busy due to any previous data transfer command. Before changing the card clock frequency, the software must ensure that there are no data or command transfers in progress.

If the card is enumerated in SDR50, or DDR50 mode, then the application must program the

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use_hold_reg bit[29] in the SDMMC_CMD register to 1'b0 (phase shift of cclk_in_drv = 0) or 1'b1 (phase shift of cclk_in_drv>0). If the card is enumerated in SDR12 or SDR25 mode, the application must program the use_hold_reg bit[29] in the SDMMC_CMD register to 1'b1. This programming should be done for all data transfer commands and non-data commands that are sent to the card. When the use_hold_reg bit is programmed to 1'b0, the Host Controller bypasses the Hold Registers in the transmit path. The value of this bit should not be changed when a Command or Data Transfer is in progress. For more details on using use_hold_reg and the implementation requirements for meeting the Card input hold time, refer to "Recommended Usage" in following table.

Table 3-11 Recommended Usage of use_hold_reg

No.	Speed Mode	use_hold_reg	cclk_in (MHz)	clk_in_drv (MHz)	clk_divider	Phase shift
1	SDR104	1'b0	200	200	0	0
2	SDR104	1'b1	200	200	0	Tunable> 0
3	SDR50	1'b0	100	100	0	0
4	SDR50	1'b1	100	100	0	Tunable> 0
5	DDR50 (8bit)	1'b0	100	100	1	0
6	DDR50 (8bit)	1'b1	100	100	1	Tunable> 0
7	DDR50 (4bit)	1'b0	50	50	0	0
8	DDR50 (4bit)	1'b1	50	50	0	Tunable> 0
9	SDR25	1'b1	50	50	0	Tunable> 0
10	SDR12	1'b1	50	50	1	Tunable> 0

To avoid glitches in the card clock outputs, the software should use the following steps when changing the card clock frequency:

1) Before disable the clocks, ensure that the card is not busy due to any previous data command. To determine this, check for 0 in bit9 of STATUS register.

2) Update the Clock Enable register to disable all clocks. To ensure completion of any previous command before this update, send a command to the CIU to update the clock registers by setting:

- start_cmd bit
- "update clock registers only" bits
- "wait_previous data complete" bit

Wait for the CIU to take the command by polling for 0 on the start_cmd bit.

3) Set the start_cmd bit to update the Clock Divider and/or Clock Source registers, and send a command to the CIU in order to update the clock registers; wait for the CIU to take the command.

4) Set start_cmd to update the Clock Enable register in order to enable the required clocks and send a command to the CIU to update the clock registers; wait for the CIU to take the command.

In non-DMA mode, while reading from a card, the Data Transfer Over (SDMMC_RINTSTS[3]) interrupt occurs as soon as the data transfer from the card is over. There still could be some data left in the FIFO, and the RX_WMark interrupt may or may not occur, depending on the remaining bytes in the FIFO. Software should read any remaining bytes upon seeing the Data Transfer Over (DTO) interrupt. While using the external DMA interface for reading from a card, the DTO interrupt occurs only after all the data is flushed to memory by the DMA interface unit.

While writing to a card in external DMA mode, if an undefined-length transfer is selected by setting the Byte Count Register to 0, the DMA logic will likely request more data than it will send to the card, since it has no way of knowing at which point the software will stop the transfer. The DMA request stops as soon as the DTO is set by the CIU.

If the software issues a controller_reset command by setting control register bit[0] to 1, all the CIU state machines are reset; the FIFO is not cleared. The DMA sends all remaining

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bytes to the host. In addition to a card-reset, if a FIFO reset is also issued, then:

- Any pending DMA transfer on the bus completes correctly
- DMA data read is ignored
- Write data is unknown(x)

Additionally, if dma_reset is also issued, any pending DMA transfer is abruptly terminated. When the DMA is used, the DMA controller channel should also be reset and reprogrammed. If any of the previous data commands do not properly terminate, then the software should issue the FIFO reset in order to remove any residual data, if any, in the FIFO. After asserting the FIFO reset, you should wait until this bit is cleared.

One data-transfer requirement between the FIFO and host is that the number of transfers should be a multiple of the FIFO data width (32bits). For example, you want to write only 15 bytes to an SD/MMC card (SDMMC_BYTCNT), the host should write 16 bytes to the FIFO or program the DMA to do 16-byte transfers. The software can still program the Byte Count register to only 15, at which point only 15 bytes will be transferred to the card. Similarly, when 15 bytes are read from a card, the host should still read all 16 bytes from the FIFO. It is recommended that you not change the FIFO threshold register in the middle of data transfers.

3.6.4 Programming Sequence

1. Initialization

Following figure illustrates the initialization flow.

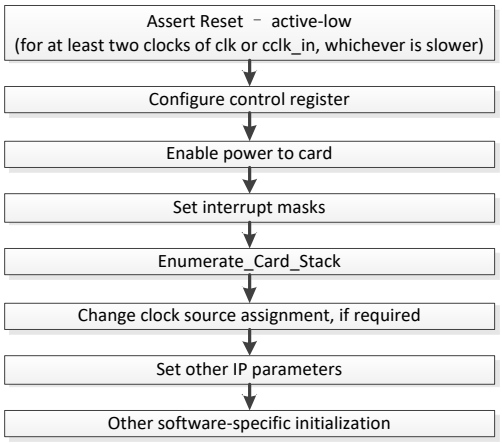


Fig. 3-11 Host Controller Initialization Sequence

Once the power and clocks are stable, reset_n should be asserted(active-low) for at least two clocks of clk or cclk_in, whichever is slower. The reset initializes the registers, ports, FIFO-pointers, DMA interface controls, and state-machines in the design. After power-on reset, the software should do the following:

1) Configure control register – For MMC mode, enable the open-drain pullup by setting enable_OD_pullup(bit24) in the control register.
2) Enable power to cards – Before enabling the power, confirm that the voltage setting to the voltage regulators is correct. Enable power to the connected cards by setting the corresponding bit to 1 in the Power Enable register. Wait for the power ramp-up time.
3) Set masks for interrupts by clearing appropriate bits in the Interrupt Mask register. Set the global int_enable bit of the Control register. It is recommended that you write 0xffff_ffff to the Raw Interrupt register in order to clear any pending interrupts before setting the int_enable bit.
4) Enumerate card stack – Each card is enumerated according to card type; for details, refer to "Enumerated Card Stack". For enumeration, you should restrict the clock frequency to 400KHz.
5) Changing clock source assignment – set the card frequency using the clock-divider and clock-source registers; for details, refer to "Clock Programming". MMC cards operate at a

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maximum of 20MHz (at maximum of 52MHz in high-speed mode). SD mode operates at a maximum of 25MHz (at maximum of 50MHz in high-speed mode).

6) Set other parameters, which normally do not need to be changed with every command, with a typical value such as timeout values in cclk_out according to SD/MMC specifications.

- ResponseTimeOut = 0x64
- DataTimeOut = highest of one of the following:
- (10*((TAAC*Fop)+(100*NSAC))
- Host FIFO read/write latency from FIFO empty/full
- Set the debounce value to 25ms(default:0x0fffff) in host clock cycle units in the DEBNCE register.
- FIFO threshold value in bytes in the SDMMC_FIFOTH register.

2. Enumerated Card Stack

The card stack does the following:

- Enumerates all connected cards
- Sets the RCA for the connected cards
- Reads card-specific information
- Stores card-specific information locally

Enumeration depends on the operating mode of the SD/MMC card; the card type is first identified and the appropriate card enumeration routine is called.

1) Check if the card is connected.
2) Clear the card type register to set the card width as a single bit. For the given card number, clear the corresponding bits in the card_type register. Clear the register bit for a 1-bit, 4-bit bus width. For example, for card number=1, clear bit 0 and bit 16 of the card_type register.
3) Set clock frequency to FOD=400KHz, maximum – Program clock divider0 (bits 0-7 in the CLKDIV register) value to one-half of the cclk_in frequency divided by 400KHz. For example, if cclk_in is 20MHz, then the value is 20, 000/(2*400)=25.
4) Identify the card type; that is, SD, MMC, or SDIO.
   a. Send CMD5 first. If a response is received, then the card is SDIO
   b. If not, send CMD8 with the following Argument
      Bit[31:12] = 20'h0 //reserved bits
      Bit[11:8] = 4'b0001 //VHS value
      Bit[7:0] = 8'b10101010 //Preferred Check Pattern by SD2.0
   c. If Response is received the card supports High Capacity SD2.0 then send ACMD41 with the following Argument
      Bit[31] = 1'b0; //Reserved bits
      Bit[30] = 1'b1; //High Capacity Status
      Bit[29:24] = 6'h0; //Reserved bits
      Bit[23:0] = Supported Voltage Range
   d. If Response is received for ACMD41 then the card is SD. Otherwise the card is MMC.
   e. If response is not received for initial CMD8 then card does not support High Capacity SD2.0, then issue CMD0 followed by ACMD41 with the following Argument
      Bit[31] = 1'b0; //Reserved bits
      Bit[30] = 1'b0; //High Capacity Status
      Bit[29:24] = 6'h0; //Reserved bits
      Bit[23:0] = Supported Voltage Range
5) Enumerate the card according to the card type.

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6) Use a clock source with a frequency = Fod (that is, 400KHz) and use the following enumeration command sequence:

- SD card – Send CMD0, CMD8, ACMD41, CMD2, CMD3.
- MMC – Send CMD0, CMD1, CMD2, CMD3.

3. Power Control

You can implement power control using the following registers, along with external circuitry:

- Control register bits card_voltage_a and card_voltage_b – Status of these bits is reflected at the IO pins. The bits can be used to generate or control the supply voltage that the memory cards require.
- Power enable register – Control power to individual cards.

Programming these two register depends on the implemented external circuitry. While turning on or off the power enable, you should confirm that power supply settings are correct. Power to all cards usually should be disabled while switching off the power.

4. Clock Programming

The Host Controller supports one clock sources. The clock to an individual card can be enabled or disabled. Registers that support this are:

- SDMMC_CLKDIV – Programs individual clock source frequency. SDMMC_CLKDIV limited to 0 or 1 is recommended.
- SDMMC_CLKSRC – Assign clock source for each card.
- SDMMC_CLKENA – Enables or disables clock for individual card and enables low-power mode, which automatically stops the clock to a card when the card is idle for more than 8 clocks.

The Host Controller loads each of these registers only when the start_cmd bit and the Update_clk_regs_only bit in the SDMMC_CMD register are set. When a command is successfully loaded, the Host Controller clears this bit, unless the Host Controller already has another command in the queue, at which point it gives an HLE(Hardware Locked Error). Software should look for the start_cmd and the Update_clk_regs_only bits, and should also set the wait_prvdata_complete bit to ensure that clock parameters do not change during data transfer. Note that even though start_cmd is set for updating clock registers, the Host Controller does not raise a command_done signal upon command completion.

The following shows how to program these registers:

1) Confirm that no card is engaged in any transaction; if there is a transaction, wait until it finishes.
2) Stop all clocks by writing xxxx0000 to the SDMMC_CLKENA register. Set the start_cmd, Update_clk_regs_only, and wait_prvdata_complete bits in the SDMMC_CMD register. Wait until start_cmd is cleared or an HLE is set; in case of an HLE, repeat the command.
3) Program the SDMMC_CLKDIV and SDMMC_CLKSRC registers, as required. Set the start_cmd, Update_clk_regs_only, and wait_prvdata_complete bits in the SDMMC_CMD register. Wait until start_cmd is cleared or an HLE is set; in case of an HLE, repeat the command.
4) Re-enable all clocks by programming the SDMMC_CLKENA register. Set the start_cmd, Update_clk_regs_only, and wait_prvdata_complete bits in the SDMMC_CMD register. Wait until start_cmd is cleared or an HLE is set; in case of an HLE, repeat the command.

5. No-Data Command With or Without Response Sequence

To send any non-data command, the software needs to program the SDMMC_CMD register @0x2C and the SDMMC_CMDARG register @0x28 with appropriate parameters. Using these two registers, the Host Controller forms the command and sends it to the command bus. The Host Controller reflects the errors in the command response through the error bits of the SDMMC_RINTSTS register.

When a response is received – either erroneous or valid – the Host Controller sets the command_done bit in the SDMMC_RINTSTS register. A short response is copied in Response

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Register0, while along response is copied to all four response registers @0x30, 0x34, 0x38, and 0x3C. The Response3 register bit 31 represents the MSB, and the Response0 register bit 0 represents the LSB of a long response.
For basic commands or non-data commands, follow these steps:

1) Program the Command register @0x28 with the appropriate command argument parameter.
2) Program the Command register @0x2C with the settings in following table.

Table 3-12 Command Settings for No-Data Command

Parameter	Value	Description
Default		
start_cmd	1	-
use_hold_reg	1/0	Choose value based on speed mode being used;ref to "use_hold_reg" on SDMMC_CMD register
update_clk_regs_only	0	No clock parameters update command
data_expected	0	No data command
card number	0	Actual card number(one controller only connect one card, the num is No. 0)
cmd_index	command-index	-
send_initialization	0	Can be 1, but only for card reset commands, such as CMD0
stop_abort_cmd	0	Can be 1 for commands to stop data transfer, such as CMD12
response_length	0	Can be 1 for R2(long) response
response_expect	1	Can be 0 for commands with no response; for example, CMD0, CMD4, CMD15, and so on
User-selectable		
wait_prvdata_complete	1	Before sending command on command line, host should wait for completion of any data command in process, if any (recommended to always set this bit, unless the current command is to query status or stop data transfer when transfer is in progress)
check_response_crc	1	If host should crosscheck CRC of response received

1) Wait for command acceptance by host. The following happens when the command is loaded into the Host Controller:
   - Host Controller accepts the command for execution and clears the start_cmd bit in the SDMMC_CMD register, unless one command is in process, at which point the Host Controller can load and keep the second command in the buffer.
   - If the Host Controller is unable to load the command – that is, a command is already in progress, a second command is in the buffer, and a third command is attempted – then it generates an HLE (hardware-locked error).

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2) Check if there is an HLE.
3) Wait for command execution to complete. After receiving either a response from a card or response timeout, the Host Controller sets the command_done bit in the SDMMC_RINTSTS register. Software can either poll for this bit or respond to a generated interrupt.
4) Check if response_timeout error, response_CRC error, or response error is set. This can be done either by responding to an interrupt raised by these errors or by polling bits 1, 6, and 8 from the SDMMC_RINTSTS register @0x44. If no response error is received, then the response is valid. If required, the software can copy the response from the response registers @0x30-0x3C.

Software should not modify clock parameters while a command is being executed.

6. Data Transfer Commands

Data transfer commands transfer data between the memory card and the Host Controller. To send a data command, the Host Controller needs a command argument, total data size, and block size. Software can receive or send data through the FIFO.

Before a data transfer command, software should confirm that the card is not busy and is in a transfer state, which can be done using the CMD13 and CMD7 commands, respectively.

For the data transfer commands, it is important that the same bus width that is programmed in the card should be set in the card type register @0x18.

The Host Controller generates an interrupt for different conditions during data transfer, which are reflected in the SDMMC_RINTSTS register @0x44 as:

1) Data_Transfer_Over (bit 3) – When data transfer is over or terminated. If there is a response timeout error, then the Host Controller does not attempt any data transfer and the "Data Transfer Over" bit is never set.
2) Transmit_FIFO_Data_request (bit 4) – FIFO threshold for transmitting data was reached; software is expected to write data, if available, in FIFO.
3) Receive_FIFO_Data_request (bit 5) – FIFO threshold for receiving data was reached; software is expected to read data from FIFO.
4) Data starvation by Host timeout (bit 10) – FIFO is empty during transmission or is full during reception. Unless software writes data for empty condition or reads data for full condition, the Host Controller cannot continue with data transfer. The clock to the card has been stopped.
5) Data read timeout error (bit 9) – Card has not sent data within the timeout period.
6) Data CRC error (bit 7) – CRC error occurred during data reception.
7) Start bit error (bit 13) – Start bit was not received during data reception.
8) End bit error (bit 15) – End bit was not received during data reception or for a write operation; a CRC error is indicated by the card.

Conditions 6, 7, and 8 indicate that the received data may have errors. If there was a response timeout, then no data transfer occurred.

7. Single-Block or Multiple-Block Read

Steps involved in a single-block or multiple-block read are:

1) Write the data size in bytes in the SDMMC_BYTCNT register @0x20.
2) Write the block size in bytes in the SDMMC_BLKSIZ register @0x1C. The Host Controller expects data from the card in blocks of size SDMMC_BLKSIZ each.
3) Program the SDMMC_CMDARG register @0x28 with the data address of the beginning of a data read.
4) Program the Command register with the parameters listed in following table. For SD and MMC cards, use CMD17 for a single-block read and CMD18 for a multiple-block read. For SDIO cards, use CMD53 for both single-block and multiple-block transfers.

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Table 3-13 Command Setting for Single or Multiple-Block Read

Parameter	Value	Description
Default		
start_cmd	1	-
use_hold_reg	1/0	Choose value based on speed mode being used;ref to "use_hold_reg" on SDMMC_CMD register
update_clk_regs_only	0	No clock parameters update command
card number	0	Actual card number(one controller only connect one card, the num is No.0)
send_initialization	0	Can be 1, but only for card reset commands, such as CMD0
stop_abort_cmd	0	Can be 1 for commands to stop data transfer, such as CMD12
send_auto_stop	0/1	-
transfer_mode	0	Block transfer
read_write	0	Read from card
data_expected	1	Data command
response_length	0	Can be 1 for R2(long) response
response_expect	1	Can be 0 for commands with no response; for example, CMD0, CMD4, CMD15, and so on
User-selectable		
cmd_index	command-index	-
wait_prvdata_complete	1	0: Sends command immediately 1: Sends command after previous data transfer ends
check_response_crc	1	0: Host Controller should not check response CRC 1: Host Controller should check response CRC

After writing to the SDMMC_CMD register, the Host Controller starts executing the command; when the command is sent to the bus, the command_done interrupt is generated.

- Software should look for data error interrupts; that is, bits 7, 9, 13, and 15 of the SDMMC_RINTSTS register. If required, software can terminate the data transfer by sending a STOP command.
- Software should look for Receive_FIFO_Data_request and/or data starvation by host timeout conditions. In both cases, the software should read data from the FIFO and make space in the FIFO for receiving more data.
- When a Data_Transfer_Over interrupt is received, the software should read the remaining data from the FIFO.

8. Single-Block or Multiple-Block Write

Steps involved in a single-block or multiple-block write are:

1) Write the data size in bytes in the BYTCNT register @0x20.

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2) Write the block size in bytes in the SDMMC_BLKSIZ register @0x1C; the Host Controller sends data in blocks of size SDMMC_BLKSIZ each.
3) Program SDMMC_CMDARG register @0x28 with the data address to which data should be written.
4) Write data in the FIFO; it is usually best to start filling data the full depth of the FIFO.
5) Program the Command register with the parameters listed in following table.

Table 3-14 Command Settings for Single or Multiple-Block Write

Parameter	Value	Description
Default		
start_cmd	1	-
use_hold_reg	1/0	Choose value based on speed mode being used;ref to "use_hold_reg" on SDMMC_CMD register
update_clk_regs_only	0	No clock parameters update command
card number	0	Actual card number(one controller only connect one card, the num is No. 0)
send_initialization	0	Can be 1, but only for card reset commands, such as CMD0
stop_abort_cmd	0	Can be 1 for commands to stop data transfer, such as CMD12
send_auto_stop	0/1	-
transfer_mode	0	Block transfer
read_write	1	Write to card
data_expected	1	Data command
response_length	0	Can be 1 for R2(long) response
response_expect	1	Can be 0 for commands with no response; for example, CMD0, CMD4, CMD15, and so on
User-selectable		
cmd_index	command-index	-
wait_prvdata_complete	1	0: Sends command immediately 1: Sends command after previous data transfer ends
check_response_crc	1	0: Host Controller should not check response CRC 1: Host Controller should check response CRC

After writing to the SDMMC_CMD register, Host Controller starts executing a command; when the command is sent to the bus, a command_done interrupt is generated.

- Software should look for data error interrupts; that is, for bits 7, 9, and 15 of the SDMMC_RINTSTS register. If required, software can terminate the data transfer by sending the STOP command.
- Software should look for Transmit_FIFO_Data_Request and/or timeout conditions from data starvation by the host. In both cases, the software should write data into the FIFO.
- When a Data_Transfer_Over interrupt is received, the data command is over. For an open-ended block transfer, if the byte count is 0, the software must send the STOP

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command. If the byte count is not 0, then upon completion of a transfer of a given number of bytes, the Host Controller should send the STOP command, if necessary. Completion of the AUTO-STOP command is reflected by the Auto_command_done interrupt – bit 14 of the SDMMC_RINTSTS register. A response to AUTO_STOP is stored in SDMMC_RESP1 @0x34.

9. Stream Read

A stream read is like the block read mentioned in "Single-Block or Multiple-Block Read", except for the following bits in the Command register:

transfer_mode = 1; //Stream transfer
cmd_index = CMD20;

A stream transfer is allowed for only a single-bit bus width.

10. Stream Write

A stream write is exactly like the block write mentioned in "Single-Block or Multiple-Block Write", except for the following bits in the Command register:

transfer_mode = 1;//Stream transfer
cmd_index = CMD11;

In a stream transfer, if the byte count is 0, then the software must send the STOP command. If the byte count is not 0, then when a given number of bytes completes a transfer, the Host Controller sends the STOP command. Completion of this AUTO_STOP command is reflected by the Auto_command_done interrupt. A response to an AUTO_STOP is stored in the SDMMC_RESP1 register@0x34.

A stream transfer is allowed for only a single-bit bus width.

11. Packed Commands

In order to reduce overhead, read and write commands can be packed in groups of commands—either all read or all write—that transfer the data for all commands in the group in one transfer on the bus.

Packed commands can be of two types:

- Packed Write: CMD23 →CMD25
- Packed Read: CMD23 → CMD25 → CMD23 → CMD18

Packed commands are put in packets by the application software and are transparent to the core.

12. Sending Stop or Abort in Middle of Transfer

The STOP command can terminate a data transfer between a memory card and the Controller, while the ABORT command can terminate an I/O data transfer for only the SDIO_IOONLY and SDIO_COMBO cards.

- Send STOP command – Can be sent on the command line while a data transfer is in progress; this command can be sent at any time during a data transfer.

You can also use an additional setting for this command in order to set the Command register bits (5-0) to CMD12 and set bit 14 (stop_abort_cmd) to 1. If stop_abort_cmd is not set to 1, the Controller does not know that the user stopped a data transfer. Reset bit 13 of the Command register (wait_prvdata_complete) to 0 in order to make the Controller send the command at once, even though there is a data transfer in progress.

- Send ABORT command – Can be used with only an SDIO_IOONLY or SDIO_COMBO card. To abort the function that is transferring data, program the function number in ASx bits (CCCR register of card, address 0x06, bits (0-2) using CMD52.

13. Read_Wait Sequence

Read_wait is used with only the SDIO card and can temporarily stall the data transfer—either from function or memory—and allow the host to send commands to any function within the SDIO device. The host can stall this transfer for as long as required. The Host Controller provides the facility to signal this stall transfer to the card. The steps for doing this are:

1) Check if the card supports the read_wait facility; read SRW (bit 2) of the CCCR register @0x08. If this bit is 1, then all functions in the card support the read_wait facility. Use CMD52 to read this bit.

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2) If the card supports the read_wait signal, then assert it by setting the read_wait (bit 6) in the SDMMC_CTRL register @0x00.
3) Clear the read_wait bit in the SDMMC_CTRL register.

14. Controller/DMA/FIFO Reset Usage

- Controller reset – Resets the controller by setting the controller_reset bit (bit 0) in the SDMMC_CTRL register; this resets the CIU and state machines, and also resets the BIU-to-CIU interface. Since this reset bit is self-clearing, after issuing the reset, wait until this bit is cleared.
- FIFO reset - Resets the FIFO by setting the fifo_reset bit (bit 1) in the SDMMC_CTRL register; this resets the FIFO pointers and counters of the FIFO. Since this reset bit is self-clearing, after issuing the reset, wait until this bit is cleared.

In external DMA transfer mode, even when the FIFO pointers are reset, if there is a DMA transfer in progress, it could push or pop data to or from the FIFO; the DMA itself completes correctly. In order to clear the FIFO, the software should issue an additional FIFO reset and clear any FIFO underrun or overrun errors in the SDMMC_RAWINTS register caused by the DMA transfers after the FIFO was reset.

15. Card Read Threshold

When an application needs to perform a Single or Multiple Block Read command, the application must program the SDMMC_CARDTHRCTL register with the appropriate Card Read Threshold size (CardRdThreshold) and set the Card Read Threshold Enable (CardRdThrEnable) bit to 1'b1. This additional programming ensures that the Host controller sends a Read Command only if there is space equal to the CardRDThreshold available in the Rx FIFO. This in turn ensures that the card clock is not stopped in the middle a block of data being transmitted from the card. The Card Read Threshold can be set to the block size of the transfer, which guarantees that there is a minimum of one block size of space in the RxFIFO before the controller enables the card clock. The Card Read Threshold is required when the Round Trip Delay is greater than 0.5cclk_in period.

16. Error Handling

The Host Controller implements error checking; errors are reflected in the SDMMC_RAWINTS register@0x44 and can be communicated to the software through an interrupt, or the software can poll for these bits. Upon power-on, interrupts are disabled (int_enable in the SDMMC_CTRL register is 0), and all the interrupts are masked (bits 0-31 of the SDMMC_INTMASK register; default is 0).

Error handling:

- Response and data timeout errors – For response timeout, software can retry the command. For data timeout, the Host Controller has not received the data start bit – either for the first block or the intermediate block – within the timeout period, so software can either retry the whole data transfer again or retry from a specified block onwards. By reading the contents of the SDMMC_TCBCNT later, the software can decide how many bytes remain to be copied.
- Response errors – Set when an error is received during response reception. In this case, the response that copied in the response registers is invalid. Software can retry the command.
- Data errors – Set when error in data reception are observed; for example, data CRC, start bit not found, end bit not found, and so on. These errors could be set for any block-first block, intermediate block, or last block. On receipt of an error, the software can issue a STOP or ABORT command and retry the command for either whole data or partial data.
- Hardware locked error – Set when the Host Controller cannot load a command issued by software. When software sets the start_cmd bit in the SDMMC_CMD register, the Host

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Controller tries to load the command. If the command buffer is already filled with a command, this error is raised. The software then has to reload the command.

- FIFO underrun/overrun error – If the FIFO is full and software tries to write data in the FIFO, then an overrun error is set. Conversely, if the FIFO is empty and the software tries to read data from the FIFO, an underrun error is set. Before reading or writing data in the FIFO, the software should read the fifo_empty or fifo_full bits in the Status register.
- Data starvation by host timeout – Raised when the Host Controller is waiting for software intervention to transfer the data to or from the FIFO, but the software does not transfer within the stipulated timeout period. Under this condition and when a read transfer is in process, the software should read data from the FIFO and create space for further data reception. When a transmit operation is in process, the software should fill data in the FIFO in order to start transferring data to the card.
- CRC Error on Command – If a CRC error is detected for a command, the CE-ATA device does not send a response, and a response timeout is expected from the Host Controller. The ATA layer is notified that an MMC transport layer error occurred.

Notes: During a multiple-block data transfer, if a negative CRC status is received from the device, the data path signals a data CRC error to the BIU by setting the data CRC error bit in the SDMMC_RINTSTS register. It then continues further data transmission until all the bytes are transmitted.

3.6.5 Voltage Switching

The Host Controller supports SD 3.0 Ultra High Speed (UHS-1) and is capable of voltage switching in SD-mode, which can be applied to SD High-Capacity (SDHC) and SD Extended Capacity (SDXC) cards. UHS-1 supports only 4-bit mode.
However, whether the IO voltage of 1.8v supported or not is depended on the SoC design.
SD 3.0 UHS-1 supports the following transfer speed modes for UHS-50 and/or UHS-104 cards:

- DS – default-speed up to 25MHz, 3.3V signaling
- HS – high-speed up to 50MHz, 3.3V signaling
- SDR12 – SDR up to SDR 25MHz, 1.8V signaling
- SDR25 – SDR up to 50MHz, 1.8V signaling
- SDR50 – SDR up to 100MHz, 1.8V signaling
- DDR50 – DDR up to 50MHz, 1.8V signaling

Voltage selection can be done in only SD mode. The first CMD0 selects the bus mode-either SD mode or SPI mode. The card must be in SD mode in order for 1.8V signaling mode to apply, during which time the card cannot be switched to SPI mode or 3.3V signaling without a power cycle.
If the System BIOS in an embedded system already knows that it is connected to an SD 3.0 card, then the driver programs the Controller to initiate ACMD41. The software knows from the response of ACMD41 whether or not the card supports voltage switching to 1.8V.

- If bit 32 of ACMD41 response is 1'b1: card supports voltage switching and next command-CMD11-invokes voltage switching sequence. After CMD11 is started, the software must program the IO voltage selection register based on the soc architecture.
- If bit 32 of ACMD41 response is 1'b0: card does not support voltage switching and CMD11 should not be started.

If the card and host controller accept voltage switching, then they support UHS-1 modes of data transfer. After the voltage switch to 1.8V, SDR12 is the default speed.
Since the UHS-1 can be used in only 4-bit mode, the software must start ACMD6 and change the card data width to 4-bit mode; ACMD6 is driven in any of the UHS-1 speeds. If the host wants to select the DDR mode of data transfer, then the software must program the SDMMC_DDR_REG register in the CSR space with the appropriate card number.
To choose from any of the SDR or DDR modes, appropriate values should be programmed in

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the SDMMC_CLKDIV register.

1. Voltage Switch Operation

The Voltage Switch operation must be performed in SD mode only.

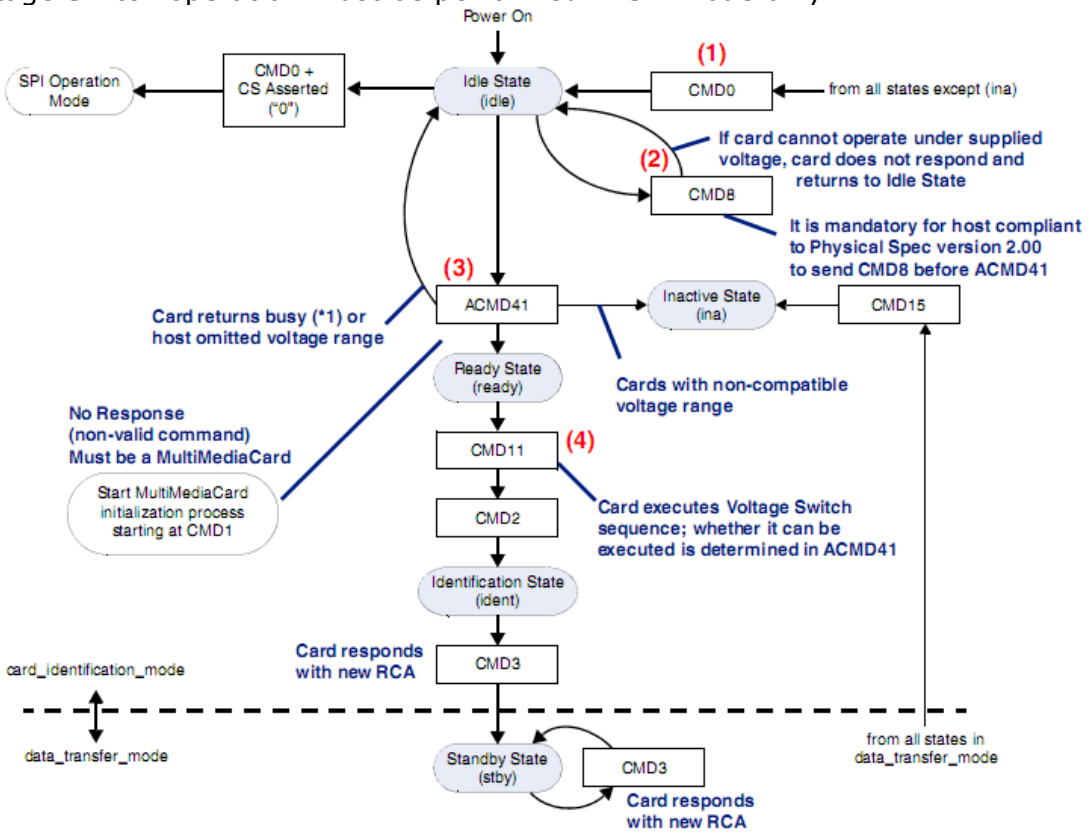


Fig. 3-12 Voltage Switching Command Flow Diagram

The following outlines the steps for the voltage switch programming sequence

1) Software Driver starts CMD0, which selects the bus mode as SD.
2) After the bus is in SD card mode, CMD8 is started in order to verify if the card is compatible with the SD Memory Card Specification, Version 2. 00. CMD8 determines if the card is capable of working within the host supply voltage specified in the VHS (19:16) field of the CMD; the card supports the current host voltage if a response to CMD8 is received.
3) ACMD 41 is started. The response to this command informs the software if the card supports voltage switching; bits 38, 36, and 32 are checked by the card argument of ACMD41; refer to following figure.

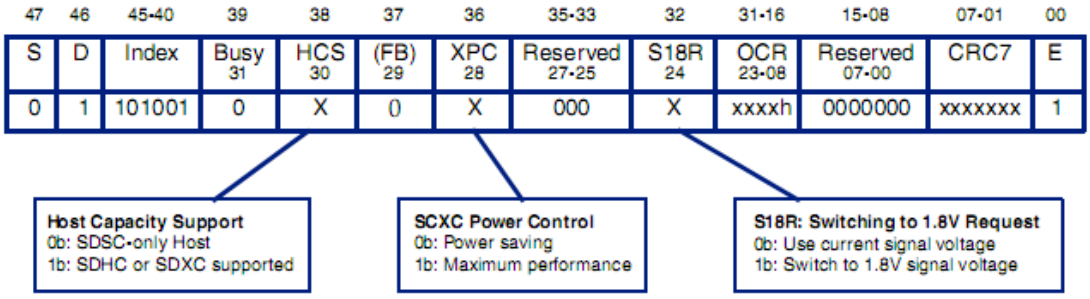


Fig. 3-13 ACMD41 Argument

- Bit 30 informs the card if host supports SDHC/SDXC or not; this bit should be set to 1'b1.
- Bit 28 can be either 1 or 0.
- Bit 24 should be set to 1'b1, indicating that the host is capable of voltage switching; refer to following figure.

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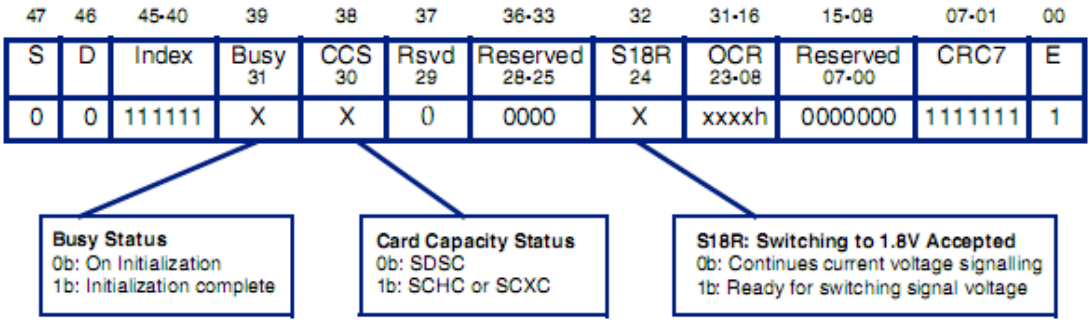


Fig. 3-14 ACMD41 Response(R3)

- Bit 30 – If set to 1'b1, card supports SDHC/SDXC; if set to 1'b0, card supports only SDSC
- Bit 24 – If set to 1'b1, card supports voltage switching and is ready for the switch
- Bit 31 – If set to 1'b1, initialization is over; if set to 1'b0, means initialization in process

4) If the card supports voltage switching, then the software must perform the steps discussed for either the "Voltage Switch Normal Scenario" or the "Voltage Switch Error Scenario".

2. Voltage Switch Normal Scenario

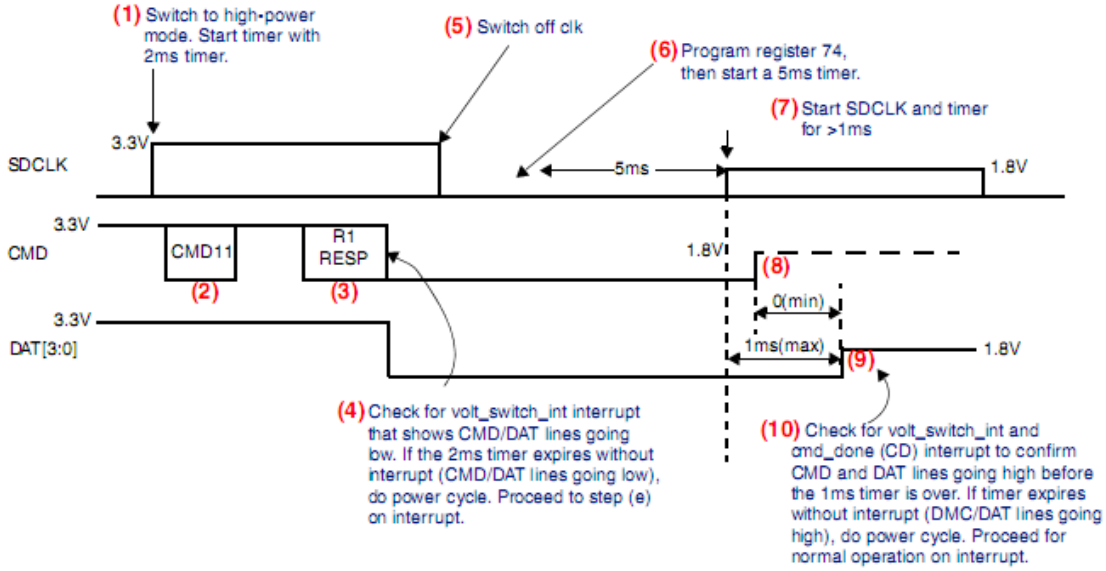


Fig. 3-15 Voltage Switch Normal Scenario

1) The host programs SDMMC_CLKENA—cclk_low_power register—with zero (0) for the corresponding card, which makes the host controller move to high-power mode. The application should start a timer with a recommended value of 2ms; this value of 2 ms is determined as below:Total clk required for CMD11 = 48 clks
   Total clk required for RESP R1 = 48 clks
   Maximum clk delay between MCD11 end to start of RESP1 = 60 clks
   Total = 48+48 + 60 = 160
   Minimum frequency during enumeration is 100 KHz; that is, 10us
   Total time = 160 * 10us = 1600us = 1. 6ms ~ 2ms
2) The host issues CMD11 to start the voltage switch sequence. Set bit 28 to 1'b1 in CMD when setting CMD11; for more information on setting bits, refer to "Boot Operation".
3) The card returns R1 response; the host controller does not generate cmd_done interrupt on receiving R1 response.
4) The card drives CMD and DAT [3:0] to low immediately after the response. The host controller generates interrupt (VOLT_SWITCH_INT) once the CMD or DAT [3:0] line goes

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low. The application should wait for this interrupt. If the 2ms timer expires without an interrupt (CMD/DAT lines going low), do a power cycle.

Note: Before doing a power cycle, switch off the card clock by programming SDMMC_CLKENA register

Proceed to step (5) on getting an interrupt (VOLT_SWITCH_INT).

Note: This interrupt must be cleared once this interrupt is received. Additionally, this interrupt should not be masked during the voltage switch sequence.

If the timer expires without interrupt (CMD/DAT lines going low), perform a power cycle.

Proceed to step (5) on interrupt.

1) Program the SDMMC_CLKENA, cclk_enable register, with 0 for the corresponding card; the host stops supplying SDCLK.
2) Program Voltage register to the required values for the corresponding card. The application should start a timer > 5ms.
3) After the 5ms timer expires, the host voltage regulator is stable. Program SDMMC_CLKENA, cclk_enable register, with 1 for the corresponding card; the host starts providing SDCLK at 1. 8V; this can be at zero time after Voltage register has been programmed. When the SDMMC_CLKENA register is programmed, the application should start another timer > 1ms.
4) By detecting SDCLK, the card drives CMD to high at 1. 8V for at least one clock and then stops driving (tri-state); CMD is triggered by the rising edge of SDCLK (SDR timing).
5) If switching to 1. 8V signaling is completed successfully, the card drives DAT [3:0] to high at 1. 8V for at least one clock and then stops driving (tri-state); DAT [3:0] is triggered by the rising edge of SDCLK (SDR timing). DAT[3:0] must be high within 1ms from the start of SDCLK.
6) The host controller generates a voltage switch interrupt (VOLT_SWITCH_INT) and a command done (CD) interrupt once the CMD and DAT[3:0] lines go high. The application should wait for this interrupt to confirm CMD and DAT lines going high before the 1ms timer is done.

If the timer expires without the voltage switch interrupt (VOLT_SWITCH_INT), a power cycle should be performed. Program the SDMMC_CLKENA register to stop the clock for the corresponding card number. Wait for the cmd_done (CD) interrupt. Proceed for normal operation on interrupt. After the sequence is completed, the host and the card start communication in SDR12 timing.

3. Voltage Switch Error Scenario

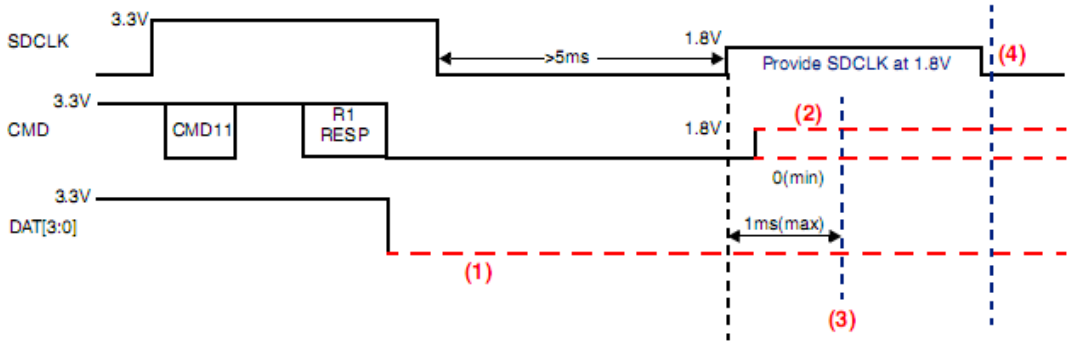


Fig. 3-16 Voltage Switch Error Scenario

1) If the interrupt (VOLT_SWITCH_INT) does not come, then the 2 ms timer should time out and a power cycle should be initiated.

Note: Before performing a power cycle, switch off the card clock by programming SDMMC_CLKENA register; no cmd_done (CD) interrupt is generated.

Additionally, if the card detects a voltage error at any point in between steps (5) and (7) in the card keeps driving DAT[3:0] to low until card power off.

2) CMD can be low or tri-state.

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3) The host controller generates a voltage switch interrupt once the CMD and DAT[3:0] lines go high. The application should check for an interrupt to confirm CMD and DAT lines going high before the 1 ms timer is done.

If the 1 ms timer expires without interrupt (VOLT_SWITCH_INT) and cmd_done (CD), a power cycle should be performed. Program the SDMMC_CLKENA register to stop SDCLK of the corresponding card. Wait for the cmd_done interrupt. Proceed for normal operation on interrupt.

4) If DAT[3:0] is low, the host drives SDCLK to low and then stops supplying the card power.

Note: The card checks voltages of its own regulator output and host signals to ensure they are less than 2. 5V. Errors are indicated by (1) and (2).

- If voltage switching is accepted by the card, the default speed is SDR12.
- Command Done is given:
  - If voltage switching is properly done, CMD and DAT line goes high.
  - If switching is not complete, the 1ms timer expires, and the card clk is switched off.

Note: No other CMD should be driven before the voltage switching operation is completed and Command Done is received.

- The application should use CMD6 to check and select the particular function; the function appropriate-speed should be selected.

After the function switches, the application should program the correct value in the CLKDIV register, depending on the function chosen. Additionally, if Function 0x4 of the Access mode is chosen—that is, DDR50, then the application should also program 1'b1 in DDR_REG for the card number that has been selected for DDR50 mode.

3.6.6 Back-End Power

Each device needs one bit to control the back-end power supply for an embedded device; this bit does not control the VDDH of the host controller. A back_end_power register enables software programming for back-end power. The value on this register is output to the back_end_power signal, which can be used to switch power on and off the embedded device.

3.6.7 DDR Operation

1. 4-bit DDR Programming Sequence

DDR programming should be done only after the voltage switch operation has completed. The following outlines the steps for the DDR programming sequence:

1) Once the voltage switch operation is complete, the user must program voltage selection register to the required values for the corresponding card.

- To start a card to work in DDR mode, the application must program a bit of the newly defined SDMMC_UHS_REG[16] register with a value of 1'b1.
- The bit that the user programs depends on which card is to be accessed in DDR mode.

2) To move back to SDR mode, a power cycle should be run on the card—putting the card in SDR12 mode—and only then should SDMMC_UHS_REG[16]be set back to 1'b0 for the appropriate card.

2. 8-bit DDR Programming Sequence

The following outlines the steps for the 8-bit DDR programming sequence:

1) The cclk_in signal should be twice the speed of the required cclk_out. Thus, if the cclk_out signal is required to be 50 MHz, the cclk_in signal should be 100 MHz.
2) The CLKDIV register should always be programmed with a value higher than zero (0); that is, a clock divider should always be used for 8-bit DDR mode.
3) The application must program the SDMMC_UHS_REG[16] register (DDR_REG bits) by assigning it with a value of 1 for the bit corresponding to the card number; this causes the selected card to start working in DDR mode.

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4) Depending on the card number, the SDMMC_CTYPE [31:16] bits should be set in order to make the host work in the 8-bit mode.

3. eMMC4.5 DDR START Bit

The eMMC4.5 changes the START bit definition in the following manner:

1) Receiver samples the START bit on the rising edge.
2) On the next rising edge after sampling the START bit, the receiver must sample the data.
3) Removes requirement of the START bit and END bit to be high for one full cycle.

Notes: The Host Controller does not support a START bit duration higher than one clock cycle. START bit durations of one or less than one clock cycle are supported and can be defined at the time of startup by programming the EMMC_DDR_REG register.

Following figure illustrates cases for the definition change of the START bit with eMMC4.5; it also illustrates how some of these cases can fail in sampling when higher-value delays are considered for I/O PADs.

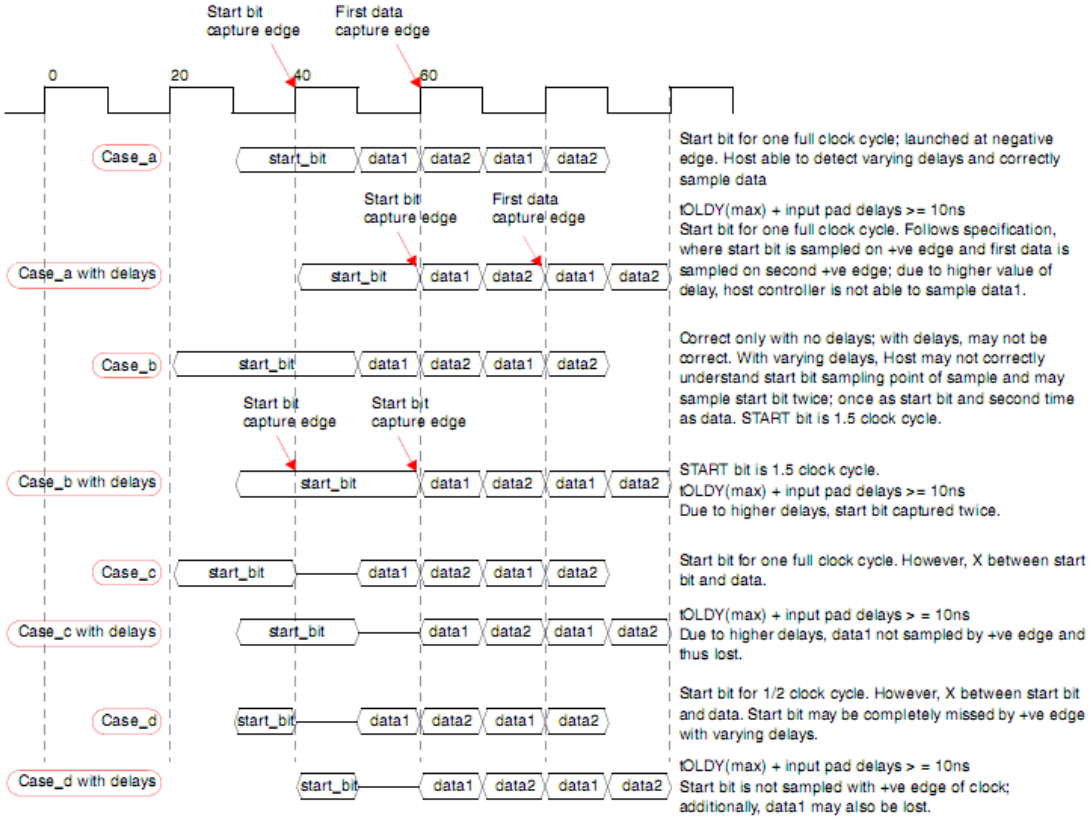


Fig. 3-17 CASES for eMMC 4.5 START bit

4. Reset Command/Moving from DDR50 to SDR12

To reset the mode of operation from DDR50 to SDR12, the following sequence of operations has to be done by the application:

1) Issue CMD0.

When CMD0 is received, the card changes from DDR50 to SDR12.

2) Program the SDMMC_CLKDIV register with an appropriate value.
3) Set DDR_REG to 0.

Note: The Voltage register should not be programmed to 0 while switching from DDR50 to SDR12, since the card is still operating in 1.8V mode after receiving CMD0.

3.6.8 H/W Reset Operation

When the RST_n signal goes low, the card enters a pre-idle state from any state other than the inactive state.

H/W Reset Programming Sequence

The following outlines the steps for the H/W reset programming sequence:

11) Program CMD12 to end any transfer in process.
12) Wait for DTO, even if no response is sent back by the card.

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13) Set the following resets:

- DMA reset–SDMMC_CTRL[2]
- FIFO reset –SDMMC_CTRL[1] bits

Note: The above steps are required only if a transfer is in process.

14) Program the CARD_RESET register with a value of 0; this can be done at any time when the card is connected to the controller. This programming asserts the RST_n signal and resets the card.
15) Wait for minimum of 1 µs or cclk_in period, whichever is greater
16) After a minimum of 1 µs, the application should program a value of 0 into the CARD_RESET register. This de-asserts the RST_n signal and takes the card out of reset.
17) The application can program a new CMD only after a minimum of 200 µs after the de-assertion of the RST_n signal, as per the MMC 4.41 standard.

Note: For backward compatibility, the RST_n signal is temporarily disabled in the card by default. The host may need to set the signal as either permanently enabled or permanently disabled before it uses the card.

3.6.9 FBE Scenarios

An FBE occurs due to an AHB error response on the AHB bus. This is a system error, so the software driver should not perform any further programming to the Host. The only recovery mechanism from such scenarios is to do one of the following:

- Issue a hard reset by asserting the reset_n signal
- Do a program controller reset by writing to the CTRL[0] register

1. FIFO Overflow and Underflow

During normal data transfer conditions, FIFO overflow and underflow will not occur. However if there is a programming error, then FIFO overflow/underflow can result. For example, consider the following scenarios.

- For transmit: PBL=4, Tx watermark = 1. For the above programming values, if the FIFO has only one location empty, it issues a dma_req to IDMAC FSM. Due to PBL value=4, the IDMAC FSM performs 4 pushes into the FIFO. This will result in a FIFO overflow interrupt.
- For receive: PBL=4, Rx watermark = 1. For the above programming values, if the FIFO has only one location filled, it issues a dma_req to IDMAC FSM. Due to PBL value=4, the IDMAC FSM performs 4 pops to the FIFO. This will result in a FIFO underflow interrupt.

The driver should ensure that the number of bytes to be transferred as indicated in the descriptor should be a multiple of 4bytes with respect to H_DATA_WIDTH=32. For example, if the BYTCNT = 13, the number of bytes indicated in the descriptor should be 16 for H_DATA_WIDTH=32.

2. Programming of PBL and Watermark Levels

The DMAC performs data transfers depending on the programmed PBL and threshold values.

Table 3-15 PBL and Watermark Levels

PBL (Number of transfers)	Tx/Rx Watermark Value
1	greater than or equal to 1
4	greater than or equal to 4
8	greater than or equal to 8
16	greater than or equal to 16
32	greater than or equal to 32
64	greater than or equal to 64
128	greater than or equal to 128
256	greater than or equal to 256

3.6.10 Variable Delay/Clock Generation

Variable delay mechanism for the cclk_in_drv is optional, but it can be useful in order to meet a range of hold-time requirements across modes. Variable delay mechanism for the cclk_in_sample is mandatory and is required to achieve the correct sampling point for data.

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cclk_in/cclk_in_sample/ cclk_in_drv is generated by Clock Generation Unit (CLKGEN) with variable delay mechanism, which includes Phase Shift Unit and Delay Line Unit selectable.
The Phase Shift Unit can shift cclk_in_sample/cclk_in_drv by 0/90/180/270-degree relative to cclk_in, controlled by sample_degree/drv_degree.
The Delay Line Unit can shift cclk_in_sample/cclk_in_drv in the unit of 40ps~80ps for every delay element. The delay unit number is determined by sample_delaynum/drv_delaynum, and enabled by sample_sel/drv_sel.
cclk_in is generated by cclkin divided by 2. cclk_in_drv and cclk_in_sample clocks are phase-shifted with delayed versions of cclk_in. All clocks are recommended to have a 50% duty cycle; DDR modes must have 50% duty cycles.
The architecture is as follows.

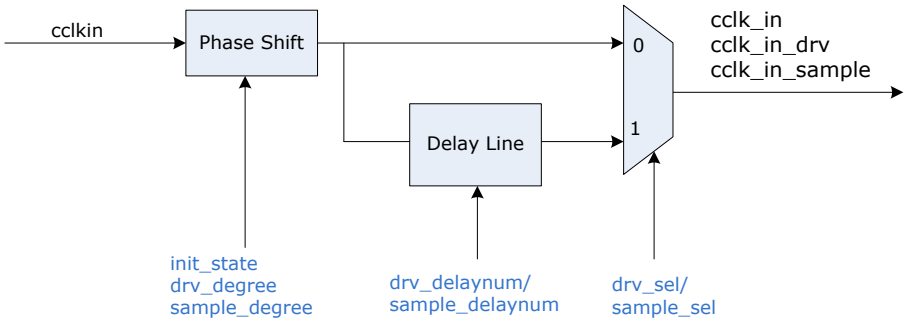


Fig. 3-18 Clock Generation Unit

The control signals for different Host Controller instance are shown as follows:

Table 3-16 Configuration for SDMMC Clock Generation

Signal Name	Source	Default	Description
init_state	CRU_SDMMC_CON0[0]	0	Soft initial state for phase shift.
drv_degree[1:0]	CRU_SDMMC_CON0[2:1]	2	Phase shift for cclk_in_drv. 0: 0-degree 1: 90-degree 2: 180-degree 3: 270-degree
drv_delaynum[7:0]	CRU_SDMMC_CON0[10:3]	0	Element number in delay line for cclk_in_drv
drv_sel	CRU_SDMMC_CON0[11]	0	cclk_in_drv source selection: 0: use clock after phase_shift 1: use clock after phase_shift and delay line
sample_degree[1:0]	CRU_SDMMC_CON1[2:1]	0	Phase shift for cclk_in_sample. 0: 0-degree 1: 90-degree 2: 180-degree 3: 270-degree
sample_delaynum[7:0]	CRU_SDMMC_CON1[10:3]	0	Element number in delay line for cclk_in_sample
sample_sel	CRU_SDMMC_CON1[11]	0	cclk_in_sample source selection: 0: use clock after phase_shift 1: use clock after phase_shift and delay line

Table 3-17 Configuration for SDIO Clock Generation

Signal Name	Source	Default	Description
init_state	CRU_SDIO_CON0[0]	0	Soft initial state for phase shift.
drv_degree[1:0]	CRU_SDIO_CON0[2:1]	2	Phase shift for cclk_in_drv. 0: 0-degree 1: 90-degree 2: 180-degree 3: 270-degree

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Signal Name	Source	Default	Description
drv_delaynum [7:0]	CRU_SDIO_CON0[10:3]	0	Element number in delay line for cclk_in_drv
drv_sel	CRU_SDIO_CON0[11]	0	cclk_in_drv source selection: 0: use clock after phase_shift 1: use clock after phase_shift and delay line
sample_degree [1:0]	CRU_SDIO_CON1[2:1]	0	Phase shift for cclk_in_sample. 0: 0-degree 1: 90-degree 2: 180-degree 3: 270-degree
sample_delaynum[7:0]	CRU_SDIO_CON1[10:3]	0	Element number in delay line for cclk_in_sample
sample_sel	CRU_SDIO_CON1[11]	0	cclk_in_sample source selection: 0: use clock after phase_shift 1: use clock after phase_shift and delay line

Table 3-18 Configuration for EMMC Clock Generation

Signal Name	Source	Default	Description
init_state	CRU_EMMC_CON0[0]	0	Soft initial state for phase shift.
drv_degree[1:0]	CRU_EMMC_CON0[2:1]	2	Phase shift for cclk_in_drv. 0: 0-degree 1: 90-degree 2: 180-degree 3: 270-degree
drv_delaynum [7:0]	CRU_EMMC_CON0[10:3]	0	Element number in delay line for cclk_in_drv
drv_sel	CRU_EMMC_CON0[11]	0	cclk_in_drv source selection: 0: use clock after phase_shift 1: use clock after phase_shift and delay line
sample_degree[1:0]	CRU_EMMC_CON1[2:1]	0	Phase shift for cclk_in_sample. 0: 0-degree 1: 90-degree 2: 180-degree 3: 270-degree
sample_delaynum[7:0]	CRU_EMMC_CON1[10:3]	0	Element number in delay line for cclk_in_sample
sample_sel	CRU_EMMC_CON1[11]	0	cclk_in_sample source selection: 0: use clock after phase_shift 1: use clock after phase_shift and delay line

The following outlines the steps for clock generation sequence:

1) Assert init_state to soft reset the CLKGEN.
2) Configure drv_degree/sample_degree.
3) If fine adjustment required, delay line can be used by configuring drv_delaynum/sample_delaynum and drv_sel/sample_sel.
4) Dis-assert init_state to start CLKGEN.

3.6.11 Variable Delay Tuning

Tuning is defined by SD and MMC cards to determine the correct sampling point required for the host, especially for the speed modes SDR104 and HS200 where the output delays from the cards can be up to 2 UI. Tuning is required for other speed modes-such as DDR50-even

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though the output delay from the card is less than one cycle.
Command for tuning is different for different cards.

- SD Memory Card:
  - CMD19 – SD card for SDR50 and SDR104 speed modes. Tuning data is defined by card specifications.
  - CMD6 – SD card for speed modes not supporting CMD19. Tuning data is the 64byte SD status.
- Multimedia Card:
  - CMD21 – MMC card for HS200 speed mode. Tuning data is defined by card specifications.
  - CMD8 – MMC card for speed modes not supporting CMD21. Tuning data is 512 byte ExtCSD data.

The following is the procedure for variable delay tuning:

1) Set a phase shift of 0-degree on cclk_in_sample.
2) Send the Tuning command to the card; the card in turn sends an R1 response on the CMD line and tuning data on the DAT line.
3) If the host sees any of the errors—start bit error, data crc error, end bit error, data read time-out, response crc error, response error—then the sampling point is incorrect.
4) Send CMD12 to bring the host controller state machines to idle.
   - The card may treat CMD12 as an invalid command because the card has successfully sent the tuning data, and it cannot send a response.
   - The host controller may generate a response time-out interrupt that must be cleared by software.
5) Repeat steps 2) to 4) by increasing the phase shift value or delay element number on cclk_in_sample until the correct sampling point is received such that the host does not see any of the errors.
6) Mark this phase shift value as the starting point of the sampling window.
7) Repeat steps 2 to 4 by increasing the phase shift value or delay element number on cclk_in_sample until the host sees the errors starting to come again or the phase shift value reaches 360-degree.
8) Mark the last successful phase shift value as the ending point of the sampling window.

A window is established where the tuning block is matched. For example, for a scenario where the tuning block is received correctly for a phase shift window of 90-degree and 180-degree, then an appropriate sampling point is established as 135-degree. Once a sampling point is established, no errors should be visible in the tuning block.

3.6.12 Package Command

In order to reduce overhead, read and write commands can be packed in groups of commands-either all read or all write-that transfer the data for all commands in the group in one transfer on the bus.
Packed commands can be of two types:

- Packed Write: CMD23 → CMD25
- Packed Read: CMD23 → CMD25 → CMD23 → CMD18

Packed commands are put in packets by the application software and are transparent to the core. For more information on packed commands, refer to the eMMC specification.

3.6.13 Card Detection Method

There are many methods for SDMMC/SDIO device detection.

- Method1: Using SDMMC_CDETECT register, which is value on card_detect_n input port. 0 represents presence of card.

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- Method2: Using card detection unit in Host Controller, outputting host interrupt. The card detection unit looks for any changes in the card-detect signals for card insertion or card removal. It filters out the debounces associated with mechanical insertion or removal, and generates one interrupt to the host. You can program the debounce filter value in SDMMC_DEBNCE [23:0]. Following figure illustrates the timing for card-detect signals.

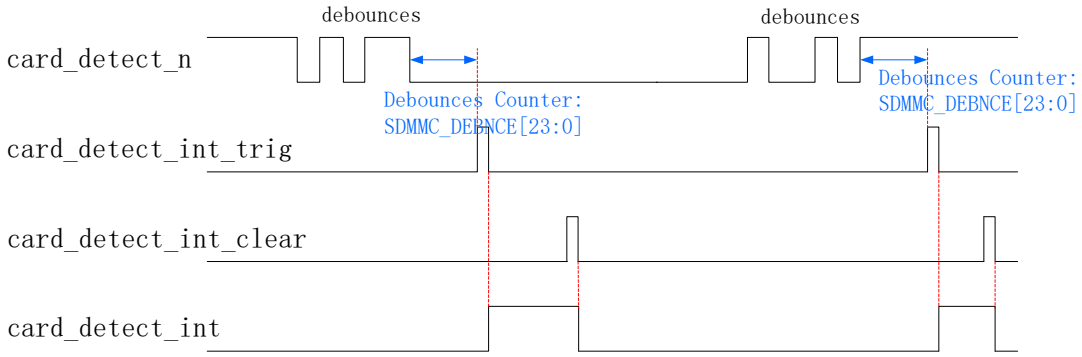


Fig. 3-19 Card Detection Method 2

- Method3: Using card detection unit in GRF, outputting sdmmc_detect_dual_edge_int connecting to IRQ[91]. Similar to Method2, except that the debounce time is configurable by PMUGRF_SDMMC_DET; and the insertion/removal detection interrupt can be enabled or cleared respectively. The detailed register information is:

Table 3-19 Register for SDMMC Card Detection Method 3

Signal Name	Source	Default	Description
sd_detectn_rise_edge_irq_en	PMUGRF_SIG_DETECT_CON[0]	0	sdmmc detect_n signal rise edge interrupt enable. 1: enable 0: disable
sd_detect_fall_edge_detect_en	PMUGRF_SIG_DETECT_CON[1]	0	sd_detect_falling_edge enable 0: disable 1: enable
sd_detect_rising_edge_dectect_status	PMUGRF_SIG_DETECT_STATUS[0]	0	sd_detect_rising_edge status 0: disable 1: enable
sd_detect_fall_edge_detect_status	PMUGRF_SIG_DETECT_STATUS[1]	0	sd_detect_falling_edge status 0: disable 1: enable
sd_detect_rising_edge_dectect_clr	PMUGRF_SIG_DETECT_CLR[0]	0	sd_detect_rising_edge clear 0: disable 1: enable
sd_detect_fall_edge_detect_clr	PMUGRF_SIG_DETECT_CLR[1]	0	sd_detect_falling_edge clear 0: disable 1: enable

- Method4: Using filtered card_detect_n with the debounce time PMUGRF_SDMMC_DET for interrupt source, connecting to IRQ [92] directly.

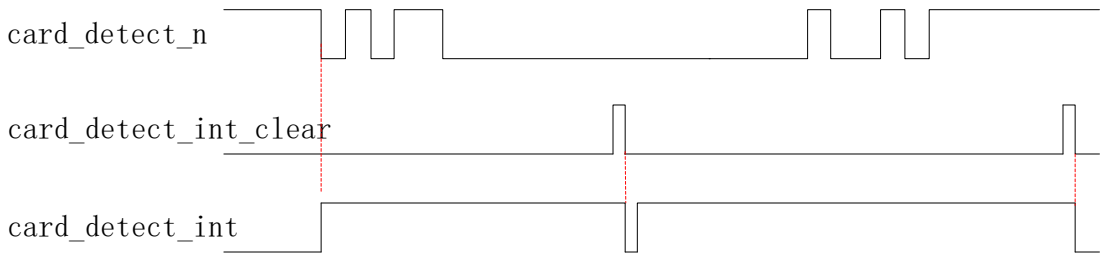


Fig. 3-20 Card Detection Method 4

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3.6.14 SDMMC IOMUX With JTAG

The IO for sdmmc_cdata2/sdmmc_cdata3 is shared with jtag_tck/jtag_tms. The condition of usage for SDMMC or JTAG usage is as follows.

- If GRF_SOC_CON7[12](grf_force_jtag) is equal to 1 and sdmmc card is not detected within detection time(in the unit of XIN24M clock), the GPIOs are used for JTAG.
- Otherwise, the GPIOs' usage is defined by IOMUX configuration.

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Chapter 4 Multi-format Video Encoder And Decoder

4.1 Overview

VPU_Combo is composed by the H.265 (HEVC) decoder and the H.264 encoder/decoder to realize the high quality video decoding. VPU_Combo is connected to the AHB bus through an AHB slave and the AXI bus through an AXI master. The register configuration is fed into the VPU_Combo through the AHB slave interface while the stream data is transacted between DDR and VPU_Combo through the AXI master interface.
To reduce the area, H.265 decoder and H.264 encoder/decoder not only share several pieces of the internal memories, but also share the bus master and slave interfaces. Therefore VPU_Combo has no any possibility to have the H.265 video decoding and H.264 video encoding/decoding to work simultaneously
In order to improve large data transaction performance, VPU embeds MMU (memory management unit) and supports the cacheable bus operation.
VPU_Combo supports the next-generation video coding standard HEVC (High Efficiency Video Coding, aka H.265) full-HD decoding up to 60fps. With HEVC standard, the data compression ratio can be doubled compared to H.264/MEPG-4 at the same video quality or alternatively to provide substantially improved video at the same bit rate.

4.1.1 Features

- Supports HEVC Main Profile up to Level 4.1 High Tier: 1920x1080@60 fps
  - MMU embedded
  - Supports frame timeout interrupt , frame finish interrupt and bitstream error interrupt
  - Supports RLC write mode, RLC mode and Normal Mode
- Supports decoding of the following standards
  - Error detection and concealment support for all video formats
  - Output data structure after decoder is YCbCr 4:2:0 semi-planar to have more efficient bus usage
  - H.264 up to HP level 4.1 : 1080p@60fps (1920x1088)
  - SVC: base layer only for Baseline/High Profile
  - MVC: Stereo High
  - MPEG-4: Simple Profile up to Level 6; Advanced Profile up to Level 5
  - MPEG-2: Main Profile up to High Level
  - MPEG-1: Main Profile up to High Level
  - H.263: Level 10-70 for Profile 0, and image size up to 720x576
  - JPEG: Baseline interleaved, and supports ROI (region of image) decode
  - RV: RV8, RV9, V10
  - VP7: up to version 3
  - VP8: version 2(webM)
  - WebP
  - For H.264, Image cropping not supported
- Built-in post processor in H.264 decoder supports:
  - Stand-alone mode: rotation, deinterlace, RGB conversion, scaling, dithering and alpha blending
  - Pipe-ling mode: RGB conversion, scaling, dithering and alpha blending
- Supports encoding of the following standards:
  - H.264: up to HP level 4.1
  - JPEG: Baseline (DCT sequential)
- Built-in pre-processor in H.264 encoder supports:
  - Cropping, rotation, YCbCr conversion

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4.2 Block Diagram

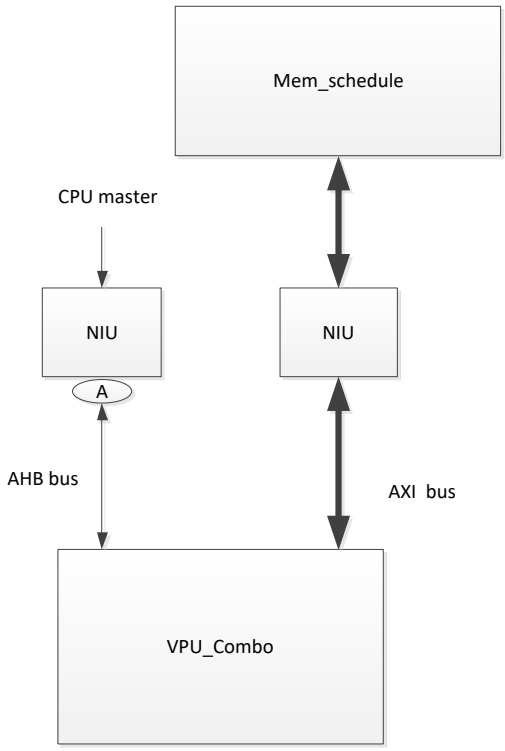


Fig. 4-1 VPU Combo in SOC

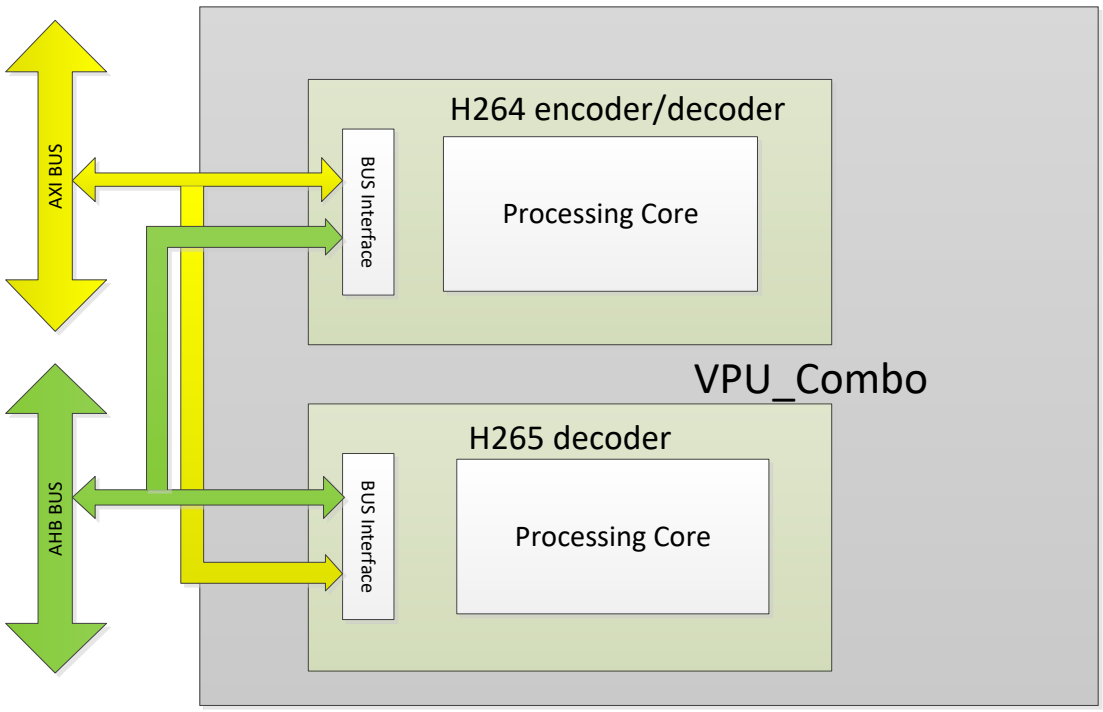


Fig. 4-2 VPU Combo Block Diagram

As shown in the figures above, CPU accesses to HEVC register bank through 32-bit AHB bus. Bitstream and compressed video data are fed into HEVC core though 128-bit AXI read channel, and after several steps of decoding process, decoded pictures are transferred to designated location in the DDR through 64-bit AXI write channel.

CPU accesses to H264encoder/decoder register bank through 32-bit AHB bus. Video data are fed into H.264 core though 64-bit AXI read channel, and after several steps of decoding process, process results are transferred to designated location in the DDR through 64-bit AXI write channel.

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4.3 Function Description

4.3.1 HEVC Standard

High Efficiency Video Coding (HEVC) is a video compression standard, a successor to H.264/MPEG-4 AVC (Advanced Video Coding), that was jointly developed by the ISO/IEC Moving Picture Experts Group (MPEG) and ITU-T Video Coding Experts Group (VCEG) as ISO/IEC 23008-2 MPEG-H Part 2 and ITU-T H.265. MPEG and VCEG established a Joint Collaborative Team on Video Coding (JCT-VC) to develop the HEVC standard.
HEVC was designed to substantially improve coding efficiency compared to H.264/MPEG-4 AVC HP, i.e. to reduce bitrate requirements by half with comparable image quality, at the expense of increased computational complexity. HEVC was designed with the goal of allowing video content to have a data compression ratio of up to 1000:1. Depending on the application requirements HEVC encoders can trade off computational complexity, compression rate, robustness to errors, and encoding delay time.Two of the key features where HEVC was improved compared to H.264/MPEG-4 AVC was support for higher resolution video and improved parallel processing methods.

4.3.2 HEVC Coding Tools

1. Coding tree unit

HEVC replaces macroblocks, which were used with previous standards, with Coding Tree Units (CTUs) which can use a larger block structures of up to 64x64 pixels and can better sub-partition the picture into variable sized structures. HEVC initially divides the picture into CTUs which can be 64x64, 32x32, or 16x16 with a larger pixel block size usually increasing the coding efficiency.

2. Parallel processing tools

Tiles allow for the picture to be divided up into a grid of rectangular regions that can independently be decoded/encoded and the main purpose of tiles is to allow for parallel processing.Tiles can be independently decoded and can even allow for random access to specific regions of a picture in a video stream.
Wavefront parallel processing (WPP) is when a slice is divided into rows of CTUs in which the first row is decoded normally but each additional row requires that decisions be made in the previous row. WPP has the entropy encoder use information from the preceding row of CTUs and allows for a method of parallel processing that may allow for better compression than tiles.
Tiles and WPP are allowed but are optional.If tiles are present they must be at least 64 pixels high and 256 pixels wide with a level specific limit on the number of tiles allowed.
Slices can for the most part be decoded independently from each other with the main purpose of tiles being re-synchronization in case of data loss in the video stream. Slices can be defined as self-contained in that prediction is not made across slice boundaries. When in-loop filtering is done on a picture though information across slice boundaries may be required.[1] Slices are CTUs decoded in the order of the raster scan and different coding types can be used for slices such as I types, P types, or B types.
Dependent slices can allow for data related to tiles or WPP to be accessed more quickly by the system than if the entire slice had to be decoded.[1] The main purpose of dependent slices is to allow for low delay video encoding due to its lower latency.

3. Entropy coding

HEVC uses a context-adaptive binary arithmetic coding (CABAC) algorithm that is fundamentally similar to CABAC in H.264/MPEG-4 AVC. CABAC is the only entropy encoder method that is allowed in HEVC while there are two entropy encoder methods allowed by H.264/MPEG-4 AVC. CABAC and the entropy coding of transform coefficients in HEVC were designed for a higher throughput than H.264/MPEG-4 AVC. For instance, the number of context coded bins have been reduced by 8x and the CABAC bypass-mode has been

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improved in terms of its design to increase throughput. Another improvement with HEVC is that the dependencies between the coded data has been changed to further increase throughput. Context modeling in HEVC has also been improved so that CABAC can better select a context that increases efficiency when compared to H.264/MPEG-4 AVC.

4. Intra prediction

HEVC specifies 33 directional modes for intra prediction compared to the 8 directional modes for intra prediction specified by H.264/MPEG-4 AVC. HEVC also specifies planar and DC intra prediction modes.[1] The intra prediction modes use data from neighboring prediction blocks that have been previously decoded.

5. Motion compensation

For the interpolation of fractional luma sample positions HEVC uses separable application of one-dimensional half-sample interpolation with an 8-tap filter or quarter-sample interpolation with a 7-tap filter while, in comparison, H.264/MPEG-4 AVC uses a two-stage process that first derives values at half-sample positions using separable one-dimensional 6-tap interpolation followed by integer rounding and then applies linear interpolation between values at nearby half-sample positions to generate values at quarter-sample positions.[1] HEVC has improved precision due to the longer interpolation filter and the elimination of the intermediate rounding error. For 4:2:0 video, the chroma samples are interpolated with separable one-dimensional 4-tap filtering to generate eighth-sample precision, while in comparison H.264/MPEG-4 AVC uses only a 2-tap bilinear filter (also with eighth-sample precision).
As in H.264/MPEG-4 AVC, weighted prediction in HEVC can be used either with uni-prediction (in which a single prediction value is used) or bi-prediction (in which the prediction values from two prediction blocks are combined).

6. Motion vector prediction

HEVC defines a signed 16-bit range for both horizontal and vertical motion vectors (MVs). This was added to HEVC at the July 2012 HEVC meeting with the mvLX variables. HEVC horizontal/vertical MVs have a range of −32768 to 32767 which given the quarter pixel precision used by HEVC allows for a MV range of −8192 to 8191.75 luma samples. This compares to H.264/MPEG-4 AVC which allows for a horizontal MV range of −2048 to 2047.75 luma samples and a vertical MV range of −512 to 511.75 luma samples.
HEVC allows for two MV modes which are Advanced Motion Vector Prediction (AMVP) and merge mode. AMVP uses data from the reference picture and can also use data from adjacent prediction blocks. The merge mode allows for the MVs to be inherited from neighboring prediction blocks. Merge mode in HEVC is similar to "skipped" and "direct" motion inference modes in H.264/MPEG-4 AVC but with two improvements. The first improvement is that HEVC uses index information to select one of several available candidates. The second improvement is that HEVC uses information from the reference picture list and reference picture index.

7. Inverse transforms

HEVC specifies four transform units (TUs) sizes of 4x4, 8x8, 16x16, and 32x32 to code the prediction residual. A CTB may be recursively partitioned into 4 or more TUs.[1] TUs use integer basis functions that are similar to the discrete cosine transform (DCT). In addition 4x4 luma transform blocks that belong to an intra coded region are transformed using an integer transform that is derived from discrete sine transform (DST). This provides a 1% bit rate reduction but was restricted to 4x4 luma transform blocks due to marginal benefits for the other transform cases. Chroma uses the same TU sizes as luma so there is no 2x2 transform for chroma.

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8. Loop filters

HEVC specifies two loop filters that are applied sequentially, with the deblocking filter (DBF) applied first and the sample adaptive offset (SAO) filter applied afterwards. Both loop filters are applied in the inter-picture prediction loop, i.e. the filtered image is stored in the decoded picture buffer (DPB) as a reference for inter-picture prediction.

8.1 Deblocking filter

The DBF is similar to the one used by H.264/MPEG-4 AVC but with a simpler design and better support for parallel processing.[1] In HEVC the DBF only applies to a 8x8 sample grid while with H.264/MPEG-4 AVC the DBF applies to a 4x4 sample grid. DBF uses a 8x8 sample grid since it causes no noticeable degradation and significantly improves parallel processing because the DBF no longer causes cascading interactions with other operations. Another change is that HEVC only allows for three DBF strengths of 0 to 2. HEVC also requires that the DBF first apply horizontal filtering for vertical edges to the picture and only after that does it apply vertical filtering for horizontal edges to the picture. This allows for multiple parallel threads to be used for the DBF.

8.2 Sample adaptive offset

The SAO filter is applied after the DBF and is designed to allow for better reconstruction of the original signal amplitudes by applying offsets stored in a lookup table in the bitstream. Per CTB the SAO filter can be disabled or applied in one of two modes: edge offset mode or band offset mode. The edge offset mode operates by comparing the value of a sample to two of its eight neighbors using one of four directional gradient patterns. Based on a comparison with these two neighbors, the sample is classified into one of five categories: minimum, maximum, an edge with the sample having the lower value, an edge with the sample having the higher value, or monotonic. For each of the first four categories an offset is applied. The band offset mode applies an offset based on the amplitude of a single sample. A sample is categorized by its amplitude into one of 32 bands (histogram bins). Offsets are specified for four consecutive of the 32 bands, because in flat areas which are prone to banding artifacts, sample amplitudes tend to be clustered in a small range.[1][135] The SAO filter was designed to increase picture quality, reduce banding artifacts, and reduce ringing artifacts.

4.3.3 MMU

The MMU divides memory into 4KB pages, where each page can be individually configured. For each page the following parameters are specified:

- Address translation of virtual memory, this enables the processor to work using address that differ from the physical address in the memory system.
- The permitted types of accesses to that page. Each page can permit read, write, both, or none.

The MMU use 2-level page table structure:

1. The first level, the page directory consists of 1024 directory table entries(DTEs), each pointing to a page table.
2. The second level, the page table consists of 1024 page table entries(PTEs), each pointing to a page in memory.

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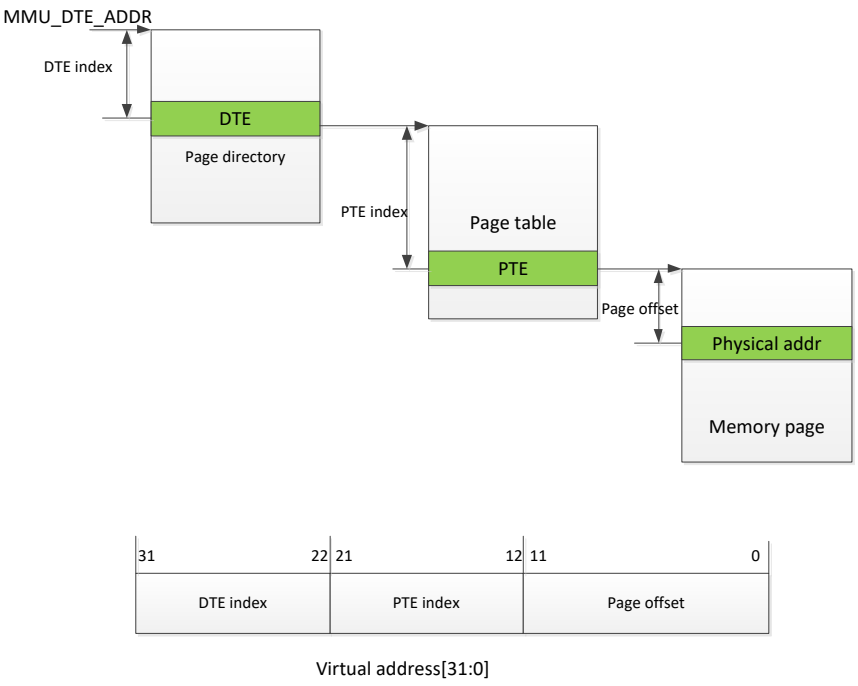


Fig. 4-3 structure of two-level page table

4.3.4 HEVC Working Mode

There are there working modes to be selected for HEVC decoder: RLC Mode, RLC Write Mode, Normal Mode.

The key differences among three working modes are whether CABAC module and Post-CABAC module are involved into the hardware decoding process.

For RLC mode, CABAC are bypassed and the input bitstream to the Post-CABAC module should be already decoded.

For RLC write mode, the decoded results by CABAC are output to the DDR, and the following decoding processes are stopped.

As for the normalmode , all the modules are involved into the decoding process, and complete decoding results are output. Normally, this mode should be selected.

4.3.5 H.264 decoder

The input of the decoder is H.264 standard bit stream in either plain NAL unit format or byte stream format. The input format in use will be automatically detected. The H.264 video encoding allows the use of multiple reference pictures, which means that the decoding order of the pictures may be different from their display order. The decoder can perform internally the display reordering of the decoded pictures or it can skip this and output all the pictures as soon as they are decoded.

The decoder has two operating modes: in the primary mode the HW performs entropy decoding, and in the secondary mode SW performs entropy decoding. Secondary mode is used in H.264 ASO or Slice Group stream decoding.

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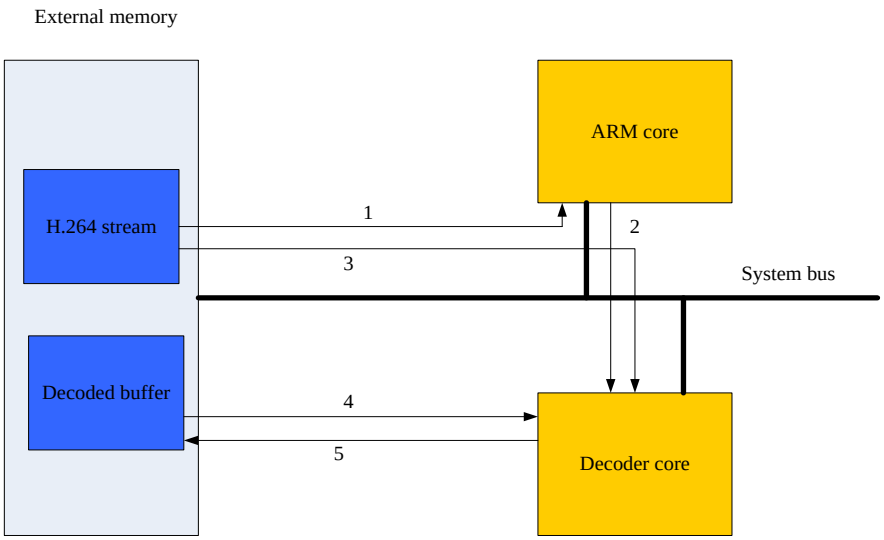


Fig. 4-4 Dataflow of HW performs entropy decoding in video decoder

The dataflow of HW performs entropy decoding is as Fig. 4-4 shown. The decoder software (SW) starts decoding the first picture by parsing the stream headers (1). Software then setups the hardware control registers (picture size, stream start address etc.) and enables the hardware (2).Hardware decodes the picture by reading stream (3) and the reference pictures (required for inter picture decoding)(4) from the external memory. Hardware writes the decoded output picture to memory one macroblock at a time (5). When the picture has been fully decodedor the hardware has run out of stream data, it gives an interrupt with a proper status flag and provides stream and address for software to continue and returns to initial state.

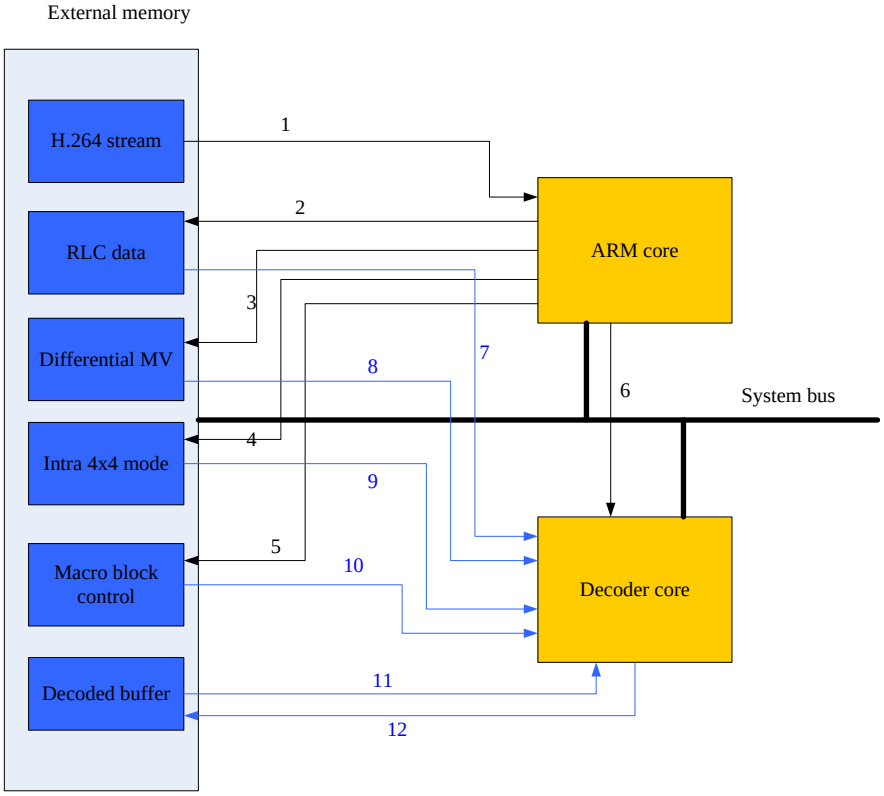


Fig. 4-5 Dataflow of SW performs entropy decoding in video decoder

SW entropy decoding mode (RLC mode) changes the input data format that is transferred from SW to HW. The dataflow of this mode is as Fig. 4-5.In this case the decoder software

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starts decoding the first picture by parsing the stream headers (1), and by performing entropy decoding. Software then writes the following items to external memory:
Run-length-code (RLC) data (2)
Differential motion vectors (3)
Intra 4x4 prediction modes (4)
Macroblock control data (5)
Last step for the software is to write the hardware control registers and to enable the hardware (6).
Hardware decodes the picture by buffering control data for several macroblocks at a time, and reading then appropriate amount of RLC data, differential motion vectors and intra modes depending on each macroblock type (7)-(10).For the rest of the decoding process (11)-(12), the functionality is identical to the HW entropy decoding mode.When the picture has been fully decoded, hardware can raise an interrupt and write the status bits in the status register.

4.4 Register Description

This section describes the control/status registers of the VPU_Combo.
If HEVC is chosen to work, HEVC register base address is the base address of the HEVC. The HEVC reading MMU master register base address is hevc_base+0x440, the writing MMU register base address is hevc_base + 0x480, and the cache control register base address is hevc_base + 0x400.
If H.264 decoder/encoder is chosen to work, VEPU(encoder) register base address is vpu_base, and VDPU(decoder) base address is vpu_base + 0x400. MMU base address is vpu_base+0x800, and VDPU cache control base address is vpu_base + 0xc00.

4.4.1 HEVC Register Summary

Name	Offset	Size	Reset Value	Description
hevc_swreg0_id	0x0000	W	0x68761100	ID register (read only)
hevc_swreg1_int	0x0004	W	0x00200022	interrupt and enable register
hevc_swreg2_sysctrl	0x0008	W	0x00000000	Data input and output endian setting and sys ctrl
hevc_swreg3_picpar	0x000c	W	0x00000000	picture parametes
hevc_swreg4_strm_rlc_base	0x0010	W	0x00000000	the stream or rlc read data base address
hevc_swreg5_stream_rlc_len	0x0014	W	0x00000000	amount of stream bytes in the input bufferor amount ot rlc bytes in the input buffer
hevc_swreg6_cabactbl_base	0x0018	W	0x00000000	the base address of cabac table
hevc_swreg7_decout_base	0x001c	W	0x00000000	base address of decoder output picturesuggest this register to config to even for advance ddr performance
hevc_swreg8_y_virstride	0x0020	W	0x00000000	the output picture y fac virtual stridesuggest this register to config to even for advance ddr performance

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Name	Offset	Size	Reset Value	Description
hevc_swreg9_yuv_virstride	0x0024	W	0x00000000	the ouput picture yuv virtual stride
hevc_swreg10_refer0_base	0x0028	W	0x00000000	base address for reference picture index 0suggest this register to config to even for advance ddr performance
hevc_swreg11_refer1_base	0x002c	W	0x00000000	base address for reference picture index 1
hevc_swreg12_refer2_base	0x0030	W	0x00000000	base address for reference picture index 2
hevc_swreg13_refer3_base	0x0034	W	0x00000000	base address for reference picture index 3
hevc_swreg14_refer4_base	0x0038	W	0x00000000	base address for reference picture index 4
hevc_swreg15_refer5_base	0x003c	W	0x00000000	base address for reference picture index 5
hevc_swreg16_refer6_base	0x0040	W	0x00000000	base address for reference picture index 6
hevc_swreg17_refer7_base	0x0044	W	0x00000000	base address for reference picture index 7
hevc_swreg18_refer8_base	0x0048	W	0x00000000	base address for reference picture index 8
hevc_swreg19_refer9_base	0x004c	W	0x00000000	base address for reference picture index 9
hevc_swreg20_refer10_base	0x0050	W	0x00000000	base address for reference picture index 10
hevc_swreg21_refer11_base	0x0054	W	0x00000000	base address for reference picture index 11
hevc_swreg22_refer12_base	0x0058	W	0x00000000	base address for reference picture index 12
hevc_swreg23_refer13_base	0x005c	W	0x00000000	base address for reference picture index 13
hevc_swreg24_refer14_base	0x0060	W	0x00000000	base address for reference picture index 14
hevc_swreg25_refer0_poc	0x0064	W	0x00000000	the poc of reference picture index 0
hevc_swreg26_refer1_poc	0x0068	W	0x00000000	the poc of reference picture index 1
hevc_swreg27_refer2_poc	0x006c	W	0x00000000	the poc of reference picture index 2
hevc_swreg28_refer3_poc	0x0070	W	0x00000000	the poc of reference picture index 3

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Name	Offset	Size	Reset Value	Description
hevc_swreg29_refer4_poc	0x0074	W	0x00000000	the poc of reference picture index 4
hevc_swreg30_refer5_poc	0x0078	W	0x00000000	the poc of reference picture index 5
hevc_swreg31_refer6_poc	0x007c	W	0x00000000	the poc of reference picture index 6
hevc_swreg32_refer7_poc	0x0080	W	0x00000000	the poc of reference picture index 7
hevc_swreg33_refer8_poc	0x0084	W	0x00000000	the poc of reference picture index 8
hevc_swreg34_refer9_poc	0x0088	W	0x00000000	the poc of reference picture index 9
hevc_swreg35_refer10_poc	0x008c	W	0x00000000	the poc of reference picture index 10
hevc_swreg36_refer11_poc	0x0090	W	0x00000000	the poc of reference picture index 11
hevc_swreg37_refer12_poc	0x0094	W	0x00000000	the poc of reference picture index 12
hevc_swreg38_refer13_poc	0x0098	W	0x00000000	the poc of reference picture index 13
hevc_swreg39_refer14_poc	0x009c	W	0x00000000	the poc of reference picture index 14
hevc_swreg40_cur_poc	0x00a0	W	0x00000000	the poc of cur picture
hevc_swreg41_rlcwrite_base	0x00a4	W	0x00000000	the base address of rlcwrite base addresswhen frame is ready , it is the address of the end of rlcwrite address
hevc_swreg42_pps_base	0x00a8	W	0x00000000	the base address of pps
hevc_swreg43_rps_base	0x00ac	W	0x00000000	the base address of rps
hevc_swreg44_cabac_error_en	0x00b0	W	0x00000000	cabac error enable config
hevc_swreg45_cabac_error_status	0x00b4	W	0x00000000	cabac error status
hevc_swreg46_cabac_error_ctu	0x00b8	W	0x00400000	cabac error ctu
hevc_swreg47_sao_ctu_position	0x00bc	W	0x00000000	when there is any error, it is for the position of sao decode output to busifd
hevc_swreg64_performance_cycle	0x0100	W	0x00000000	hevc performnace cycle
hevc_swreg65_axi_ddr_rdata	0x0104	W	0x00000000	axi ddr read data num

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Name	Offset	Size	Reset Value	Description
hevc_swreg66_axi_ddr_wdata	0x0108	W	0x00000000	axi ddr write data num

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

4.4.2 HEVC Detail Register Description

hevc_swreg0_id

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	RO	0x6876	prod_num The ascii code of "hv", which is 0x6876
15	RO	0x0	reserved
14	RW	0x0	codec_flag 0: only dec 1: dec + enc
13	RO	0x0	reserved
12	RW	0x1	profile 0: Main 1: Main10
11:9	RO	0x0	reserved
8	RO	0x1	level 0: FHD 1: UHD
7:0	RO	0x00	minor_ver minor version

hevc_swreg1_int

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31	RW	0x0	sw_auto_reset_en 0:not allow 1:allow
30:23	RO	0x0	reserved
22	RW	0x0	sw_softreset_rdy when it is 1'b1, it says that softreset has been done
21	RW	0x1	sw_force_softreset_valid when sw_force_softreset_valid is 1'b1, sw_softrst_en will always be valid to the system no matter that whether the axi bus is idle; when sw_force_softreset_valid is 1'b0, sw_softrst_en will only be valid when the axi bus is idle.
20	RW	0x0	sw_softrst_en_p softreset enable signal write 1 to soft reset, write 0 invalid puls register
19	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
18	RW	0x0	sw_cabu_end_sta cabac decode end status
17	RW	0x0	sw_colmv_ref_error_sta colmv ref error status when it is 1'b1, it means that inter module read the invalid dpb frame
16	RO	0x0	reserved
15	RW	0x0	sw_dec_timeout_sta When high the decoder has been idling for too long. it will self reset the hardware only when sw_dec_timeout_e is 1'b1, this bit is valid
14	RW	0x0	sw_dec_error_sta when high, an error is found in input data stream decoding. It will self reset the hardware
13	RW	0x0	sw_dec_bus_sta When this bit is high, there is error on the axi bus, it will self reset hardware
12	RW	0x0	sw_dec_rdy_sta when this bit is high, decoder has decoded a picture
11:10	RO	0x0	reserved
9	RW	0x0	sw_dec_irq_raw the raw status of sw_dec_irq,SW should reset this bit after interrupt is handled
8	RO	0x0	sw_dec_irq when high, decoder requests an interrrupt. sw_dec_irq = sw_dec_irq_raw && (sw_dec_irq_dis == 1'b0)
7	RW	0x0	sw_stmerror_waitdecfifo_empty when it is 1'b0, the stream error process will no wait the ca2decfifo empty when it is 1'b1, the stream error process will wait the ca2decfifo empty
6	RO	0x0	reserved
5	RW	0x1	sw_dec_timeout_e If enabled HW may return timeout interrupt in case HW gets stucked while decoding picture.
4	RW	0x0	sw_dec_irq_dis When hight, there are no interrupts concerning decoder from HW. Polling must be used to see the interrupt status
3:2	RO	0x0	reserved
1	RW	0x1	sw_dec_clkgate_e 0 = clock is running for all structures 1 = clock is gated for decoder structures that are not used

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Bit	Attr	Reset Value	Description
0	RW	0x0	sw_dec_e Decoder enable. Setting this bit high will start the decoding operation. HW will reset this when picture is processed or stream error is detected or bus error or time out interrupt is given

hevc_swreg2_sysctrl

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:12	RW	0x00	sw_strm_start_bit exact bit of streamd start word where decoding can be started (asosiates with sw_str_rlc_base)
11	RW	0x0	sw_rlc_mode 0 = HW decodes video from bit stream 1 = HW decodes video from RLC input data
10	RW	0x0	sw_rlc_mode_direct_write cabac decode output direct write enable when this bit is enable , all the module other than cabac and busifd are not work
9	RO	0x0	reserved
8	RW	0x0	sw_out_cbcr_swap 1'b0: cb(u) is in the lower address, cr(v) is in the higher address 1'b1: cb(u) is in the higher address,cr(v) is in the lower address sw_in_cbcr_swap is the same with sw_out_cbcr_swap
7	RW	0x0	sw_out_swap32_e may be used for 64 or 128 bit environment 0 = no swapping of 32 bit words 1 = 32 bit data words are swapped
6	RW	0x0	sw_out_endian 0 = little endian 1 = big endian for litter enadian , a data 0x12345678, 0x78 is stored in lower address, 0x12 is stored in higher address
5	RW	0x0	sw_str_swap64_e may be used for 128 bit environment 0 = no swapping of 64 bit words 1 = 64 bit data words are swapped
4	RW	0x0	sw_str_swap32_e may be used for 64 or 128 bit environment 0 = no swapping of 32 bit words 1 = 32 bit data words are swapped

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Bit	Attr	Reset Value	Description
3	RW	0x0	sw_str_endian 0 = little endian 1 = big endian for litter enadian , a data 0x12345678, 0x78 is stored in lower address, 0x12 is stored in higher address
2	RW	0x0	sw_in_swap64_e may be used for 128 bit environment 0 = no swapping of 64 bit words 1 = 64 bit data words are swapped
1	RW	0x0	sw_in_swap32_e may be used for 64 or 128 bit environment 0 = no swapping of 32 bit words 1 = 32 bit data words are swapped
0	RW	0x0	sw_in_endian 0 = little endian 1 = big endian for litter enadian , a data 0x12345678, 0x78 is stored in lower address, 0x12 is stored in higher address

hevc_swreg3_picpar

Address: Operational Base + offset (0x000c)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:21	RW	0x000	sw_slice_num slice number in a frame (0~199, when it is 0, it real means 1 slice in a frame) just only used for rps read. 2013.11.27 change the meaning from count from 1, so it will be in 1~200 2013.11.30 sw_slice_num max value is change to 600, so sw_slice_num expand to 10bit
20:12	RW	0x000	sw_uv_hor_virstride picture horizontal virtual stride (the unit is 128bit) the max is (4096x1.5 + 128) /16 = 0x188 suggest this register to config to even for advance ddr performance
11:9	RO	0x0	reserved
8:0	RW	0x000	sw_y_hor_virstride picture horizontal virtual stride (the unit is 128bit) the max is (4096x1.5 + 128) /16 = 0x188 suggest this register to config to even for advance ddr performance

hevc_swreg4_strm_rlc_base

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Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_strm_rlc_base when swreg2.sw_rlc_mode =1, it is base address for rlc data when swreg2.sw_rlc_mode =0, it is base address for stream , after a frame is decoded ready or error (stream error , time out , bus error) , it is the last address of the stream the address should 128bit align
3:0	RO	0x0	reserved

hevc_swreg5_stream_rlc_len

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved
26:0	RW	0x0000000	sw_stream_len amount of stream 8bits in the input buffer the max of sw_stream_len : 4096x2304x1.5x1.5 = 0x1440000 128bits unit: 0x1440000/16 = 0x144000 it is count from 0 2013.10.15 change to 23bit for zty's suggestion 2013.10.28, amount of stream data bytes in input buffer. it is count from 1, change to 27bits

hevc_swreg6_cabactbl_base

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_cabactbl_base the base address of cabac table the address should 128bit align
3:0	RO	0x0	reserved

hevc_swreg7_decout_base

Address: Operational Base + offset (0x001c)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_decout_base base address of decoder output picture the address should be 128bit align
3:0	RO	0x0	reserved

hevc_swreg8_y_virstride

Address: Operational Base + offset (0x0020)

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Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:0	RW	0x00000	sw_y_virstride the output picture y virtual stride (the unit is 128bit) the max: (4096x1.5 +128) x 2304 = 0xdc8000 we can know the sw_uvout_base = sw_decout_base + (sw_y_virstride <<4)

hevc_swreg9_yuv_virstride

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:21	RO	0x0	reserved
20:0	RW	0x000000	sw_yuv_virstride the output picture yuv virtual stride (the unit is 128bit) the max : (4096x1.5 +128) x 2304 x1.5 = 0x14ac000 we can know the sw_mvout_base = sw_decout_base + (sw_yuv_virstride <<4)

hevc_swreg10_refer0_base

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_refer0_base base address for reference picture index 0 (the address should be 128bit align)
3:0	RW	0x0	sw_ref_valid_0_3 valid flag for picture index 0 ~3

hevc_swreg11_refer1_base

Address: Operational Base + offset (0x002c)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_refer1_base base address for reference picture index 1 (the address should be 128bit align)
3:0	RW	0x0	sw_ref_valid_4_7 valid flag for picture index 4 ~7

hevc_swreg12_refer2_base

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_refer2_base base address for reference picture index 2 (the address should be 128bit align)
3:0	RW	0x0	sw_ref_valid_8_11 valid flag for picture index 8~11

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hevc_swreg13_refer3_base

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_refer3_base base address for reference picture index 3 (the address should be 128bit align)
3	RO	0x0	reserved
2:0	RW	0x0	sw_ref_valid_12_14 valid flag for picture index 12~14

hevc_swreg14_refer4_base

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_refer4_base base address for reference picture index 4(the address should be 128bit align)
3:0	RO	0x0	reserved

hevc_swreg15_refer5_base

Address: Operational Base + offset (0x003c)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_refer5_base base address for reference picture index 5(the address should be 128bit align)
3:0	RO	0x0	reserved

hevc_swreg16_refer6_base

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_refer6_base base address for reference picture index 6(the address should be 128bit align)
3:0	RO	0x0	reserved

hevc_swreg17_refer7_base

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_refer7_base base address for reference picture index 7(the address should be 128bit align)
3:0	RO	0x0	reserved

hevc_swreg18_refer8_base

Address: Operational Base + offset (0x0048)

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Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_refer8_base base address for reference picture index 8(the address should be 128bit align)
3:0	RO	0x0	reserved

hevc_swreg19_refer9_base

Address: Operational Base + offset (0x004c)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_refer9_base base address for reference picture index 9(the address should be 128bit align)
3:0	RO	0x0	reserved

hevc_swreg20_refer10_base

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_refer10_base base address for reference picture index 10(the address should be 128bit align)
3:0	RO	0x0	reserved

hevc_swreg21_refer11_base

Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_refer11_base base address for reference picture index 11(the address should be 128bit align)
3:0	RO	0x0	reserved

hevc_swreg22_refer12_base

Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_refer12_base base address for reference picture index 12(the address should be 128bit align)
3:0	RO	0x0	reserved

hevc_swreg23_refer13_base

Address: Operational Base + offset (0x005c)

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Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_refer13_base base address for reference picture index 13(the address should be 128bit align)
3:0	RO	0x0	reserved

hevc_swreg24_refer14_base

Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_refer14_base base address for reference picture index 14(the address should be 128bit align)
3:0	RO	0x0	reserved

hevc_swreg25_refer0_poc

Address: Operational Base + offset (0x0064)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer0_poc the poc of reference picture index 0

hevc_swreg26_refer1_poc

Address: Operational Base + offset (0x0068)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer1_poc the poc of reference picture index 1

hevc_swreg27_refer2_poc

Address: Operational Base + offset (0x006c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer2_poc the poc of reference picture index 2

hevc_swreg28_refer3_poc

Address: Operational Base + offset (0x0070)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer3_poc the poc of reference picture index 3

hevc_swreg29_refer4_poc

Address: Operational Base + offset (0x0074)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer4_poc the poc of reference picture index 4

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hevc_swreg30_refer5_poc

Address: Operational Base + offset (0x0078)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer5_poc the poc of reference picture index 5

hevc_swreg31_refer6_poc

Address: Operational Base + offset (0x007c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer6_poc the poc of reference picture index 6

hevc_swreg32_refer7_poc

Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer7_poc the poc of reference picture index 7

hevc_swreg33_refer8_poc

Address: Operational Base + offset (0x0084)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer8_poc the poc of reference picture index 8

hevc_swreg34_refer9_poc

Address: Operational Base + offset (0x0088)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer9_poc the poc of reference picture index 9

hevc_swreg35_refer10_poc

Address: Operational Base + offset (0x008c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer10_poc the poc of reference picture index 10

hevc_swreg36_refer11_poc

Address: Operational Base + offset (0x0090)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer11_poc the poc of reference picture index 11

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hevc_swreg37_refer12_poc
Address: Operational Base + offset (0x0094)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer12_poc the poc of reference picture index 12

hevc_swreg38_refer13_poc
Address: Operational Base + offset (0x0098)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer13_poc the poc of reference picture index 13

hevc_swreg39_refer14_poc
Address: Operational Base + offset (0x009c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_refer14_poc the poc of reference picture index 14

hevc_swreg40_cur_poc
Address: Operational Base + offset (0x00a0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_cur_poc the poc of the cur picture

hevc_swreg41_rlcwrite_base
Address: Operational Base + offset (0x00a4)

Bit	Attr	Reset Value	Description
31:3	RW	0x00000000	sw_rlcwrite_base the base address of rlcwrite(the address should 64bit align) cabac output write to this rlcwrite base address when sw_rlc_mode_direct_write in swreg2_sysctrl is valid
2:0	RO	0x0	reserved

hevc_swreg42_pps_base
Address: Operational Base + offset (0x00a8)

Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_pps_base the base address of pps (the address should 128bit align) it is for storing sps(sequence parameter set) and pps(picture parameter set)
3:0	RO	0x0	reserved

hevc_swreg43_rps_base
Address: Operational Base + offset (0x00ac)

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Bit	Attr	Reset Value	Description
31:4	RW	0x0000000	sw_rps_base rps(reference picture set) base address (the address should 128bit align)
3:0	RO	0x0	reserved

hevc_swreg44_cabac_error_en

Address: Operational Base + offset (0x00b0)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RW	0x0000000	sw_cabac_error_e cabac error enable regs

hevc_swreg45_cabac_error_status

Address: Operational Base + offset (0x00b4)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	sw_colmv_error_ref_picidx when sw_colmv_ref_error_sta is 1'b1, these bits are used for tell which dpb frame is invalid but is read by inter module
27:0	RW	0x0000000	sw_cabac_error_status cabac error status

hevc_swreg46_cabac_error_ctu

Address: Operational Base + offset (0x00b8)

Bit	Attr	Reset Value	Description
31:23	RO	0x0	reserved
22:16	RW	0x40	sw_streamfifo_space2full It is for debug use, to tell the stream fifo space to full
15:8	RW	0x00	sw_cabac_error_ctu_yoffset cabac error ctu yoffset
7:0	RW	0x00	sw_cabac_error_ctu_xoffset cabac error ctu xoffset

hevc_swreg47_sao_ctu_position

Address: Operational Base + offset (0x00bc)

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:16	RW	0x000	sw_saowr_yoffset saowr y offset , its unit is 4 pixels
15:9	RO	0x0	reserved
8:0	RW	0x000	sw_saowr_xoffet saowr x address offset, its unit is 128bit

hevc_swreg64_performance_cycle

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Address: Operational Base + offset (0x0100)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_performance_cycle hevc running cycle if just want to analys a frame performance cycle, should set the register 0 before start a frame

hevc_swreg65_axi_ddr_rdata

Address: Operational Base + offset (0x0104)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_axi_ddr_rdata axi ddr rdata num, the unit is byte

hevc_swreg66_axi_ddr_wdata

Address: Operational Base + offset (0x0108)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_axi_ddr_wdata hevc write data byte num

4.4.3 HEVC MMU Register Summary

Name	Offset	Size	Reset Value	Description
rkvdec_mmu_DTE_ADDR	0x0000	W	0x00000000	MMU current page Table addressIt is only can be written when MMU state is disable or page fault or mmu enable stall state
rkvdec_mmu_STATUS	0x0004	W	0x00000018	MMU status register
rkvdec_mmu_COMMAND	0x0008	W	0x00000000	MMU command register
rkvdec_mmu_PAGE_FAULT_ADDR	0x000c	W	0x00000000	MMU logical address of last page fault
rkvdec_mmu_ZAP_ONE_LINE	0x0010	W	0x00000000	MMU Zap cache line register
rkvdec_mmu_INT_RAWSTAT	0x0014	W	0x00000000	MMU raw interrupt status register
rkvdec_mmu_INT_CLEAR	0x0018	W	0x00000000	MMU raw interrupt status register
rkvdec_mmu_INT_MASK	0x001c	W	0x00000000	MMU raw interrupt status register
rkvdec_mmu_INT_STATUS	0x0020	W	0x00000000	MMU raw interrupt status register
rkvdec_mmu_AUTO_GATING	0x0024	W	0x00000001	mmu auto gating

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

4.4.4 HEVC MMU Detail Register Description

rkvdec_mmu_DTE_ADDR

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MMU_DTE_ADDR mmu dte base addr , the address must be 4kb aligned

rkvdec_mmu_STATUS

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:11	RO	0x0	reserved
10:6	RO	0x00	PAGE_FAULT_BUS_ID Index of master reponsible for last page fault
5	RO	0x0	PAGE_FAULT_IS_WRITE The direction of access for last page fault: 0 = Read 1 = Write
4	RO	0x1	REPLAY_BUFFER_EMPTY The MMU replay buffer is empty
3	RO	0x1	MMU_IDLE The MMU is idle when accesses are being translated and there are no unfinished translated accesses.
2	RO	0x0	STAIL_ACTIVE MMU stall mode currently enabled. The mode is enabled by command
1	RO	0x0	PAGE_FAULT_ACTIVE MMU page fault mode currently enabled . The mode is enabled by command.
0	RO	0x0	PAGING_ENABLED Paging is enabled

rkvdec_mmu_COMMAND

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:3	RO	0x0	reserved
2:0	WO	0x0	MMU_CMD MMU_CMD. This can be: 0: MMU_ENABLE_PAGING 1: MMU_DISABLE_PAGING 2: MMU_ENABLE_STALL 3: MMU_DISABLE_STALL 4: MMU_ZAP_CACHE 5: MMU_PAGE_FAULT_DONE 6: MMU_FORCE_RESET

rkvdec_mmu_PAGE_FAULT_ADDR

Address: Operational Base + offset (0x000c)

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	PAGE_FAULT_ADDR address of last page fault

rkvdec_mmu_ZAP_ONE_LINE

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	MMU_ZAP_ONE_LINE address to be invalidated from the page table cache

rkvdec_mmu_INT_RAWSTAT

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x0	READ_BUS_ERROR read bus error
0	RW	0x0	PAGE_FAULT page fault

rkvdec_mmu_INT_CLEAR

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	WO	0x0	READ_BUS_ERROR read bus error
0	WO	0x0	PAGE_FAULT page fault

rkvdec_mmu_INT_MASK

Address: Operational Base + offset (0x001c)

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x0	READ_BUS_ERROR read bus error enable an interrupt source if the corresponding mask bit is set to 1
0	RW	0x0	PAGE_FAULT page fault enable an interrupt source if the corresponding mask bit is set to 1

rkvdec_mmu_INT_STATUS

Address: Operational Base + offset (0x0020)

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Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RO	0x0	READ_BUS_ERROR read bus error
0	RO	0x0	PAGE_FAULT page fault

rkvdec_mmu_AUTO_GATING

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x1	mmu_auto_gating when it is 1'b1, the mmu will auto gating it self

4.4.5 HEVC CACHE Register Summary

Name	Offset	Size	Reset Value	Description
pref_cache_VERSION	0x0000	W	0xcac20101	VERSION register
pref_cache_SIZE	0x0004	W	0x07100206	L2 cache SIZE
pref_cache_STATUS	0x0008	W	0x00000000	Status register
pref_cache_COMMAND	0x0010	W	0x00000000	Command setting register
pref_cache_CLEAR_PAGE	0x0014	W	0x00000000	clear page register
pref_cache_MAX_READS	0x0018	W	0x0000001c	maximum read register
pref_cache_ENABLE	0x001c	W	0x00000003	enables cacheable accesses and cache read allocation
pref_cache_PERFCNT_SRC0	0x0020	W	0x00000000	performance counter 0 source register
pref_cache_PERFCNT_VAL0	0x0024	W	0x00000000	performance counter 0 value register
pref_cache_PERFCNT_SRC1	0x0028	W	0x00000000	This register holds all the possible source values for Performance Counter 00: total clock cycles1: active clock cycles2: read transactions, master3: word reads, master4: read transactions, slave5: word reads, slave6: read hit, slave7: read misses, slave8: read invalidates, slave9: cacheable read transactions, slave10: bad hit nmber, slave
pref_cache_PERFCNT_VAL1	0x002c	W	0x00000000	performance counter 1 value register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

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4.4.6 HEVC CACHE Detail Register Description

pref_cache_VERSION

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	RO	0xcac2	PRODUCT_ID Field0000 Description
15:8	RO	0x01	VERSION_MAJOR Field0000 Description
7:0	RO	0x01	VERSION_MINOR Field0000 Description

pref_cache_SIZE

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:24	RO	0x07	External_bus_width Log2 external bus width in bits
23:16	RO	0x10	CACHE_SIZE Log2 cache size in bytes for Y channel , its value is 0x10 for UV channel, its value is 0xf
15:8	RO	0x02	ASSOCIATIVITY Log2 associativity
7:0	RO	0x06	LINE_SIZE Log2 line size in bytes

pref_cache_STATUS

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x0	DATA_BUSY set when the cache is busy handling data
0	RW	0x0	CMD_BUSY set when the cache is busy handling commands

pref_cache_COMMAND

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5:4	RW	0x0	sw_addrb_sel 2'b00: to sel b[14:6] 2'b01: to sel b[15:9], b[7:6] 2'b10: to sel b[16:10], b[7:6] 2'b11: to sel b[17:11], b[7:6]

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Bit	Attr	Reset Value	Description
3:0	RW	0x0	COMMAND The possible command is 1 = Clear entire cache

pref_cache_CLEAR_PAGE

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	CLEAR_PAGE writing an address, invlidates all lines in that page from the cache

pref_cache_MAX_READS

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4:0	RW	0x1c	MAX_READS Limit the number of outstanding read transactions to this amount

pref_cache_ENABLE

Address: Operational Base + offset (0x001c)

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4	RW	0x0	sw_cache_linsize 1'b0: the cache line is 32bytes 1'b1: the cache line is 64bytes
3	RW	0x0	sw_cache_clk_disgate cache clk disgate when it is 1'b0, enable cache clk auto clkgating when it is 1'b1, disable cache clk auto clkgating
2	RW	0x0	sw_readbuffer_counter_reject_en default is 1'b0, for enhance cacheable read performnace in readbuffer. 1'b1: normal origin counter reject
1	RW	0x1	permit_cache_read_allocate 1'b1: permit cache read allocate
0	RW	0x1	permit_cacheable_access 1'b1: permit cacheable access

pref_cache_PERFCNT_SRC0

Address: Operational Base + offset (0x0020)

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Bit	Attr	Reset Value	Description
31:7	RO	0x0	reserved
6:0	RW	0x00	PERFCNT_SRC0 This register holds all the possible source values for Performance Counter 0 0: disabled 1: total clock cycles 2: active clock cycles 3: read transactions, master 4: word reads, master 5: read transactions, slave 6: word reads, slave 7: read hit, slave 8: read misses, slave 9: read invalidates, slave 10: cacheable read transactions, slave 11: bad hit nmber, slave

pref_cache_PERFCNT_VAL0

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PERFCNT_VAL0 Performance counter 0 value

pref_cache_PERFCNT_SRC1

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:7	RO	0x0	reserved
6:0	RW	0x00	PERFCNT_SRC1 This register holds all the possible source values for Performance Counter 1 0: disabled 1: total clock cycles 2: active clock cycles 3: read transactions, master 4: word reads, master 5: read transactions, slave 6: word reads, slave 7: read hit, slave 8: read misses, slave 9: read invalidates, slave 10: cacheable read transactions, slave 11: bad hit nmber, slave

pref_cache_PERFCNT_VAL1

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Address: Operational Base + offset (0x002c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PERFCNT_VAL1 Performance counter 1 value

4.4.7 VEPU121 Register Summary

Name	Offset	Size	Reset Value	Description
VEPU_swreg_0	0x0000	W	0x00000000	1st quantization for jpeg lumin table
VEPU_swreg_1	0x0004	W	0x00000000	2st quantization for jpeg lumin table
VEPU_swreg_2	0x0008	W	0x00000000	3st quantization for jpeg lumin table
VEPU_swreg_3	0x000c	W	0x00000000	4st quantization for jpeg lumin table
VEPU_swreg_4	0x0010	W	0x00000000	5st quantization for jpeg lumin table
VEPU_swreg_5	0x0014	W	0x00000000	6st quantization for jpeg lumin table/part 1 for qp round
VEPU_swreg_6	0x0018	W	0x00000000	7st quantization for jpeg lumin table
VEPU_swreg_7	0x001c	W	0x00000000	8st quantization for jpeg lumin table
VEPU_swreg_8	0x0020	W	0x00000000	9st quantization for jpeg lumin table
VEPU_swreg_9	0x0024	W	0x00000000	10st quantization for jpeg lumin table
VEPU_swreg_10	0x0028	W	0x00000000	11st quantization for jpeg lumin table
VEPU_swreg_11	0x002c	W	0x00000000	12st quantization for jpeg lumin table

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Name	Offset	Size	Reset Value	Description
VEPU_swreg_12	0x0030	W	0x00000000	13st quantization for jpeg lumin table
VEPU_swreg_13	0x0034	W	0x00000000	14st quantization for jpeg lumin table
VEPU_swreg_14	0x0038	W	0x00000000	15st quantization for jpeg lumin table
VEPU_swreg_15	0x003c	W	0x00000000	16st quantization for jpeg lumin table
VEPU_swreg_16	0x0040	W	0x00000000	1st quantization for jpeg chroma table
VEPU_swreg_17	0x0044	W	0x00000000	2st quantization for jpeg chroma table
VEPU_swreg_18	0x0048	W	0x00000000	3st quantization for jpeg chroma table
VEPU_swreg_19	0x004c	W	0x00000000	4st quantization for jpeg chroma table
VEPU_swreg_20	0x0050	W	0x00000000	5st quantization for jpeg chroma table
VEPU_swreg_21	0x0054	W	0x00000000	6st quantization for jpeg chroma table
VEPU_swreg_22	0x0058	W	0x00000000	7st quantization for jpeg chroma table
VEPU_swreg_23	0x005c	W	0x00000000	8st quantization for jpeg chroma table/part 3 for qp round
VEPU_swreg_24	0x0060	W	0x00000000	9st quantization for jpeg chroma table
VEPU_swreg_25	0x0064	W	0x00000000	10st quantization for jpeg chroma table

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Name	Offset	Size	Reset Value	Description
VEPU_swreg_26	0x0068	W	0x00000000	11st quantization for jpeg chroma table
VEPU_swreg_27	0x006c	W	0x00000000	12st quantization for jpeg chroma
VEPU_swreg_28	0x0070	W	0x00000000	13st quantization for jpeg chroma
VEPU_swreg_29	0x0074	W	0x00000000	14st quantization for jpeg chroma
VEPU_swreg_30	0x0078	W	0x00000000	15st quantization for jpeg chroma
VEPU_swreg_31	0x007c	W	0x00000000	16st quantization for jpeg chroma
VEPU_swreg_44	0x00b0	W	0x00000000	Intra slice bitmap
VEPU_swreg_45	0x00b4	W	0x00000000	Intra slice bitmap1
VEPU_swreg_46	0x00b8	W	0x00000000	intra macro block sellect register
VEPU_swreg_47	0x00bc	W	0x00000000	CIR intra control register
VEPU_swreg_48	0x00c0	W	0x00000000	base addr for input luma
VEPU_swreg_49	0x00c4	W	0x00000000	base address for input cb
VEPU_swreg_50	0x00c8	W	0x00000000	input cr start address
VEPU_swreg_51	0x00cc	W	0x00000000	stream header bits left register
VEPU_swreg_52	0x00d0	W	0x00000000	stream header bits left register
VEPU_swreg_53	0x00d4	W	0x00000000	stream buffer register
VEPU_swreg_54	0x00d8	W	0x01010000	axi control register
VEPU_swreg_55	0x00dc	W	0x00000000	qp related

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Name	Offset	Size	Reset Value	Description
VEPU_swreg_56	0x00e0	W	0x00000000	the luma reference frame start address
VEPU_swreg_57	0x00e4	W	0x00000000	the chroma reference frame start address
VEPU_swreg_58	0x00e8	W	0x00000000	the result of qp sum div2
VEPU_swreg_59	0x00ec	W	0x00000000	h264 slice ctrl
VEPU_swreg_60	0x00f0	W	0x00000000	spill ctrl
VEPU_swreg_61	0x00f4	W	0x00000000	input luminance information
VEPU_swreg_62	0x00f8	W	0x00000000	rlc_sum
VEPU_swreg_63	0x00fc	W	0x00000000	the reconstructed luma start address
VEPU_swreg_64	0x0100	W	0x00000000	the reconstructed chroma start address
VEPU_swreg_65_reuse	0x0104	W	0x00000000	checkpoint 1 and 2
VEPU_swreg_66_reuse	0x0108	W	0x00000000	checkpoint 3 and 4
VEPU_swreg_67_reuse	0x010c	W	0x00000000	checkpoint 5 and 6
VEPU_swreg_68_reuse	0x0110	W	0x00000000	checkpoint 7 and 8
VEPU_swreg_69_reuse	0x0114	W	0x00000000	checkpoint 9 and 10
VEPU_swreg_70_reuse	0x0118	W	0x00000000	checkpoint word error 1 and 2
VEPU_swreg_71_reuse	0x011c	W	0x00000000	checkpoint word error 1 and 2
VEPU_swreg_72_reuse	0x0120	W	0x00000000	checkpoint word error 1 and 2
VEPU_swreg_73_reuse	0x0124	W	0x00000000	checkpoint delta QP register
VEPU_swreg_74	0x0128	W	0x00000000	input image format
VEPU_swreg_75	0x012c	W	0x00000000	intra/inter mode

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Name	Offset	Size	Reset Value	Description
VEPU_swreg_76_reuse	0x0130	W	0x00000000	encoder control regsiter 0
VEPU_swreg_77	0x0134	W	0x00000000	output stream start address
VEPU_swreg_78	0x0138	W	0x00000000	output control start address
VEPU_swreg_79	0x013c	W	0x00000000	next picture luminance start address
VEPU_swreg_80	0x0140	W	0x00000000	Base address for MV output
VEPU_swreg_81	0x0144	W	0x00000000	the cabac table start address
VEPU_swreg_82	0x0148	W	0x00000000	ROI area register
VEPU_swreg_83	0x014c	W	0x00000000	the second of ROI area register
VEPU_swreg_84	0x0150	W	0x00000000	Stabilization matrix1
VEPU_swreg_85	0x0154	W	0x00000000	Stabilization matrix2
VEPU_swreg_86	0x0158	W	0x00000000	Stabilization matrix3
VEPU_swreg_87	0x015c	W	0x00000000	Stabilization matrix4
VEPU_swreg_88	0x0160	W	0x00000000	Stabilization matrix5
VEPU_swreg_89	0x0164	W	0x00000000	Stabilization matrix6
VEPU_swreg_90	0x0168	W	0x00000000	Stabilization matrix7
VEPU_swreg_91	0x016c	W	0x00000000	Stabilization matrix8
VEPU_swreg_92	0x0170	W	0x00000000	Stabilization matrix9
VEPU_swreg_93	0x0174	W	0x00000000	the output of Stabilization motion sum
VEPU_swreg_94	0x0178	W	0x00000000	output of Stabilization
VEPU_swreg_95	0x017c	W	0x00000000	RGB to YUV conversion coefficient register

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Name	Offset	Size	Reset Value	Description
VEPU_swreg_96	0x0180	W	0x00000000	RGB to YUV conversion coefficient register
VEPU_swreg_97	0x0184	W	0x00000000	RGB to YUV conversion coefficient register
VEPU_swreg_98	0x0188	W	0x00000000	RGA MASK
VEPU_swreg_99	0x018c	W	0x00000000	mv related
VEPU_swreg_100_reuse	0x0190	W	0x00000000	QP register
VEPU_swreg_101_read	0x0194	W	0x1f522780	hw config reg
VEPU_swreg_102	0x0198	W	0x00000000	mvc related
VEPU_swreg_103	0x019c	W	0x00000000	encoder start
VEPU_swreg_104	0x01a0	W	0x00000000	mb control register
VEPU_swreg_105	0x01a4	W	0x00000000	swap ctrl register
VEPU_swreg_106_reuse	0x01a8	W	0x00000000	encoder control register 1
VEPU_swreg_107_reuse	0x01ac	W	0x00000000	JPEG control regsiter
VEPU_swreg_108_reuse	0x01b0	W	0x00000000	intra slice bmp2
VEPU_swreg_109	0x01b4	W	0x00001000	encoder status
VEPU_swreg_110_read	0x01b8	W	0x48311220	product ID
VEPU_swreg_120_183	0x01e0	W	0x00000000	addr range : 0x01e0~0x02dcswreg120: DMV 4p/1p penalty table valuesswreg121: DMV 4p/1p penalty table valuesswreg122: DMV 4p/1p penalty table valuesswreg123: DMV 4p/1p penalty table values.....swreg183: DMV 4p/1p penalty table values

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

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4.4.8 VEPU121 Detail Register Description

VEPU_swreg_0

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	vp8_pt1_qut_dc_y2 part 1 for qp quant dc y2
15:14	RO	0x0	reserved
13:0	RW	0x0000	vp8_pt1_qut_dc_y1 part1 for qp quant dc y1

VEPU_swreg_1

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	vp8_pt1_qut_ac_y1 part 1 for qp quant ac y1
15:14	RO	0x0	reserved
13:0	RW	0x0000	vp8_pt1_qut_dc_ch part 1 for qp quant dc chroma

VEPU_swreg_2

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	vp8_pt1_qut_ac_ch part 1 for qp quant ac chroma
15:14	RO	0x0	reserved
13:0	RW	0x0000	vp8_pt1_qut_ac_y2 part 1 for qp quant ac y2

VEPU_swreg_3

Address: Operational Base + offset (0x000c)

Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved
26:18	RW	0x000	vp8_pt1_zb_dc_ch part 1 for qp zbin dc chroma
17:9	RW	0x000	vp8_pt1_zb_dc_y2 part 1 for qp zbin dc y2
8:0	RW	0x000	vp8_pt1_zb_dc_y1 part 1 for qp zbin dc y1

VEPU_swreg_4

Address: Operational Base + offset (0x0010)

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Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved
26:18	RW	0x000	vp8_pt1_zb_ac_ch part 1 for qp zbin ac chroma
17:9	RW	0x000	vp8_pt1_zb_ac_y2 part 1 for qp zbin ac y2
8:0	RW	0x000	vp8_pt1_zb_ac_y1 part 1 for qp zbin ac y1

VEPU_swreg_5

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:16	RW	0x00	vp8_pt1_rnd_dc_ch part 1 for qp round dc chroma
15:8	RW	0x00	vp8_pt1_rnd_dc_y2 part 1 for qp round dc y2
7:0	RW	0x00	vp8_pt1_rnd_dc_y1 part 1 for qp round dc y1

VEPU_swreg_6

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:16	RW	0x00	vp8_pt1_rnd_ac_ch part 1 for qp round ac chroma
15:8	RW	0x00	vp8_pt1_rnd_ac_y2 part 1 for qp round ac y2
7:0	RW	0x00	vp8_pt1_rnd_ac_y1 part 1 for qp round ac y1

VEPU_swreg_7

Address: Operational Base + offset (0x001c)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:25	RW	0x00	vp8_pt1_filter_sel VP8 part1 filter select
24:17	RW	0x00	vp8_pt1_dequt_dc_ch part 1 for qp dequnt dc chroma
16:8	RW	0x000	vp8_pt1_deqnt_dc_y2 part 1 for qp dequnt dc y2
7:0	RW	0x00	vp8_pt1_dequt_dc_y1 part 1 for qp dequnt dc y1

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VEPU_swreg_8
Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved
26:18	RW	0x000	vp8_pt1_dequt_ac_ch part 1 for qp dequnt ac chroma
17:9	RW	0x000	vp8_pt1_dequt_ac_y2 part 1 for qp dequnt ac y2
8:0	RW	0x000	vp8_pt1_dequt_ac_y1 part 1 for qp dequnt ac y1

VEPU_swreg_9
Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	vp8_pt2_qut_dc_y2 part 2 for qp quant dc y2
15:14	RO	0x0	reserved
13:0	RW	0x0000	vp8_pt2_qut_dc_y1 part2 for qp quant dc y1

VEPU_swreg_10
Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	vp8_pt2_qut_ac_y1 part 2 for qp quant ac y1
15:14	RO	0x0	reserved
13:0	RW	0x0000	vp8_pt2_qut_dc_ch part 2 for qp quant dc chroma

VEPU_swreg_11
Address: Operational Base + offset (0x002c)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	vp8_pt2_qut_ac_ch part 2 for qp quant ac chroma
15:14	RO	0x0	reserved
13:0	RW	0x0000	vp8_pt2_qut_ac_y2 part 2 for qp quant ac y2

VEPU_swreg_12
Address: Operational Base + offset (0x0030)

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Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved
26:18	RW	0x000	vp8_pt2_zb_dc_ch part 2 for qp zbin dc chroma
17:9	RW	0x000	vp8_pt2_zb_dc_y2 part 2 for qp zbin dc y2
8:0	RW	0x000	vp8_pt2_zb_dc_y1 part 2 for qp zbin dc y1

VEPU_swreg_13

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved
26:18	RW	0x000	vp8_pt2_zb_ac_ch part 2 for qp zbin ac chroma
17:9	RW	0x000	vp8_pt2_zb_ac_y2 part 2 for qp zbin ac y2
8:0	RW	0x000	vp8_pt2_zb_ac_y1 part2 for qp zbin ac y1

VEPU_swreg_14

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:16	RW	0x00	vp8_pt2_rnd_dc_ch part 2 for qp round dc chroma
15:8	RW	0x00	vp8_pt2_rnd_dc_y2 part 2 for qp round dc y2
7:0	RW	0x00	vp8_pt2_rnd_dc_y1 part 2 for qp round dc y1

VEPU_swreg_15

Address: Operational Base + offset (0x003c)

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:16	RW	0x00	vp8_pt2_rnd_ac_ch part 2 for qp round ac chroma
15:8	RW	0x00	vp8_pt2_rnd_ac_y2 part 2 for qp round ac y2
7:0	RW	0x00	vp8_pt2_rnd_ac_y1 part 2 for qp round ac y1

VEPU_swreg_16

Address: Operational Base + offset (0x0040)

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Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:25	RW	0x00	vp8_pt2_filter_sel VP8 part2 filter select
24:17	RW	0x00	vp8_pt2_dequt_dc_ch part2 for qp dequnt dc chroma
16:8	RW	0x000	vp8_pt2_deqnt_dc_y2 part 2 for qp dequnt dc y2
7:0	RW	0x00	vp8_pt2_dequt_dc_y1 part 2 for qp dequnt dc y1

VEPU_swreg_17

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved
26:18	RW	0x000	vp8_pt2dequt_ac_ch part 2 for qp dequnt ac chroma
17:9	RW	0x000	vp8_pt2_dequt_ac_y2 part 2 for qp dequnt ac y2
8:0	RW	0x000	vp8_pt2_dequt_ac_y1 part2 for qp dequnt ac y1

VEPU_swreg_18

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	vp8_pt3_qut_dc_y2 part 3 for qp quant dc y2
15:14	RO	0x0	reserved
13:0	RW	0x0000	vp8_pt3_qut_dc_y1 part3 for qp quant dc y1

VEPU_swreg_19

Address: Operational Base + offset (0x004c)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	vp8_pt3_qut_ac_y1 part 3 for qp quant ac y1
15:14	RO	0x0	reserved
13:0	RW	0x0000	vp8_pt3_qut_dc_ch part 3 for qp quant dc chroma

VEPU_swreg_20

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Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	vp8_pt3_qut_ac_ch part 3 for qp quant ac chroma
15:14	RO	0x0	reserved
13:0	RW	0x0000	vp8_pt3_qut_ac_y2 part 3 for qp quant ac y2

VEPU_swreg_21

Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved
26:18	RW	0x000	vp8_pt3_zb_dc_ch part 3 for qp zbin dc chroma
17:9	RW	0x000	vp8_pt3_zb_dc_y2 part 3 for qp zbin dc y2
8:0	RW	0x000	vp8_pt3_zb_dc_y1 part 3 for qp zbin dc y1

VEPU_swreg_22

Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved
26:18	RW	0x000	vp8_pt3_zb_ac_ch part 3 for qp zbin ac chroma
17:9	RW	0x000	vp8_pt3_zb_ac_y2 part 3 for qp zbin ac y2
8:0	RW	0x000	vp8_pt3_zb_ac_y1 part 3 for qp zbin ac y1

VEPU_swreg_23

Address: Operational Base + offset (0x005c)

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:16	RW	0x00	vp8_pt3_rnd_dc_ch part 3 for qp round dc chroma
15:8	RW	0x00	vp8_pt3_rnd_dc_y2 part 3 for qp round dc y2
7:0	RW	0x00	vp8_pt3_rnd_dc_y1 part 3 for qp round dc y1

VEPU_swreg_24

Address: Operational Base + offset (0x0060)

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Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:16	RW	0x00	vp8_pt3_rnd_ac_ch part 3 for qp round ac chroma
15:8	RW	0x00	vp8_pt3_rnd_ac_y2 part 3 for qp round ac y2
7:0	RW	0x00	vp8_pt3_rnd_ac_y1 part 3 for qp round ac y1

VEPU_swreg_25

Address: Operational Base + offset (0x0064)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:25	RW	0x00	vp8_pt3_filter_sel VP8 part3 filter select
24:17	RW	0x00	vp8_pt3_dequt_dc_ch part 3 for qp dequnt dc chroma
16:8	RW	0x000	vp8_pt3_deqnt_dc_y2 part 3 for qp dequnt dc y2
7:0	RW	0x00	vp8_pt3_dequt_dc_y1 part 3 for qp dequnt dc y1

VEPU_swreg_26

Address: Operational Base + offset (0x0068)

Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved
26:18	RW	0x000	vp8_pt3_dequt_ac_ch part 3 for qp dequnt ac chroma
17:9	RW	0x000	vp8_pt3_dequt_ac_y2 part 3 for qp dequnt ac y2
8:0	RW	0x000	vp8_pt3_dequt_ac_y1 part 3 for qp dequnt ac y1

VEPU_swreg_27

Address: Operational Base + offset (0x006c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	vp8_seg_st_adres 11st quantization for jpeg chr/ VP8 segment start address

VEPU_swreg_28

Address: Operational Base + offset (0x0070)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
27:16	RW	0x000	vp8_imp_4x4_1 VP8 intra penalty for 4x4 1st sel
15:12	RO	0x0	reserved
11:0	RW	0x000	vp8_imp_4x4_0 VP8 intra penalty for 4x4 0st sel

VEPU_swreg_29

Address: Operational Base + offset (0x0074)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	vp8_imp_4x4_3 VP8 intra penalty for 4x4 3st sel
15:12	RO	0x0	reserved
11:0	RW	0x000	vp8_imp_4x4_2 VP8 intra penalty for 4x4 2st sel

VEPU_swreg_30

Address: Operational Base + offset (0x0078)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	vp8_imp_4x4_5 VP8 intra penalty for 4x4 5st sel
15:12	RO	0x0	reserved
11:0	RW	0x000	vp8_imp_4x4_4 VP8 intra penalty for 4x4 4st sel

VEPU_swreg_31

Address: Operational Base + offset (0x007c)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	vp8_imp_4x4_7 VP8 intra penalty for 4x4 7st sel
15:12	RO	0x0	reserved
11:0	RW	0x000	vp8_imp_4x4_6 VP8 intra penalty for 4x4 6st sel

VEPU_swreg_32

Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	vp8_imp_4x4_9 VP8 intra penalty for 4x4 9st sel
15:12	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
11:0	RW	0x000	vp8_imp_4x4_8 VP8 intra penalty for 4x4 8st sel

VEPU_swreg_33

Address: Operational Base + offset (0x0084)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	vp8_imp_16x16_1 VP8 intra penalty for 16x16 1st sel
15:12	RO	0x0	reserved
11:0	RW	0x000	vp8_imp_16x16_0 VP8 intra penalty for 16x16 0st sel

VEPU_swreg_34

Address: Operational Base + offset (0x0088)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	vp8_imp_16x16_3 VP8 intra penalty for 16x16 3st sel
15:12	RO	0x0	reserved
11:0	RW	0x000	vp8_imp_16x16_2 VP8 intra penalty for 16x16 2st sel

VEPU_swreg_40

Address: Operational Base + offset (0x00a0)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x00	vp8_lpf_bpred The bpred of loop filter for vp8
23	RO	0x0	reserved
22:16	RW	0x00	vp8_lpf_intra The intra macro block of loop filter for vp8
15:12	RO	0x0	reserved
11:0	RW	0x000	vp8_inter_type inter type for vp8

VEPU_swreg_41

Address: Operational Base + offset (0x00a4)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	vp8_coef_dmv_ply The coefficient of dmv penalty for VP8
15:12	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
11:0	RW	0x000	vp8_ref_frame The reference frame for vp8

VEPU_swreg_42

Address: Operational Base + offset (0x00a8)

Bit	Attr	Reset Value	Description
31:23	RO	0x0	reserved
22:16	RW	0x00	vp8_lpf_altref loop filter for alt reference frame
15	RO	0x0	reserved
14:8	RW	0x00	vp8_lpf_lastref loop filter for last reference frame
7	RO	0x0	reserved
6:0	RW	0x00	vp8_lpf_orgref loop filter for reference frame

VEPU_swreg_43

Address: Operational Base + offset (0x00ac)

Bit	Attr	Reset Value	Description
31:23	RO	0x0	reserved
22:16	RW	0x00	vp8_lpf_divmv loop filter for divide mv used in vp8
15	RO	0x0	reserved
14:8	RW	0x00	vp8_lpf_zeromv loop filter for zero mv used in vp8
7	RO	0x0	reserved
6:0	RW	0x00	vp8_lpf_newmv loop filter for new mv used in vp8

VEPU_swreg_44

Address: Operational Base + offset (0x00b0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	intra_slice_bmp0 bit0 : slices0 bit1 : slices1 bit2 : slices2 ..... bit31 : slices31

VEPU_swreg_45

Address: Operational Base + offset (0x00b4)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	intra_slice_bmp1 bit0 : slices32 bit1 : slices33 bit2 : slices34 ..... bit31 : slices63

VEPU_swreg_46

Address: Operational Base + offset (0x00b8)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	intra_up_mb_area The top intra macro block's area used in row
23:16	RW	0x00	intra_down_mb_area The bottom intra macro block's area used in row
15:8	RW	0x00	intra_left_mb_area The left intra macro block's area used in column
7:0	RW	0x00	intra_right_mb_area The right intra macro block's area used in column

VEPU_swreg_47

Address: Operational Base + offset (0x00bc)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	cir_first_intra 0:disable other:enable and be set
15:0	RW	0x0000	cir_intra_mb_itvl 0: disable other: enable and be set

VEPU_swreg_48

Address: Operational Base + offset (0x00c0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	luma_in_st_adr input luma start address

VEPU_swreg_49

Address: Operational Base + offset (0x00c4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	cb_in_st_adr input cb start address

VEPU_swreg_50

Address: Operational Base + offset (0x00c8)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	cr_in_st_adr input cr start address

VEPU_swreg_51

Address: Operational Base + offset (0x00cc)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	strm_header_left_hbits the high 32 bit of stram header be left

VEPU_swreg_52

Address: Operational Base + offset (0x00d0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	strm_header_left_lbits the low 32 bit of stram header be left

VEPU_swreg_53

Address: Operational Base + offset (0x00d4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	strm_bufsize_lmt the limit size of steam buffer

VEPU_swreg_54

Address: Operational Base + offset (0x00d8)

Bit	Attr	Reset Value	Description
31:24	RW	0x01	axi_rd_id if config 0,it will be modify as 1 by HW auto
23:16	RW	0x01	axi_wr_id if config 0,it will be modify as 1 by HW auto
15:14	RO	0x0	reserved
13:8	RW	0x00	burst_len burst length
7:3	RO	0x0	reserved
2	RW	0x0	burst_incr_mod_sel 0: single burst selected 1: incr burst selected
1	RW	0x0	burst_discard 0:disable ,off 1:enable,on
0	RW	0x0	burst_disable 0: enable 1:disable

VEPU_swreg_55

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Address: Operational Base + offset (0x00dc)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:12	RW	0x0	roi_dlt_qp1 1st for delta qp for roi
11:8	RW	0x0	roi_dlt_qp2 2st for delta qp for roi
7:4	RO	0x0	reserved
3:0	RW	0x0	qp_adjst signed register; range from -8 to 7

VEPU_swreg_56

Address: Operational Base + offset (0x00e0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	luma_ref_st_adr the luma reference frame start address

VEPU_swreg_57

Address: Operational Base + offset (0x00e4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	chroma_ref_st_adr the chroma reference frame start address

VEPU_swreg_58

Address: Operational Base + offset (0x00e8)

Bit	Attr	Reset Value	Description
31:11	RW	0x000000	qp_sum_div2 the result of (qp sum)/2
10:0	RO	0x0	reserved

VEPU_swreg_59

Address: Operational Base + offset (0x00ec)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28	RW	0x0	h264_qurt_pixmv_dis 1:disable 0:default,enable
27:26	RO	0x0	reserved
25:24	RW	0x0	dblking_flt_mode 0 : enabled 1 : disabled 2 : disabled on slice (vp8=simple)
23	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
22:21	RW	0x0	h264_cabac_idc 0,1,2: used 3:no use
20	RW	0x0	entry_code_fmt h.264: 0: cavlc 1: cabac VP8:boolenc enable
19:18	RO	0x0	reserved
17	RW	0x0	h264_trfmod_8x8 on-off for 8x8 transform used in h264
16	RW	0x0	h264_res_intermod_4x4 the restriction inter mode selected in 4x4 block
15	RW	0x0	h264_strm_mod_sel 0 : NAL unit ; 1 : BYTE
14:8	RW	0x00	h264_slice_num 0=one slice in currect picture 1=two slice in currect picture .....
7:0	RO	0x0	reserved

VEPU_swreg_60

Address: Operational Base + offset (0x00f0)

Bit	Attr	Reset Value	Description
31:22	RO	0x0	reserved
21:16	RW	0x00	strm_st_offset
15:8	RW	0x00	skip_mb_mode H.264:SKIP macroblock mode VP8 :zero/nearest/near mode penalty
7:6	RO	0x0	reserved
5:4	RW	0x0	right_spill div4 value range:0~3
3:0	RW	0x0	bot_spill the bottom edge of image for spill pixels

VEPU_swreg_61

Address: Operational Base + offset (0x00f4)

Bit	Attr	Reset Value	Description
31:23	RO	0x0	reserved
22:20	RW	0x0	offset_in_chroma byte unit

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Bit	Attr	Reset Value	Description
19	RO	0x0	reserved
18:16	RW	0x0	offset_in_luma byte unit
15:14	RO	0x0	reserved
13:0	RW	0x0000	row_len_in_luma

VEPU_swreg_62

Address: Operational Base + offset (0x00f8)

Bit	Attr	Reset Value	Description
31:22	RO	0x0	reserved
21:0	RW	0x000000	rlc_sum rlc_sum

VEPU_swreg_63

Address: Operational Base + offset (0x00fc)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	recon_luma_st_adr the reconstructed luma start address

VEPU_swreg_64

Address: Operational Base + offset (0x0100)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	recon_chroma_st_adr the reconstructed chroma start address

VEPU_swreg_65_reuse

Address: Operational Base + offset (0x0104)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	h264_chkpt_1 1st word used for check point used in h.264
15:0	RW	0x0000	h264_chkpt_2 2st word used for check point used in h.264

VEPU_swreg_66_reuse

Address: Operational Base + offset (0x0108)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	h264_chkpt_3 3st word used for check point used in h.264
15:0	RW	0x0000	h264_chkpt_4 4st word used for check point used in h.264

VEPU_swreg_67_reuse

Address: Operational Base + offset (0x010c)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	h264_chkpt_5 5st word used for check point used in h.264
15:0	RW	0x0000	h264_chkpt_6 6st word used for check point used in h.264

VEPU_swreg_68_reuse

Address: Operational Base + offset (0x0110)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	h264_chkpt_7 7st word used for check point used in h.264
15:0	RW	0x0000	h264_chkpt_8 8st word used for check point used in h.264

VEPU_swreg_69_reuse

Address: Operational Base + offset (0x0114)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	h264_chkpt_9 9st word used for check point used in h.264
15:0	RW	0x0000	h264_chkpt_10 10st word used for check point used in h.264

VEPU_swreg_70_reuse

Address: Operational Base + offset (0x0118)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	h264_errchkpt_1 1st word error check point used in h.264
15:0	RW	0x0000	h264_errchkpt_2 2st word error check point used in h.264

VEPU_swreg_71_reuse

Address: Operational Base + offset (0x011c)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	h264_errchkpt_3 3st word error check point used in h.264
15:0	RW	0x0000	h264_errchkpt_4 4st word error check point used in h.264

VEPU_swreg_72_reuse

Address: Operational Base + offset (0x0120)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	h264_errchkpt_5 5st word error check point used in h.264

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Bit	Attr	Reset Value	Description
15:0	RW	0x0000	h264_errchkpt_6 6st word error check point used in h.264

VEPU_swreg_73_reuse

Address: Operational Base + offset (0x0124)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:24	RW	0x0	chkqp_1 1st for delta qp check point
23:20	RW	0x0	chkqp_2 2st for delta qp check point
19:16	RW	0x0	chkqp_3 3st for delta qp check point
15:12	RW	0x0	chkqp_4 4st for delta qp check point
11:8	RW	0x0	chkqp_5 5st for delta qp check point
7:4	RW	0x0	chkqp_6 6st for delta qp check point
3:0	RW	0x0	chkqp_7 7st for delta qp check point

VEPU_swreg_74

Address: Operational Base + offset (0x0128)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RW	0x00	mad_thsld value = (MAD threshold)/256
23:16	RW	0x00	encodered_slices the number of encoder slices which used in h.264
15:8	RO	0x0	reserved
7:4	RW	0x0	img_fmt_in YUV420P YUV420SP YUV422 UYVY422 RGB565 RGB444 RGB888 RGB101010
3:2	RW	0x0	img_in_rot 0 : no rotation 1 : rotate right 90 degress 2 : rotate left 90 degress

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Bit	Attr	Reset Value	Description
1	RO	0x0	reserved
0	RW	0x0	nal_mode the output of NAL size to base control

VEPU_swreg_75

Address: Operational Base + offset (0x012c)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	intramod_16x16
15:0	RW	0x0000	intermod the intra/inter selection for inter macro block mode favor

VEPU_swreg_76_reuse

Address: Operational Base + offset (0x0130)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	pps_init_qp pps init qp in picture used in h264 range : 0~51
25:22	RW	0x0	slice_flt_alpha offset div2 range : -6~6
21:18	RW	0x0	slice_flt_beta config value = (real value)/2 signed register range : -6 ~6
17:13	RW	0x00	qp_offset_ch signed register range : -12~12
12:9	RO	0x0	reserved
8	RW	0x0	sw_qpass
7:5	RO	0x0	reserved
4:1	RW	0x0	idr_picid IDR pic ID
0	RW	0x0	constr_intra_pred constrained intra prediction

VEPU_swreg_77

Address: Operational Base + offset (0x0134)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	output_strm_st_adr output stream start address

VEPU_swreg_78

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Address: Operational Base + offset (0x0138)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	output_ctrl_st_adr output control start address

VEPU_swreg_79

Address: Operational Base + offset (0x013c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	next_luma_st_adr next picture luminance start address

VEPU_swreg_80

Address: Operational Base + offset (0x0140)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mv_out_st_adr

VEPU_swreg_81

Address: Operational Base + offset (0x0144)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	cabac_table_st_adr H264: cabac table VP8 : probability tables

VEPU_swreg_82

Address: Operational Base + offset (0x0148)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	first_roi_tmb (inside area)
23:16	RW	0x00	first_roi_bmb (outside area)
15:8	RW	0x00	first_roi_lmb qp=qp + roi1_Delta_Qp (inside area)
7:0	RW	0x00	first_roi_rmb qp=qp - roi1_Delta_Qp (outside area)

VEPU_swreg_83

Address: Operational Base + offset (0x014c)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	second_roi_rmb (inside area)
23:16	RW	0x00	second_roi_bmb (outside area)

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Bit	Attr	Reset Value	Description
15:8	RW	0x00	second_roi_lmb qp=qp + roi1_Delta_Qp (inside area)
7:0	RW	0x00	second_roi_tmb qp=qp - roi1_Delta_Qp (outside area)

VEPU_swreg_84

Address: Operational Base + offset (0x0150)

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:0	RW	0x000000	stab_matrix1 (position@ up-left)

VEPU_swreg_85

Address: Operational Base + offset (0x0154)

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:0	RW	0x000000	stab_matrix2 (position @ up)

VEPU_swreg_86

Address: Operational Base + offset (0x0158)

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:0	RW	0x000000	stab_matrix3 (position @up-right)

VEPU_swreg_87

Address: Operational Base + offset (0x015c)

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:0	RW	0x000000	stab_matrix4 (position @ left)

VEPU_swreg_88

Address: Operational Base + offset (0x0160)

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:0	RW	0x000000	stab_matrix5 (position @GMV)

VEPU_swreg_89

Address: Operational Base + offset (0x0164)

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:0	RW	0x000000	stab_matrix6 (position@right)

VEPU_swreg_90

Address: Operational Base + offset (0x0168)

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:0	RW	0x000000	stab_matrix7 (position@down-left)

VEPU_swreg_91

Address: Operational Base + offset (0x016c)

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:0	RW	0x000000	stab_matrix8 (position@down)

VEPU_swreg_92

Address: Operational Base + offset (0x0170)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	stab_gmv_vrtl signed register range : -16~16
25:24	RO	0x0	reserved
23:0	RW	0x000000	stab_matrix9 (position@down- right)

VEPU_swreg_93

Address: Operational Base + offset (0x0174)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	stab_motion_sum read value = (real value)/8 range : 0~1089*253*255*53/8

VEPU_swreg_94

Address: Operational Base + offset (0x0178)

Bit	Attr	Reset Value	Description
31:8	RW	0x000000	stab_min_value range : 0~255*253*253

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Bit	Attr	Reset Value	Description
7:6	RW	0x0	stab_mod_sel 0 : disabled 1 : stab only 2 : stab+encode
5:0	RW	0x00	stab_hor_gmv signed register range : -16~16

VEPU_swreg_95

Address: Operational Base + offset (0x017c)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	rgb2yuv_coe2 the 2st conversion coefficien for RGB to YUV
15:0	RW	0x0000	rgb2yuv_coe1 the 1st conversion coefficien for RGB to YUV

VEPU_swreg_96

Address: Operational Base + offset (0x0180)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	rgb2yuv_coe5 the 5st conversion coefficien for RGB to YUV
15:0	RW	0x0000	rgb2yuv_coe3 the 3st conversion coefficien for RGB to YUV

VEPU_swreg_97

Address: Operational Base + offset (0x0184)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0000	rgb2yuv_coe6 the 6st conversion coefficien for RGB to YUV

VEPU_swreg_98

Address: Operational Base + offset (0x0188)

Bit	Attr	Reset Value	Description
31:21	RO	0x0	reserved
20:16	RW	0x00	bcmpt_mask_postition range : 0~31
15:13	RO	0x0	reserved
12:8	RW	0x00	gcmpt_mask_postition range : 0~31
7:5	RO	0x0	reserved
4:0	RW	0x00	rcmpt_mask_postition range : 0~31

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VEPU_swreg_99

Address: Operational Base + offset (0x018c)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:21	RW	0x000	mv_1p_ply differential MV penalty for 1p
20:11	RW	0x000	mv_1p_4p_ply ME. DMVPenaltyQp
10:1	RW	0x000	mv_4p_ply
0	RW	0x0	mutimv_en on-off flag for using exceed one mv every mb

VEPU_swreg_100_reuse

Address: Operational Base + offset (0x0190)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	h264_init_luma_qp range: 0~51
25:20	RW	0x00	h264_max_qp range : 0~51
19:14	RW	0x00	h264_min_qp range:0~51
13	RO	0x0	reserved
12:0	RW	0x0000	h264_chkpt_distance checkpoint distance for macro block

VEPU_swreg_101_read

Address: Operational Base + offset (0x0194)

Bit	Attr	Reset Value	Description
31:12	RO	0x1f522	HW_CONFIG Field0000 Description
11:0	RO	0x780	MAX_VID_WIDTH Field0000 Description

VEPU_swreg_102

Address: Operational Base + offset (0x0198)

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:20	RW	0x0	mv_favor_16x16 value = (real value)/2.
19:11	RW	0x000	mv_ply_4x4
10:8	RW	0x0	mvc_view_id
7	RW	0x0	mvc_anchor_pic_flag

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Bit	Attr	Reset Value	Description
6:4	RW	0x0	mvc_priority_id
3:1	RW	0x0	mvc_temporal_id
0	RW	0x0	mvc_inter_view_flag MVC inter_view_flag.

VEPU_swreg_103
Address: Operational Base + offset (0x019c)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:20	RW	0x000	enc_height lum height (macroblock unit) H264: [6..255] JPEG: [6..511]
19:17	RO	0x0	reserved
16:8	RW	0x000	enc_width lum width (macroblock unit) H264: range : 9~255 JPEG: range : 6~511
7:6	RW	0x0	enc_frame_type 0: INTER 1: INTRA(IDR) 2: MVC-INTER
5:4	RW	0x0	enc_fmt 1 : VP8, 2 : JPEG 3 : H264
3:1	RO	0x0	reserved
0	RW	0x0	enc_en encoder enable

VEPU_swreg_104
Address: Operational Base + offset (0x01a0)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	mb_count_out mb_count_out
15:0	RW	0x0000	mb_cnt macroblock_count

VEPU_swreg_105
Address: Operational Base + offset (0x01a4)

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Bit	Attr	Reset Value	Description
31	RW	0x0	swap8_in 0: no swap 1: swap 8bit
30	RW	0x0	swap16_in 0: no swap 1: swap 16bit
29	RW	0x0	swap32_in 0: no swap 1: swap 32bit
28	RW	0x0	swap8_out 0: no swap 1: swap 8bit
27	RW	0x0	swap16_out 0: no swap 1: swap 16bit
26	RW	0x0	swap32_out 0: no swap 1: swap 32bit
25	RO	0x0	reserved
24	RW	0x0	test_irq test irq
23:20	RW	0x0	test_counter test counter
19	RW	0x0	coher_test_reg test register coherency
18	RW	0x0	coher_test_mem test memory coherency
17:0	RW	0x00000	test_len test data length

VEPU_swreg_106_reuse

Address: Operational Base + offset (0x01a8)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	pic_para_id
23:16	RW	0x00	intra_pred_mode H.264 intra prediction previous 4x4 mode favor
15:0	RW	0x0000	frame_num H.264 frame number

VEPU_swreg_107_reuse

Address: Operational Base + offset (0x01ac)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
29:20	RW	0x000	mv_ply_16x8_8x16 Penalty for using 16x8 or 8x16 MV
19:10	RW	0x000	mv_ply_8x8 Penalty for using 8x8 MV
9:0	RW	0x000	mv_ply_8x4_4x8 Penalty for using 8x4 or 4x8 MV.

VEPU_swreg_108_reuse

Address: Operational Base + offset (0x01b0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	intra_slice_bmp2 bit0 : slices64 bit1 : slices65 bit2 : slices66 ..... bit31 : slices95 VP8: VP8 counters or probability updates start address

VEPU_swreg_109

Address: Operational Base + offset (0x01b4)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28	RW	0x0	int_non Field0000 Description
27:25	RO	0x0	reserved
24	RW	0x0	mv_sad_wren
23:21	RO	0x0	reserved
20	RW	0x0	rocon_write_dis
19:17	RO	0x0	reserved
16	RW	0x0	slice_rdyint_en enable slice ready interruupt
15:13	RO	0x0	reserved
12	RW	0x1	clk_gating_en default clk_gating_en =1'b1
11	RO	0x0	reserved
10	RW	0x0	int_timeout_en enable interrupt for timeout
9	RW	0x0	irq_clr
8	RW	0x0	irq_dis
7	RO	0x0	reserved
6	RW	0x0	irq_timeout
5	RW	0x0	irq_buffer_full
4	RW	0x0	irq_bus_error

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Bit	Attr	Reset Value	Description
3	RW	0x0	fuse_int Field0000 Description
2	RW	0x0	irq_slice_ready
1	RW	0x0	irq_frame_rdy
0	RW	0x0	enc_irq

VEPU_swreg_110_read

Address: Operational Base + offset (0x01b8)

Bit	Attr	Reset Value	Description
31:16	RO	0x4831	prod_id Product ID
15:12	RO	0x1	major_num Major number
11:4	RO	0x22	minor_num Minor number
3:0	RO	0x0	synthesis

VEPU_swreg_120_183

Address: Operational Base + offset (0x01e0)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	dmv_ply_table addr range : 0x01e0~0x02dc swreg120: DMV 4p/1p penalty table values swreg121: DMV 4p/1p penalty table values swreg122: DMV 4p/1p penalty table values swreg123: DMV 4p/1p penalty table values ..... swreg183: DMV 4p/1p penalty table values

4.4.9 VDPU121 Register Summary

Name	Offset	Size	Reset Value	Description
VDPU_SWREG0	0x0000	W	0x00010100	axi control
VDPU_SWREG1	0x0004	W	0x00000000	color coeff register0
VDPU_SWREG2	0x0008	W	0x00000000	color coeff register1
VDPU_SWREG3	0x000c	W	0x00000000	color coeff register2
VDPU_SWREG4	0x0010	W	0x00000000	scl ctrl register0
VDPU_SWREG5	0x0014	W	0x00000000	scl ctrl register1

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Name	Offset	Size	Reset Value	Description
VDPU_SWREG6	0x0018	W	0x00000000	scl ctrl register2
VDPU_SWREG7	0x001c	W	0x00000000	Amount of pixels beyond border register0
VDPU_SWREG8	0x0020	W	0x00000000	Amount of pixels beyond border register2
VDPU_SWREG9	0x0024	W	0x00000000	Rmask register
VDPU_SWREG10	0x0028	W	0x00000000	Gmask register
VDPU_SWREG11	0x002c	W	0x00000000	Bmask register
VDPU_SWREG12	0x0030	W	0x00000000	PP input picture base address for Y bottom field
VDPU_SWREG13	0x0034	W	0x00000000	PP input picture base for Ch bottom field
VDPU_SWREG14	0x0038	W	0x00000000	coordinate used in macroblock crop
VDPU_SWREG15	0x003c	W	0x00000000	range map register
VDPU_SWREG16	0x0040	W	0x00000000	total num of padded for RGB
VDPU_SWREG17	0x0044	W	0x00000000	hw support informan,read only
VDPU_SWREG18	0x0048	W	0x00000000	base address for reading post-processing input picture uminance (top field/frame)
VDPU_SWREG19	0x004c	W	0x00000000	Base address for reading post-processing input picture Cb/Ch (topfield/frame)
VDPU_SWREG20	0x0050	W	0x00000000	input cr component address
VDPU_SWREG21	0x0054	W	0x00000000	Base address for writing post-processed picture luminance/RGB

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Name	Offset	Size	Reset Value	Description
VDPU_SWREG22	0x0058	W	0x00000000	Base address for writing post-processed picture Ch
VDPU_SWREG23	0x005c	W	0x00000000	Display width and PP input size extension register
VDPU_SWREG24	0x0060	W	0x00000000	alpha blending base address
VDPU_SWREG25	0x0064	W	0x00000000	ablend of pixels scanline
VDPU_SWREG26	0x0068	W	0x00000000	x-coordinate of mask area 1 for Horizontal start pixel
VDPU_SWREG27	0x006c	W	0x00000000	y-coordinate of mask area 1 for Horizontal start pixel
VDPU_SWREG28	0x0070	W	0x00000000	x-coordinate of mask area 2 for Horizontal start pixel
VDPU_SWREG29	0x0074	W	0x00000000	y-coordinate of mask area 2 for Horizontal start pixel
VDPU_SWREG30	0x0078	W	0x00000000	register for deinterlace ctrl
VDPU_SWREG31	0x007c	W	0x00000000	contrast adjust threshold
VDPU_SWREG32	0x0080	W	0x00000000	contrast adjust offset
VDPU_SWREG33	0x0084	W	0xfc874780	Synthesis configuration register post-processor (read only)
VDPU_SWREG34	0x0088	W	0x00000000	PP input pic size register
VDPU_SWREG35	0x008c	W	0x00000000	PP output pic size register
VDPU_SWREG36	0x0090	W	0x00000000	the dither mode for RGB
VDPU_SWREG37	0x0094	W	0x00000000	PP input/output data format
VDPU_SWREG38	0x0098	W	0x00000000	PP input/output data format
VDPU_SWREG39	0x009c	W	0x00000000	the display width ctrl

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Name	Offset	Size	Reset Value	Description
VDPU_SWREG40	0x00a0	W	0x00000000	Register0001 Description
VDPU_SWREG41	0x00a4	W	0x00000008	enable ctrl flag
VDPU_SWREG50	0x00c8	W	0x00000000	video decoder ctrl register
VDPU_SWREG51	0x00cc	W	0x00000000	the stream length
VDPU_SWREG52	0x00d0	W	0x00000000	error concealment case related
VDPU_SWREG53	0x00d4	W	0x00000000	decoder format
VDPU_SWREG54	0x00d8	W	0x00000000	endian for input/output data
VDPU_SWREG55	0x00dc	W	0x00000000	decoder int register
VDPU_SWREG56	0x00e0	W	0x00200101	axi ctrl for decoder
VDPU_SWREG57	0x00e4	W	0x00000010	enable flag for decoder
VDPU_SWREG58	0x00e8	W	0x00000000	soft reset registerconfig addr= 4E8
VDPU_SWREG59	0x00ec	W	0x00000000	H264, MPEG4, VC1, VP6 Prediction filter tap
VDPU_SWREG60	0x00f0	W	0x00000000	additional chrominance address
VDPU_SWREG61	0x00f4	W	0x00000000	standard dependent tables start address
VDPU_SWREG62	0x00f8	W	0x00000000	Direct mode motion vector write/read start address
VDPU_SWREG63	0x00fc	W	0x00000000	write decoder output picture or field start address
VDPU_SWREG64	0x0100	W	0x00000000	rlc or vlc mode input data start addr
VDPU_SWREG65	0x0104	W	0x00000000	refbufferd related
VDPU_SWREG66	0x0108	W	0x67312688	ID register

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Name	Offset	Size	Reset Value	Description
VDPU_SWREG67	0x010c	W	0xc1520000	Synthesis configuration register decoder 1(read only)
VDPU_SWREG68	0x0110	W	0x00000000	sum of partitions(read only)
VDPU_SWREG69	0x0114	W	0x00000000	sum information (read only)
VDPU_SWREG70	0x0118	W	0x00000000	sum of the decoded motion vector y-components(read only)
VDPU_SWREG71	0x011c	W	0xfbb56780	information for read only register
VDPU_SWREG72	0x0120	W	0x00000000	debug0
VDPU_SWREG73	0x0124	W	0x00000000	debug registers
VDPU_SWREG74	0x0128	W	0x00000000	MV address for h264
VDPU_SWREG75	0x012c	W	0x00000000	H.264 Intra prediction 4x4 mode start address
VDPU_SWREG76	0x0130	W	0x00000000	the number of referance pic0
VDPU_SWREG77	0x0134	W	0x00000000	the number of referance pic1
VDPU_SWREG78	0x0138	W	0x00000000	the number of referance pic2
VDPU_SWREG79	0x013c	W	0x00000000	the number of referance pic3
VDPU_SWREG80	0x0140	W	0x00000000	the number of referance pic4
VDPU_SWREG81	0x0144	W	0x00000000	the number of referance pic5
VDPU_SWREG82	0x0148	W	0x00000000	the number of referance pic6
VDPU_SWREG83	0x014c	W	0x00000000	the number of referance pic7
VDPU_SWREG84	0x0150	W	0x00000000	referance frame0 address for h264
VDPU_SWREG85	0x0154	W	0x00000000	referance frame1 address for h264

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Name	Offset	Size	Reset Value	Description
VDPU_SWREG86	0x0158	W	0x00000000	referance frame2 address for h264
VDPU_SWREG87	0x015c	W	0x00000000	referance frame3 address for h264
VDPU_SWREG88	0x0160	W	0x00000000	referance frame4 address for h264
VDPU_SWREG89	0x0164	W	0x00000000	referance frame5 address for h264
VDPU_SWREG90	0x0168	W	0x00000000	referance frame6 address for h264
VDPU_SWREG91	0x016c	W	0x00000000	referance frame6 address for h264
VDPU_SWREG92	0x0170	W	0x00000000	referance frame8 address for h264
VDPU_SWREG93	0x0174	W	0x00000000	referance frame9 address for h264
VDPU_SWREG94	0x0178	W	0x00000000	referance frame10 address for h264
VDPU_SWREG95	0x017c	W	0x00000000	referance frame11 address for h264
VDPU_SWREG96	0x0180	W	0x00000000	referance frame12 address for h264
VDPU_SWREG97	0x0184	W	0x00000000	referance frame13 address for h264
VDPU_SWREG98	0x0188	W	0x00000000	referance frame14 address for h264
VDPU_SWREG99	0x018c	W	0x00000000	referance frame15 address for h264

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Name	Offset	Size	Reset Value	Description
VDPU_SWREG100	0x0190	W	0x00000000	initial reference picture list related0
VDPU_SWREG101	0x0194	W	0x00000000	initial reference picture list related1
VDPU_SWREG102	0x0198	W	0x00000000	initial reference picture list related2
VDPU_SWREG103	0x019c	W	0x00000000	initial reference picture list related3
VDPU_SWREG104	0x01a0	W	0x00000000	initial reference picture list related4
VDPU_SWREG105	0x01a4	W	0x00000000	initial reference picture list related5
VDPU_SWREG106	0x01a8	W	0x00000000	initial reference picture list related6
VDPU_SWREG107	0x01ac	W	0x00000000	long term flag for reference pictuure index
VDPU_SWREG108	0x01b0	W	0x00000000	valid flag for reference picture index
VDPU_SWREG109	0x01b4	W	0x00000000	the stream start word for decoder
VDPU_SWREG110	0x01b8	W	0x00000000	h264 pic mb size
VDPU_SWREG111	0x01bc	W	0x00000000	h264 ctrl related
VDPU_SWREG112	0x01c0	W	0x00000000	current frame related
VDPU_SWREG113	0x01c4	W	0x00000000	reference picture related
VDPU_SWREG114	0x01c8	W	0x00000000	maximum reference
VDPU_SWREG115	0x01cc	W	0x00000000	enable flag
VDPU_SWREG120	0x01e0	W	0x00000000	multi format reuse register0

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Name	Offset	Size	Reset Value	Description
VDPU_SWREG121	0x01e4	W	0x00000000	multi format reuse register1
VDPU_SWREG122	0x01e8	W	0x00000000	multi format reuse register2
VDPU_SWREG123	0x01ec	W	0x00000000	multi format reuse register3
VDPU_SWREG124	0x01f0	W	0x00000000	multi format reuse register4
VDPU_SWREG125	0x01f4	W	0x00000000	multi format reuse register5
VDPU_SWREG126	0x01f8	W	0x00000000	multi format reuse register6
VDPU_SWREG127	0x01fc	W	0x00000000	multi format reuse register7
VDPU_SWREG128	0x0200	W	0x00000000	multi format reuse register8
VDPU_SWREG129	0x0204	W	0x00000000	multi format reuse register9
VDPU_SWREG130	0x0208	W	0x00000000	multi format reuse register10
VDPU_SWREG131	0x020c	W	0x00000000	multi format reuse register11
VDPU_SWREG132	0x0210	W	0x00000000	multi format reuse register12
VDPU_SWREG133	0x0214	W	0x00000000	multi format reuse register13
VDPU_SWREG134	0x0218	W	0x00000000	multi format reuse register14
VDPU_SWREG135	0x021c	W	0x00000000	multi format reuse register15
VDPU_SWREG136	0x0220	W	0x00000000	multi format reuse register16
VDPU_SWREG137	0x0224	W	0x00000000	multi format reuse register17
VDPU_SWREG138	0x0228	W	0x00000000	multi format reuse register18
VDPU_SWREG139	0x022c	W	0x00000000	multi format reuse register19
VDPU_SWREG140	0x0230	W	0x00000000	multi format reuse register20
VDPU_SWREG141	0x0234	W	0x00000000	multi format reuse register21

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Name	Offset	Size	Reset Value	Description
VDPU_SWREG142	0x0238	W	0x00000000	multi format reuse register22
VDPU_SWREG143	0x023c	W	0x00000000	multi format reuse register23
VDPU_SWREG144	0x0240	W	0x00000000	multi format reuse register24
VDPU_SWREG145	0x0244	W	0x00000000	multi format reuse register25
VDPU_SWREG146	0x0248	W	0x00000000	multi format reuse register26
VDPU_SWREG147	0x024c	W	0x00000000	multi format reuse register27
VDPU_SWREG148	0x0250	W	0x00000000	multi format reuse register28
VDPU_SWREG149	0x0254	W	0x00000000	multi format reuse register29
VDPU_SWREG150	0x0258	W	0x00000000	multi format reuse register30
VDPU_SWREG151	0x025c	W	0x00000000	multi format reuse register31
VDPU_SWREG152	0x0260	W	0x00000000	multi format reuse register32
VDPU_SWREG153	0x0264	W	0x00000000	multi format reuse register33
VDPU_SWREG154	0x0268	W	0x00000000	multi format reuse register34
VDPU_SWREG155	0x026c	W	0x00000000	multi format reuse register35
VDPU_SWREG156	0x0270	W	0x00000000	multi format reuse register36
VDPU_SWREG157	0x0274	W	0x00000000	multi format reuse register37
VDPU_SWREG158	0x0278	W	0x00000000	multi format reuse register38
VDPU_SWREG164_PERF_LATENCY_CTRL0	0x0290	W	0x00000000	Axi performance latency module contrl register0
VDPU_SWREG165_PERF_LATENCY_CTRL1	0x0294	W	0x00000000	PERF_LATENCY_CTRL1
VDPU_SWREG166_PERF_RD_MAX_LATENCY_NUM0	0x0298	W	0x00000000	Read max latency number

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Name	Offset	Size	Reset Value	Description
VDPU_SWREG167_PERF_RD_LATENCY_SAMP_NUM	0x029c	W	0x00000000	The number of bigger than configed threshold value
VDPU_SWREG168_PERF_RD_LATENCY_ACC_SUM	0x02a0	W	0x00000000	Total sample number
VDPU_SWREG169_PERF_RD_AXI_TOTAL_BYTE	0x02a4	W	0x00000000	perf_rd_axi_total_byte
VDPU_SWREG170_PERF_WR_AXI_TOTAL_BYTE	0x02a8	W	0x00000000	perf_wr_axi_total_byte
VDPU_SWREG171_PERF_WORKING_CNT	0x02ac	W	0x00000000	perf_working_cnt

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

4.4.10 VDPU121 Detail Register Description

VDPU_SWREG0

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:16	RW	0x01	sw_axi_id_wr if you config 0,will modify as 1 by hw
15:8	RW	0x01	sw_axi_id_rd if you config 0,will modify as 1 by hw
7:6	RO	0x0	reserved
5	RW	0x0	sw_scmd_off on-off for AXI Single Command Multiple Data 0:on 1:off
4:0	RW	0x00	sw_max_burst_len range : 1-16

VDPU_SWREG1

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x000	sw_coe_2st used for red color components calculate,used together with cr pix
19:10	RW	0x000	sw_coe_1st_1 used for all color components calculate,used together with y pix
9:0	RW	0x000	sw_coe_1st_0 used for all color components calculate,used together with y pix

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VDPU_SWREG2

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x000	sw_coe_5st used for blue components calculate,used together with cb pix
19:10	RW	0x000	sw_coe_4st used for green color components calculate,used together with cb pix
9:0	RW	0x000	sw_coe_3st used for green color components calculate,used together with cr pix

VDPU_SWREG3

Address: Operational Base + offset (0x000c)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x00	sw_coe_6st used for burightness adjust,used together with y pix

VDPU_SWREG4

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:22	RW	0x0	sw_scl_mode_vrt 0 = no scl 1 = up scl 2 = down scl
21:20	RW	0x0	sw_scl_mode_hrz 0 = no scl 1 = up scl 2 = down scl
19:18	RO	0x0	reserved
17:0	RW	0x00000	sw_scl_fct_w value = (output_width-1)/(input_width-1)

VDPU_SWREG5

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:18	RO	0x0	reserved
17:0	RW	0x00000	sw_scl_fct_h value = (output_width-1)/(input_width-1)

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VDPU_SWREG6

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_scl_fct_h_inv value =(inputw-1) / (outputw-1)
15:0	RW	0x0000	sw_scl_fct_w_inv value =(inputw-1) / (outputw-1)

VDPU_SWREG7

Address: Operational Base + offset (0x001c)

Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved
26:16	RW	0x000	sw_pixnum_down_byd Range : 0-dst_height
15:11	RO	0x0	reserved
10:0	RW	0x000	sw_pixnum_up_byd Range : 0-dst_height

VDPU_SWREG8

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved
26:16	RW	0x000	sw_pixnum_right_byd Range : 0~dst_width
15:11	RO	0x0	reserved
10:0	RW	0x000	sw_pixnum_left_byd Range : 0~dst_width

VDPU_SWREG9

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_mask_r color R/(alpha channnel) component 's bit mask

VDPU_SWREG10

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_mask_g color G/(alpha channnel) component 's bit mask

VDPU_SWREG11

Address: Operational Base + offset (0x002c)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_mask_b color B/(alpha channnel) component 's bit mask

VDPU_SWREG12

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	sw_botfld_y_st_adr input bottom field pp start address for y component
1:0	RO	0x0	reserved

VDPU_SWREG13

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	sw_botfld_c_st_adr input bottom field pp start address for c component
1:0	RO	0x0	reserved

VDPU_SWREG14

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29	RW	0x0	sw_mrmb_8pix_flag 829PP input picture width is not 16 pixels multiple. Only 8 pixels of the most right MB of the unrotated input picture is used for PP input.
28	RW	0x0	sw_mdmb_8pix_flag the most down unrotated MB of input picture just 8 rows pix data
27	RO	0x0	reserved
26:24	RW	0x0	sw_mbcrop_crdty_ext in order to support jpeg to extend coordinate y bits
23:16	RW	0x00	sw_mbcrop_crdty coordinate y used in macroblock crop
15:12	RO	0x0	reserved
11:9	RW	0x0	sw_mbcrop_crdtx_ext in order to support jpeg to extend bits
8:0	RW	0x000	sw_mbcrop_crdtx coordinate x used in macroblock crop

VDPU_SWREG15

Address: Operational Base + offset (0x003c)

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Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12:8	RW	0x00	sw_rangemap_coef_c VC- 1:c range map value +9
7:6	RO	0x0	reserved
5	RW	0x0	sw_yuv_conv_range Y: 0:16~235 1:0~255 C: 0:16~240 1:0~255
4:0	RW	0x00	sw_rangemap_y VC- 1:y range map value +9

VDPU_SWREG16

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:21	RO	0x0	reserved
20:16	RW	0x00	sw_padd_b the total num of padded in front of B componet
15:13	RO	0x0	reserved
12:8	RW	0x00	sw_padd_g the total num of padded in front of G componet
7:5	RO	0x0	reserved
4:0	RW	0x00	sw_padd_r the total num of padded in front of R componet

VDPU_SWREG17

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RO	0x0	pp_deinterl_en 0: off 1 : on
29	RO	0x0	pp_abled_en 0: off 1 : on
28	RO	0x0	pp_work_en 0 : off 1: on
27:4	RO	0x0	reserved
3	RO	0x0	pp_outw_1920_en 1st priority used

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Bit	Attr	Reset Value	Description
2	RO	0x0	pp_outw_1280_en 2st priority used
1	RO	0x0	pp_outw_720_en 3st priority used
0	RO	0x0	pp_outw_352_en 4st priority used

VDPU_SWREG18

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	sw_y_in_st_adr The start address of topfield of the picture when data come from fields.extemal mode support only
1:0	RO	0x0	reserved

VDPU_SWREG19

Address: Operational Base + offset (0x004c)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	sw_cb_in_st_adr The start address of topfield of the picture when data come from fields,extemal mode support only
1:0	RO	0x0	reserved

VDPU_SWREG20

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	sw_cr_in_st_adr The start address of topfield of the picture when data come from fields,extemal mode support only
1:0	RO	0x0	reserved

VDPU_SWREG21

Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_y_out_st_adr also the start address of YUYV and RGB

VDPU_SWREG22

Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_c_out_st_adr format is uvuvuv....

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VDPU_SWREG23

Address: Operational Base + offset (0x005c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_abled_st_adr_1st 1.valid when mask1 is used in alpha blending mode 2.Format of data the same as in PP input. 3.Amount of data is related to mask 1 size or ablend1_scanline informed with mask 1 size or with ablend1_scanline if ablend when crop flag valid

VDPU_SWREG24

Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_abled_st_adr_2st 1.valid when mask2 is used in alpha blending mode 2.Format of data the same as in PP input. 3.Amount of data is related to mask 2 size or ablend1_scanline informed with mask 1 size or with ablend1_scanline if ablend when crop flag valid

VDPU_SWREG25

Address: Operational Base + offset (0x0064)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	sw_scanl_abld2 corresponding function should be enabled
15:13	RO	0x0	reserved
12:0	RW	0x0000	sw_scanl_abld1 corresponding function should be enabled

VDPU_SWREG26

Address: Operational Base + offset (0x0068)

Bit	Attr	Reset Value	Description
31:23	RO	0x0	reserved
22:12	RW	0x000	sw_end_coordx_ma1 range:sw_st_coordx_ma1-dst width
11	RO	0x0	reserved
10:0	RW	0x000	sw_st_coordx_ma1 the start x-coordinate of mask area 1 of Horizontal start pixel

VDPU_SWREG27

Address: Operational Base + offset (0x006c)

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Bit	Attr	Reset Value	Description
31:23	RO	0x0	reserved
22:12	RW	0x000	sw_end_coordy_ma1 range:sw_st_coordy_ma1~dst width
11	RO	0x0	reserved
10:0	RW	0x000	sw_st_coordy_ma1 the start y-coordinate of mask area 1 of Vertical start pixel

VDPU_SWREG28

Address: Operational Base + offset (0x0070)

Bit	Attr	Reset Value	Description
31:22	RO	0x0	reserved
21:11	RW	0x000	sw_end_coordx_ma2 range:sw_st_coordx_ma2~dst width
10:0	RW	0x000	sw_st_coordx_ma2 the start x-coordinate of mask area 2 of Horizontal start pixel

VDPU_SWREG29

Address: Operational Base + offset (0x0074)

Bit	Attr	Reset Value	Description
31:22	RO	0x0	reserved
21:11	RW	0x000	sw_end_coordy_ma2 range:sw_st_coordy_ma2-dst width
10:0	RW	0x000	sw_st_coordy_ma2 the start y-coordinate of mask area 2 of Vertical start pixel

VDPU_SWREG30

Address: Operational Base + offset (0x0078)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:16	RW	0x0000	sw_deinterl_edge Edge detect value used for deinterlacing
15:14	RO	0x0	reserved
13:0	RW	0x0000	sw_deinterl_thr the threshold value of deinterlace

VDPU_SWREG31

Address: Operational Base + offset (0x007c)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:8	RW	0x00	sw_cont_thr1 the threshold value 1 for contrast adjust
7:0	RW	0x00	sw_cont_thr0 the threshold value 0 for contrast adjust

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VDPU_SWREG32

Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:16	RW	0x000	sw_cont_offset1 the offset value 1 for contrast adjust
15:10	RO	0x0	reserved
9:0	RW	0x000	sw_cont_offset0 the offset value 0 for contrast adjust

VDPU_SWREG33

Address: Operational Base + offset (0x0084)

Bit	Attr	Reset Value	Description
31	RO	0x1	abld_crop_flag 0: unsupport crop,the exact image of the area being alpha blended should exist in the external memory 1: supprot crop,one picture in external memory which come from blended area can be cropped
30	RO	0x1	accut_out_exist_flag PIP: 0 : use 8 pixels (width) or 2 pixels (height) steps to adjust Scaling and masks 1 : use 1 pixel for RGB and 2 pixels for subsampled chroma formats to adjust Scaling and masks
29	RO	0x1	tile_exist_flag 0 : no exist 1 : exist
28	RO	0x1	dither_exist_flag 0 : no exist 1 : exist
27:26	RO	0x3	scl_perf_sel 0 : without scaling 1 : low perfomance scaling 2 : high perfomance scaling 3 : high and fast perfomance scaling
25	RO	0x0	deinterl_exist_flag 0 : no exist 1 : exist
24	RO	0x0	abld_exist_flag 0 : no exist 1 : exist
23	RO	0x1	pp_in_buf_sel 0 : output buffering is 1 MB 1 : output buffering is 4 MB

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Bit	Attr	Reset Value	Description
22:19	RO	0x0	reserved
18	RO	0x1	pp_endian_mode 0 : Endian mode supported except RGB 1 : Endian mode supported for all format
17	RO	0x1	pp_out_buf_sel 0 : output buffering is 1 unit 1 : output buffering is 4 unit
16	RO	0x1	ppd_exist_flag 0 : no exist 1 : exist
15:14	RO	0x1	pp_tile_in_mode 0 : unsupport 1 : 8x4 tile be used
13:11	RO	0x0	reserved
10:0	RO	0x780	ppd_max_outw the max pixels width allow for pp output

VDPU_SWREG34

Address: Operational Base + offset (0x0088)

Bit	Attr	Reset Value	Description
31:29	RW	0x0	sw_pp_inh_ext in order to support jpeg
28:21	RW	0x00	sw_pp_inh the picture height of PP input with in macro blocks which can be cropped from a bigger picture when in the condtion of external mode
20:12	RW	0x000	sw_org_inw_ext the orginal width of pp input pic in MBS
11:9	RW	0x0	sw_pp_inw_ext in order to support jpeg
8:0	RW	0x000	sw_pp_inw the picture width of PP input with in macro blocks which can be cropped from a bigger picture when in the condtion of external mode

VDPU_SWREG35

Address: Operational Base + offset (0x008c)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27	RW	0x0	sw_pp_outh_ext the extension height of pp output

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Bit	Attr	Reset Value	Description
26:16	RW	0x000	sw_pp_outh (output width = 2*n (n=1,2,.....) || output width =(configurationed Pixel Accurate PP output configuration)*n) && (pp output width < 1920 || pp output width< 3*(sw_pp_inh-8))
15:12	RO	0x0	reserved
11	RW	0x0	sw_pp_outw_ext the extension width of pp output
10:0	RW	0x000	sw_pp_outw (output width = 8*n (n=1,2,.....) || output width =(configurationed Pixel Accurate PP output configuration)*n) && (pp output width < 1920 || pp output width< 3*(sw_pp_inw-8))

VDPU_SWREG36

Address: Operational Base + offset (0x0090)

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5:4	RW	0x0	sw_dither_mode_b 0 : no use dithering 1 : 4-bits dither matrix be used 2 : 5-bits dither matrix be used 3 : 6-bits dither matrix be used
3:2	RW	0x0	sw_dither_mode_g 0 : no use dithering 1 : 4-bits dither matrix be used 2 : 5-bits dither matrix be used 3 : 6-bits dither matrix be used
1:0	RW	0x0	sw_dither_mode_r 0 : no use dithering 1 : 4-bits dither matrix be used 2 : 5-bits dither matrix be used 3 : 6-bits dither matrix be used

VDPU_SWREG37

Address: Operational Base + offset (0x0094)

Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
26:24	RW	0x0	sw_pp_in_data_strc 0 : Top field 1 : Bottom field 2 : Interlaced field 3 : Interlaced frame 4 : Ripped top field 5 : Ripped bottom field if value=0/1/2,then should read every line from the base address,if value=3/4/5,then should read every second line from the base address
23:20	RO	0x0	reserved
19	RW	0x0	sw_pp_out_crbf_en 0 : Y0CbY0Cr / CbY0CrY0 1 : Y0CrY0Cb / CrY0CbY0
18	RW	0x0	sw_pp_in_crbf_en yuv422: 0 : Y0CbY0Cr / CbY0CrY0 1 : Y0CrY0Cb / CrY0CbY0 yuv420 semiplanar chrominance: 0 : CbCrCbCr 1:CrCbCrCb
17	RW	0x0	sw_pp_out_yuv_order 0 : Y0CbY0Cr / Y0CrY0Cb 1 : CbY0CrY0 / CrY0CbY0
16	RW	0x0	sw_pp_in_yuv_order 0 : Y0CbY0Cr / Y0CrY0Cb 1 : CbY0CrY0 / CrY0CbY0
15:12	RO	0x0	reserved
11	RW	0x0	sw_pp_out_wordsp it will be used in 64 bit environment 0 : no swapping 1 : swapping high and low 32bit data
10	RW	0x0	sw_pp_out_hfwordsp 0:no swap 1:swap also be used as change pixel orders for 16 bit RGB,support all output format require pp_endian_mode=1
9	RW	0x0	sw_pp_abld1_in_wordsp for Alpha blend source 1 0 : no swapping 1 : swapping high and low 32bit data

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Bit	Attr	Reset Value	Description
8	RW	0x0	sw_pp_in_wordsp it will be used in 64 bit environment 0 : no swapping 1 : swapping high and low 32bit data
7:5	RO	0x0	reserved
4	RW	0x0	sw_rgb_pix_bits 0: every word have only one rga pixel 1:every word have two rga pixel
3	RW	0x0	sw_pp_out_endian for all yuv output endian mode or any data when pp_endian_mode=1 0 : big endian 1 : little endian if pp_endian_mode=0: 16 bit RGB: this bit used as pixel swapping bit 32 bit RGB: no used
2	RW	0x0	sw_pp_abld2_in_endian 0: same with sw_pp_in_endian 1: same with sw_pp_abld1_in_endian '0' = Use PP in endian/swap definitions (sw_pp_in_endian, sw_pp_in_swap) '1' = Use Ablend source 1 endian/swap definitions
1	RW	0x0	sw_pp_abld1_in_endian 0 : big endian (0-1-2-3) 1 : little endian (3-2-1-0)
0	RW	0x0	sw_pp_in_endian this bit will no to be used when PP is running pipelined with the decoder 0 : big endian (0-1-2-3) 1 : little endian (3-2-1-0)

VDPU_SWREG38

Address: Operational Base + offset (0x0098)

Bit	Attr	Reset Value	Description
31:22	RO	0x0	reserved
21:20	RW	0x0	sw_pp_in_tilmod only support yuv420 input data,can be as pipeline or external mode 0 : Tiled mode not be actived 1 : 8x4 sized tiles be used 2,3 : reserved
19	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
18:16	RW	0x0	sw_pp_in_fmt_ecp be actived when sw_pp_in_fmt = 3'b111 0 : YCbCr 4:4:4 1 : YCbCr 4:1:1
15:14	RO	0x0	reserved
13:11	RW	0x0	sw_pp_out_fmt 0 : RGB 1 : YCbCr 4:2:0 ; planar (Not supported) 2 : YCbCr 4:2:2 ; planar (Not supported) 3 : YUYV 4:2:2 ; interleaved 4 : YCbCr 4:4:4 ; planar (Not supported) 5 : YCh 4:2:0 ; chrominance interleaved 6 : YCh 4:2:2 ; (Not supported) 7 : YCh 4:4:4 (Not supported)
10:8	RW	0x0	sw_pp_in_fmt 0 : YUYV 4:2:2 ; interleaved and it only supported in external mode 1 : YCbCr 4:2:0 ; the format of Semi-planar in linear raster-scan 2 : YCbCr 4:2:0 ; planar and it only supported in external mode 3 : YCbCr 4:0:0 ; it only supported in pipelined mode 4 : YCbCr 4:2:2 ; Semi-planar and it only supported only in pipelined mode 5 : YCbCr 4:2:0 ; Semi-planar in tiled format and it only supported in external mode 6 : YCbCr 4:4:0 ; Semi-planar and it only supported for jpeg in pipelined mode 7 : same as sw_pp_in_fmt_ecp
7:3	RO	0x0	reserved
2:0	RW	0x0	sw_rot_mode 0 : rotation disabled 1 : rotate + 90 2 : rotate –90 3 : horizontal flip (mirror) 4 : vertical flip 5 : rotate 180

VDPU_SWREG39

Address: Operational Base + offset (0x009c)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0x000	sw_display_w Max support 1920

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VDPU_SWREG40

Address: Operational Base + offset (0x00a0)

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3	RW	0x0	sw_pp_bus_sts the Interrupt status bit for tell sw bus have some error
2	RW	0x0	sw_pp_rdy_sts the Interrupt status bit for tell sw processed a picture
1	RW	0x0	sw_pp_irq_dis 1 : use polling to see the interrupt 0 : use sw_pp_irq
0	RW	0x0	sw_pp_irq after sw query this interrupt,shoud write 0 to reset. this bit will no used in pipeline mode

VDPU_SWREG41

Address: Operational Base + offset (0x00a4)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28	RW	0x0	sw_pp_ahb_hlock_en the service is locked to pp as long as it needs the bus
27	RW	0x0	sw_rightwd_cross_en 0 : disable, 1 : enable
26	RW	0x0	sw_leftsd_cross_en 0 : disable, 1 : enable
25	RW	0x0	sw_downwd_cross_en 0 : disable, 1 : enable
24	RW	0x0	sw_upwd_cross_en 0 : disable, 1 : enable
23	RW	0x0	sw_mask2_abld_en alpha blending for the output picture , only be supported when data format is RGB/YUYV422 Alpha blending read data from alpha blend 2 base address
22	RW	0x0	sw_mask1_abld_en alpha blending for the output picture , only be supported when data format is RGB/YUYV422 Alpha blending read data from alpha blend 1 base address
21	RW	0x0	sw_mask2_en 0 : disable, 1 : enable

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Bit	Attr	Reset Value	Description
20	RW	0x0	sw_mask1_en 0 : disable, 1 : enable
19:17	RO	0x0	reserved
16	RW	0x0	sw_pp_discd_en the burst length will be fix after sw_pp_discd_en=1,and extra read data will auto be discarded by HW
15:12	RO	0x0	reserved
11	RW	0x0	sw_pp_out_tiled_en only used in YCbYCr format . Tile size : 4x4 pixels.
10	RW	0x0	sw_pp_fdscl_en 0 : disable 1 : enabled. it will inprove the performance but will decrease the quality of the pic
9	RW	0x0	sw_rangemap_c_en the enable flag for C component Range map
8	RW	0x0	sw_rangemap_y_en VC1: used as range expansion enable
7:5	RO	0x0	reserved
4	RW	0x0	sw_pp_pipl_en 0 : disable, external mode 1 : enable, pipeline mode,Post-processing pipeline with decoder
3	RW	0x1	sw_pp_clkgate_en pp auto clock gating: default is 1 0 : don't auto gating 1 : audo gating PP dynamic clock gating enable: 1 = Clock is gated from PP structures that are not used 0 = Clock is running for all PP structures Note: Clock gating value can be changed only when PP is not enabled
2	RW	0x0	sw_deint_en the input data should be interlaced format
1	RW	0x0	sw_deint_bld_en on-off Blend for deinterlacing
0	RW	0x0	sw_pp_dec_st after config other register,write 1 to start post-processing operation,and hw will reset to 0 after it decodered a picture should be under External mode.

VDPU_SWREG50

Address: Operational Base + offset (0x00c8)

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Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:25	RW	0x00	sw_refbuf_pid The used reference picture ID for reference buffer usage
24:13	RW	0x000	sw_refbuf_thrd Used shut down buffer
12	RW	0x0	sw_dec_tiled_lsb 0 : Tiled mode disable 1 : Tiled mode enabled for 8x4 tile size
11	RW	0x0	sw_adv_pref_dis disable for Advanced PREFETCH mode
10	RW	0x0	sw_dec_ascmd0_dis the disable for AXI Single Command Multiple Data0
9	RW	0x0	sw_skip_sel AVS format: 0 : skip mbs use special MB type 1 : avs skip mbs have the same skip run syntax element as h264
8	RW	0x0	sw_dblk_flt_dis 1: disable 0: enable
7	RW	0x0	sw_dec_fixed_quant h.264: this bit is for the enable of multi view coding other format(VC1) 0: it can be different inside pic for Quantization parameter 1: it is fixed for Quantization parameter
6:1	RW	0x00	sw_adtion_latency Can be used to slow down 8*sw_dec_latency cycles of IDLE between services,so if sw_dec_latency =0,that is no latency
0	RW	0x0	sw_dec_tiled_msb 0 : Tiled mode disable 1 : Tiled mode enabled for 8x4 tile size

VDPU_SWREG51

Address: Operational Base + offset (0x00cc)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:25	RW	0x00	sw_qp_init_val the qp(quantization parameter)'s Initial value
24	RW	0x0	sw_strm_len_ext The extension bit of sw_strm_len

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Bit	Attr	Reset Value	Description
23:0	RW	0x000000	sw_strm_len if the buffer size be given small than it required,hw will give an interrupt,and then you should config again,and the stream start address should be config also. VC1: one picture/slice of the picture's should be included in the input buffer H264/H263/MPEG*: one slice of the picture's should be included in the input buffer JPEG: 256bytes or onepicture should be included in the input buffer

VDPU_SWREG52

Address: Operational Base + offset (0x00d0)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:17	RW	0x0000	sw_adv_pref_thrd when current MB num > this threshold value,then advanced mode will be closed
16:8	RW	0x000	sw_xdim_mbst it may be used in error concealment case
7:0	RW	0x00	sw_ydim_mbst it may be used in error concealment case

VDPU_SWREG53

Address: Operational Base + offset (0x00d4)

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3:0	RW	0x0	sw_dec_fmt_sel 0 : H.264, 1 : MPEG-4, 2 : H.263, 3 : JPEG, 4 : VC-1, 5 : MPEG-2, 6 : MPEG-1, 9 : VP7, 11 : AVS, others : reserved

VDPU_SWREG54

Address: Operational Base + offset (0x00d8)

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
5	RW	0x0	sw_dec_strendian_e 0 : Big endian (0-1-2-3 order) 1 : Little endian (3-2-1-0 order)
4	RW	0x0	sw_dec_strm_wordsp it will be used in 64 bit environment 0 : no swapping 1 : swapping high and low 32bit data
3	RW	0x0	sw_dec_out_wordsp it will be used in 64 bit environment 0 : no swapping 1 : swapping high and low 32bit data
2	RW	0x0	sw_dec_in_wordsp it will be used in 64 bit environment 0 : no swapping 1 : swapping high and low 32bit data note : it no used for stream data
1	RW	0x0	sw_dec_out_endian Decoder output endian mode: 0 : Big endian (0-1-2-3 order) 1 : Little endian (3-2-1-0 order)
0	RW	0x0	sw_dec_in_endian 0 : Big endian (0-1-2-3 order) 1 : Little endian (3-2-1-0 order) note : it no used for stream data

VDPU_SWREG55

Address: Operational Base + offset (0x00dc)

Bit	Attr	Reset Value	Description
31:14	RO	0x0	reserved
13	RW	0x0	sw_timeout_det_sts AXI in IDLE status too long
12	RW	0x0	sw_error_det_sts Interrupt status bit input stream error. When high, an error is found in input data stream decoding. HW will self reset. (1,2,3,6,48,55,57)
11	RO	0x0	reserved
10	RO	0x0	reserved
9	RW	0x0	sw_slice_det_sts the Interrupt status bit for tell us slice be decoded
8	RW	0x0	sw_aso_det_sts ASO:Arbitrary Slice Ordering
7	RO	0x0	reserved
6	RW	0x0	sw_buf_emt_sts the Interrupt status bit for tell input buffer empty

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Bit	Attr	Reset Value	Description
5	RW	0x0	sw_pp_bus_sts the Interrupt status bit for tell sw bus have some error
4	RW	0x0	sw_dec_rdy_sts the Interrupt status bit for tell sw processed a picture
3:2	RO	0x0	reserved
1	RW	0x0	sw_dec_irq_dis 1 : use polling to see the interrupt 0 : use sw_pp_irq
0	RW	0x0	sw_dec_irq after sw query this interrupt,shoud write 0 to reset.

VDPU_SWREG56

Address: Operational Base + offset (0x00e0)

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23	RW	0x0	sw_axi_sel 0: auto sel for encoder or decoder 1: sel decoder (only used in the middle decoder frame to set bus_dec_en to 0)
22	RW	0x0	sw_dec_data_discd_en the fixed burst length will be used ,and the more read datas will be auto discarded by hw
21	RW	0x1	sw_bus_pos_sel 0:serial 1:parallel
20:16	RW	0x00	sw_dec_max_burlen range : 1-16
15:8	RW	0x01	sw_dec_axi_id_wr if you config 0,will modify as 1 by hw
7:0	RW	0x01	sw_dec_axi_id_rd if you config 0/5,will modify as 1 by hw

VDPU_SWREG57

Address: Operational Base + offset (0x00e4)

Bit	Attr	Reset Value	Description
31	RW	0x0	sw_dec_timeout_mode when 1'b0 , timeout cycle is 181'b1 when 1'b1, timeout cycle is 221'b1
30	RO	0x0	reserved
29	RW	0x0	sw_cache_en 1'b1: cache enable 1'b0: cache disable when sw_cache_en is 1'b1, sw_pref_sigchan should also be 1'b1

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Bit	Attr	Reset Value	Description
28	RW	0x0	sw_pref_sigchan 1'b1: prefetch single channel enable
27	RW	0x0	sw_intra_dbl3t In chroma dc intra prediction, when this bit is enable, there will 3 cycle enhance for every block
26	RW	0x0	sw_intra_dblspeed Intra double speed enable
25	RW	0x0	sw_inter_dblspeed Inter double speed enable
24:23	RO	0x0	reserved
22	RW	0x0	sw_st_code_exist 0 : not exist 1 : exist
21	RW	0x0	sw_addit_ch_fmt_wen tiled mode should be disable,when this bit be used decoder writes chrominance: group of 8 pixels of Cb then corresponding 8 pixels of Cr Data is written to sw_dec_ch8pix_st_adr.
20	RW	0x0	sw_rlc_mode_en 0:decoder data come from bit stream(VLC mode),side information (bitplane data in VC-1) 1:decoder data come from RLC input data,only h.264 and MPEG4 sp be valid
19	RO	0x0	reserved
18	RW	0x0	sw_prog_jpeg_en 0 : baseline JPEG 1 : progressive JPEG
17	RW	0x0	sw_curpic_code_sel 0 : progressive 1 : interlaced
16	RW	0x0	sw_curpic_stru_sel 0 : frame structure, (that isMBAFF structured picture is interlaced) 1 : field structure
15	RW	0x0	sw_pic_type_sel1 0:desided by sw_pic_type_sel0 1: picture type is BI/D/B note: BI is for vc1 D is for mpeg1 B is for h264
14	RW	0x0	sw_pic_type_sel0 should need sw_pic_type_sel1=0 0: Intra type (I) 1:Inter type (P)

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Bit	Attr	Reset Value	Description
13	RW	0x0	sw_pic_decfield_sel 0 : bottom field 1 : top field
12	RW	0x0	sw_fwd_refpic_mode_sel used for forward reference picture: 0 : progressive 1 : interlaced the backward reference picture is the same as current picture
11	RO	0x0	reserved
10	RW	0x0	sw_dmmv_wr_en 0:disable 1:enable this bit used in MPEG2 is for the purpose error concealment case. this bit used in h264 is for the purpose write DPB case with the corresponding reference picture. this bit used in other decoder format is for the purpose writing to external memory starting from mv start address
9	RW	0x0	sw_reftop_en sw_dec_fmt_sel =VC-1 and sw_ref_frm = 0 , 0 = bottom field 1 = top field
8	RW	0x0	sw_first_reftop_en 0 : FWD reference bottom field 1 : FWD reference top field
7	RW	0x0	sw_sequ_mbaff_en 0:disable 1:enable
6	RW	0x0	sw_rd_cnt_tab_en read data from memory used 0:disable 1:enable (hw will read pic order counts)
5	RW	0x0	sw_timeout_sts_en 0:disable 1:enable (if hw can be working status too long,you will get an timeout interrupt)
4	RW	0x1	sw_dec_clkgate_en default hw will reset to 1 0:disable 1:enable
3	RO	0x0	reserved
2	RW	0x0	sw_dec_wr_extmem_dis 0 : enable 1:disable(no write to external memory)

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Bit	Attr	Reset Value	Description
1	RW	0x0	sw_refpic_buf2_en 0:disable 1:enable (should : pic size > QVGA)
0	RW	0x0	sw_dec_st_work hw will auto reset this be after a frame be decodered no matter it right or have some error

VDPU_SWREG58

Address: Operational Base + offset (0x00e8)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	W1C	0x0	sw_soft_rst write 1 to reset,and it will auto reset to 0 after one cycle

VDPU_SWREG59

Address: Operational Base + offset (0x00ec)

Bit	Attr	Reset Value	Description
31:22	RW	0x000	sw_pflt_set0_tap0 0, tap 0
21:12	RW	0x000	sw_pflt_set0_tap1 set 0, tap 1
11:2	RW	0x000	sw_pflt_set0_tap2 set 0, tap 2
1:0	RO	0x0	reserved

VDPU_SWREG60

Address: Operational Base + offset (0x00f0)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	sw_addit_ch_st_adr The usage is enabled by sw_addit_ch_fmt_wen
1:0	RO	0x0	reserved

VDPU_SWREG61

Address: Operational Base + offset (0x00f4)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	sw_qtable_st_adr JPEG : AC,DC, QP tables MPEG4/2 : QP table H.264 :various tables VP7 : stream decoding tables
1:0	RO	0x0	reserved

VDPU_SWREG62

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Address: Operational Base + offset (0x00f8)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	sw_dmmv_st_adr H264: Direct mode motion vector write/read start address Progressive JPEG: the start address for ACDC coefficient read/write If current round is for DC components : this start address is pointing to luminance AC component rounds: this start address is used for current type
1:0	RO	0x0	reserved

VDPU_SWREG63

Address: Operational Base + offset (0x00fc)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	sw_dec_out_st_adr video: write decoder output picture or field start address JPEG snapshot: wirete decoder output luminance picture start address
1:0	RO	0x0	reserved

VDPU_SWREG64

Address: Operational Base + offset (0x0100)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	sw_rlc_vlc_st_adr RLC mode: RLC data start address VLC mode: Stream start address HW return value of last_byte_address by this register to tell where stream has been read when you get some abnormality interrupt,may be used for debug VP7: DCT stream for MB rows 0,2n start address
1:0	RO	0x0	reserved

VDPU_SWREG65

Address: Operational Base + offset (0x0104)

Bit	Attr	Reset Value	Description
31	RW	0x0	sw_refbu_e 0 : disable 1 : enable

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Bit	Attr	Reset Value	Description
30:19	RW	0x000	sw_refbu_thr_level Reference buffer disable threshold value (cache miss amount). Used to buffer shut down (if more misses than allowed)
18:14	RW	0x00	sw_refbuf_picid
13	RW	0x0	sw_refbuf_idcal_e If given threshold level is reached by any picture_id after first MB row, that picture_id is used for reference buffer fill for rest of the picture
12	RW	0x0	sw_refbuf_fildpar_mod_e the mode enable for Field parity mode enable. 0 : the result field of the evaluation be used 1 : the parity mode field be used
11:9	RO	0x0	reserved
8:0	RW	0x000	sw_refbuf_y_ofset if hw should compensate the global motion of the video for better buffer hit rate will use this coordinate

VDPU_SWREG66

Address: Operational Base + offset (0x0108)

Bit	Attr	Reset Value	Description
31:16	RO	0x6731	prod_id product number
15:12	RO	0x2	major_num major_num
11:4	RO	0x68	minor_num minor_num
3	RO	0x1	ascii_id_en enable for ASCII product ID
2:0	RO	0x0	build_ver build_ver

VDPU_SWREG67

Address: Operational Base + offset (0x010c)

Bit	Attr	Reset Value	Description
31	RO	0x1	jpeg_allow_flag 16Mpixel~67Mpixel be sampled and supported by 411 and 444
30	RO	0x1	refbuf_allow_flag 0:no support 1:support
29	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
28	RO	0x0	refbuf2_allow_flag refbuffer2 support
27:26	RO	0x0	reserved
25	RO	0x0	rom_imp_type 0: from actual ROM units 1: from RTL
24	RO	0x1	vp7_allow_flag vp7 support
23	RO	0x0	reserved
22	RO	0x1	avs_allow_flag avs support
21:20	RO	0x1	mvc_allow_flag mvc support
19	RO	0x0	reserved
18:17	RO	0x1	tile_mode_sel 0:no support 1: 8x4 support 2,3: no used
16:0	RO	0x0	reserved

VDPU_SWREG68

Address: Operational Base + offset (0x0110)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	sw_refbuf_sum_top sum of the top partitions
15:0	RO	0x0000	sw_refbuf_sum_bot sum of the bottom partitions

VDPU_SWREG69

Address: Operational Base + offset (0x0114)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	sw_refbuf_sum_hit sum of the refbufferd hits of the picture
15:0	RO	0x0000	sw_luma_sum_intra sum of the luminance 8x8 intra partitons of the picture.

VDPU_SWREG70

Address: Operational Base + offset (0x0118)

Bit	Attr	Reset Value	Description
31:22	RO	0x0	reserved
21:0	RO	0x000000	sw_ycomp_mv_sum sum of the decoded motion vector y-components

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VDPU_SWREG71

Address: Operational Base + offset (0x011c)

Bit	Attr	Reset Value	Description
31	RO	0x1	dec_mpeg2_allow 0:no support 1:support
30:29	RO	0x3	dec_vc1_allow 0 :not supported 1 :simple profile be supported 2 :main profile be supported 3 :advanced profile be supported
28	RO	0x1	dec_jpeg_allow 0:no support 1:support
27:26	RO	0x2	dec_mpeg4_allow 0 :not supported 1 :simple profile be supported 2 :advanced simple profile be supported
25:24	RO	0x3	dec_h264_allow 0:no support 1:baseline profile be supported 2:high profile be supported
23	RO	0x0	reserved
22	RO	0x0	dec_prog_jpeg_allow 0:no support 1:support
21	RO	0x1	outbuf_sel 0 : 1MB buffer be used 1 : 4MB buffer be used
20	RO	0x1	refbuf_exist 0 : not supported 1 : support
19:16	RO	0x5	dec_std_bus 0 : error 1 : AHB master, AHB slave 2 : OCP master, OCP slave 3 : AXI master, AXI slave 4 : AXI master, APB slave 5 : AXI master, AHB slave
15:14	RO	0x1	rtl_lan_sel 0: no used 1:vhdl 2:verilog

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Bit	Attr	Reset Value	Description
13:12	RO	0x2	bus_w 0 : error 1 : word bus 2 : double word bus 3 : quadruple word bus
11	RO	0x0	reserved
10:0	RO	0x780	sw_dec_max_allow_w the max width can be decoder

VDPU_SWREG72

Address: Operational Base + offset (0x0120)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RO	0x00	debug_service this value[6:0]=service_wr[2:0], service_rd[3:0]
23:0	RO	0x0	reserved

VDPU_SWREG73

Address: Operational Base + offset (0x0124)

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30	RO	0x0	debug_mv_req mvst_mv_req signal value
29	RO	0x0	debug_rlc_req prtr_res_y_req signal value
28	RO	0x0	debug_res_y_req prtr_res_y_req signal value
27	RO	0x0	debug_res_c_req debug_res_c_req
26	RO	0x0	debug_strm_da_e debug_strm_da_e
25	RO	0x0	debug_frm_rdy debug_frm_rdy
24	RO	0x0	debug_flt_req debug_flt_req
23	RO	0x0	debug_ref0_req debug_ref0_req
22	RO	0x0	debug_ref1_req debug_ref1_req
21	RO	0x0	reserved
20:0	RO	0x000000	debug_mb_cnt debug_mb_cnt

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VDPU_SWREG74

Address: Operational Base + offset (0x0128)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	h264_diff_mv_st_adr Differential motion vector base address used for h264 only it also reuse used as: [29:25] : 9st forward picid of inital reference pic list [24:20] : 8st forward picid of inital reference pic list [19:15] : 7st forward picid of inital reference pic list [14:10] : 6st forward picid of inital reference pic list [9:5] : 5st forward picid of inital reference pic list [4:0] : 4st forward picid of inital reference pic list
1:0	RO	0x0	reserved

VDPU_SWREG75

Address: Operational Base + offset (0x012c)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	h264_pred4x4_st_adr also be used as: [29:25] : 15st forward picid of inital reference pic list [24:20] : 14st forward picid of inital reference pic list [19:15] : 13st forward picid of inital reference pic list [14:10] : 12st forward picid of inital reference pic list [9:5] : 11st forward picid of inital reference pic list [4:0] : 10st forward picid of inital reference pic list
1:0	RO	0x0	reserved

VDPU_SWREG76

Address: Operational Base + offset (0x0130)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	h264_num_ref_idx1 the number of referance pic index1
15:0	RW	0x0000	h264_num_ref_idx0 the number of referance pic index0

VDPU_SWREG77

Address: Operational Base + offset (0x0134)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	h264_num_ref_idx3 the number of referance pic index3
15:0	RW	0x0000	h264_num_ref_idx2 the number of referance pic index2

VDPU_SWREG78

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Address: Operational Base + offset (0x0138)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	h264_num_ref_idx5 the number of referance pic index5
15:0	RW	0x0000	h264_num_ref_idx4 the number of referance pic index4

VDPU_SWREG79

Address: Operational Base + offset (0x013c)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	h264_num_ref_idx7 the number of referance pic index7
15:0	RW	0x0000	h264_num_ref_idx6 the number of referance pic index6

VDPU_SWREG80

Address: Operational Base + offset (0x0140)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	h264_num_ref_idx9 the number of referance pic index9
15:0	RW	0x0000	h264_num_ref_idx8 the number of referance pic index8

VDPU_SWREG81

Address: Operational Base + offset (0x0144)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	h264_num_ref_idx11 the number of referance pic index11
15:0	RW	0x0000	h264_num_ref_idx10 the number of referance pic index10

VDPU_SWREG82

Address: Operational Base + offset (0x0148)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	h264_num_ref_idx13 the number of referance pic index13
15:0	RW	0x0000	h264_num_ref_idx12 the number of referance pic index12

VDPU_SWREG83

Address: Operational Base + offset (0x014c)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	h264_num_ref_idx15 the number of referance pic index15

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Bit	Attr	Reset Value	Description
15:0	RW	0x0000	h264_num_ref_idx14 the number of referance pic index14

VDPU_SWREG84

Address: Operational Base + offset (0x0150)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	h264_ref0_st_addr the start address of referance frame0
1	RW	0x0	h264_ref0_field_en 0 : frame 1 : field
0	RW	0x0	h264_ref0_closer_sel 0 : bottom field be selected 1 : top field be selected

VDPU_SWREG85

Address: Operational Base + offset (0x0154)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	h264_ref1_st_addr the start address of referance frame1
1	RW	0x0	h264_ref1_field_en 0 : frame 1 : field
0	RW	0x0	h264_ref1_closer_sel 0 : bottom field be selected 1 : top field be selected

VDPU_SWREG86

Address: Operational Base + offset (0x0158)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	h264_ref2_st_addr the start address of referance frame2
1	RW	0x0	h264_ref2_field_en 0 : frame 1 : field
0	RW	0x0	h264_ref2_closer_sel 0 : bottom field be selected 1 : top field be selected

VDPU_SWREG87

Address: Operational Base + offset (0x015c)

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Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	h264_ref3_st_addr the start address of referance frame3
1	RW	0x0	h264_ref3_field_en 0 : frame 1 : field
0	RW	0x0	h264_ref3_closer_sel 0 : bottom field be selected 1 : top field be selected

VDPU_SWREG88

Address: Operational Base + offset (0x0160)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	h264_ref4_st_addr the start address of referance frame4
1	RW	0x0	h264_ref4_field_en 0 : frame 1 : field
0	RW	0x0	h264_ref4_closer_sel 0 : bottom field be selected 1 : top field be selected

VDPU_SWREG89

Address: Operational Base + offset (0x0164)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	h264_ref5_st_addr the start address of referance frame5
1	RW	0x0	h264_ref5_field_en 0 : frame 1 : field
0	RW	0x0	h264_ref5_closer_sel 0 : bottom field be selected 1 : top field be selected

VDPU_SWREG90

Address: Operational Base + offset (0x0168)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	h264_ref6_st_addr the start address of referance frame6
1	RW	0x0	h264_ref6_field_en 0 : frame 1 : field
0	RW	0x0	h264_ref6_closer_sel 0 : bottom field be selected 1 : top field be selected

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VDPU_SWREG91

Address: Operational Base + offset (0x016c)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	h264_ref7_st_addr the start address of referance frame7
1	RW	0x0	h264_ref7_field_en 0 : frame 1 : field
0	RW	0x0	h264_ref7_closer_sel 0 : bottom field be selected 1 : top field be selected

VDPU_SWREG92

Address: Operational Base + offset (0x0170)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	h264_ref8_st_addr the start address of referance frame8
1	RW	0x0	h264_ref8_field_en 0 : frame 1 : field
0	RW	0x0	h264_ref8_closer_sel 0 : bottom field be selected 1 : top field be selected

VDPU_SWREG93

Address: Operational Base + offset (0x0174)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	h264_ref9_st_addr the start address of referance frame9
1	RW	0x0	h264_ref9_field_en 0 : frame 1 : field
0	RW	0x0	h264_ref9_closer_sel 0 : bottom field be selected 1 : top field be selected

VDPU_SWREG94

Address: Operational Base + offset (0x0178)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	h264_ref10_st_addr the start address of referance frame10
1	RW	0x0	h264_ref10_field_en 0 : frame 1 : field

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Bit	Attr	Reset Value	Description
0	RW	0x0	h264_ref10_closer_sel 0 : bottom field be selected 1 : top field be selected

VDPU_SWREG95

Address: Operational Base + offset (0x017c)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	h264_ref11_st_addr the start address of referance frame11
1	RW	0x0	h264_ref11_field_en 0 : frame 1 : field
0	RW	0x0	h264_ref11_closer_sel 0 : bottom field be selected 1 : top field be selected

VDPU_SWREG96

Address: Operational Base + offset (0x0180)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	h264_ref12_st_addr the start address of referance frame12
1	RW	0x0	h264_ref12_field_en 0 : frame 1 : field
0	RW	0x0	h264_ref12_closer_sel 0 : bottom field be selected 1 : top field be selected

VDPU_SWREG97

Address: Operational Base + offset (0x0184)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	h264_ref13_st_addr the start address of referance frame13
1	RW	0x0	h264_ref13_field_en 0 : frame 1 : field
0	RW	0x0	h264_ref13_closer_sel 0 : bottom field be selected 1 : top field be selected

VDPU_SWREG98

Address: Operational Base + offset (0x0188)

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Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	h264_ref14_st_addr the start address of referance frame14
1	RW	0x0	h264_ref14_field_en 0 : frame 1 : field
0	RW	0x0	h264_ref14_closer_sel 0 : bottom field be selected 1 : top field be selected

VDPU_SWREG99

Address: Operational Base + offset (0x018c)

Bit	Attr	Reset Value	Description
31:2	RW	0x00000000	h264_ref15_st_addr the start address of referance frame15
1	RW	0x0	h264_ref15_field_en 0 : frame 1 : field
0	RW	0x0	h264_ref15_closer_sel 0 : bottom field be selected 1 : top field be selected

VDPU_SWREG100

Address: Operational Base + offset (0x0190)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:25	RW	0x00	h264_init_reflist_df5 used for h264
24:20	RW	0x00	h264_init_reflist_df4 used for h264
19:15	RW	0x00	h264_init_reflist_df3 used for h264
14:10	RW	0x00	h264_init_reflist_df2 used for h264
9:5	RW	0x00	h264_init_reflist_df1 used for h264
4:0	RW	0x00	h264_init_reflist_df0 used for h264

VDPU_SWREG101

Address: Operational Base + offset (0x0194)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:25	RW	0x00	h264_init_reflist_df11 used for h264

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Bit	Attr	Reset Value	Description
24:20	RW	0x00	h264_init_reflist_df10 used for h264
19:15	RW	0x00	h264_init_reflist_df9 used for h264
14:10	RW	0x00	h264_init_reflist_df8 used for h264
9:5	RW	0x00	h264_init_reflist_df7 used for h264
4:0	RW	0x00	h264_init_reflist_df6 used for h264

VDPU_SWREG102

Address: Operational Base + offset (0x0198)

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:15	RW	0x00	h264_init_reflist_df15 used for h264
14:10	RW	0x00	h264_init_reflist_df14 used for h264
9:5	RW	0x00	h264_init_reflist_df13 used for h264
4:0	RW	0x00	h264_init_reflist_df12 used for h264

VDPU_SWREG103

Address: Operational Base + offset (0x019c)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:25	RW	0x00	h264_init_reflist_db5 used for h264
24:20	RW	0x00	h264_init_reflist_db4 used for h264
19:15	RW	0x00	h264_init_reflist_db3 used for h264
14:10	RW	0x00	h264_init_reflist_db2 used for h264
9:5	RW	0x00	h264_init_reflist_db1 used for h264
4:0	RW	0x00	h264_init_reflist_db0 used for h264

VDPU_SWREG104

Address: Operational Base + offset (0x01a0)

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Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:25	RW	0x00	h264_init_reflist_db11 used for h264
24:20	RW	0x00	h264_init_reflist_db10 used for h264
19:15	RW	0x00	h264_init_reflist_db9 used for h264
14:10	RW	0x00	h264_init_reflist_db8 used for h264
9:5	RW	0x00	h264_init_reflist_db7 used for h264
4:0	RW	0x00	h264_init_reflist_db6 used for h264

VDPU_SWREG105

Address: Operational Base + offset (0x01a4)

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:15	RW	0x00	h264_init_reflist_db15 used for h264
14:10	RW	0x00	h264_init_reflist_db14 used for h264
9:5	RW	0x00	h264_init_reflist_db13 used for h264
4:0	RW	0x00	h264_init_reflist_db12 used for h264

VDPU_SWREG106

Address: Operational Base + offset (0x01a8)

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:15	RW	0x00	h264_init_reflist_pf3 Initial reference picture list for P forward picid 3
14:10	RW	0x00	h264_init_reflist_pf2 Initial reference picture list for P forward picid 2
9:5	RW	0x00	h264_init_reflist_pf1 Initial reference picture list for P forward picid 1
4:0	RW	0x00	h264_init_reflist_pf0 used in 264

VDPU_SWREG107

Address: Operational Base + offset (0x01ac)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	h264_refpic_term_flag long term flag for reference pictuure index

VDPU_SWREG108

Address: Operational Base + offset (0x01b0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	h264_refpic_valid_flag valid flag for reference picture index

VDPU_SWREG109

Address: Operational Base + offset (0x01b4)

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5:0	RW	0x00	h264_strm_start_bit assosiates with sw_rlc_vlc_st_adr

VDPU_SWREG110

Address: Operational Base + offset (0x01b8)

Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved
26:22	RW	0x00	h264_flt_offset_cr_qp filter offset of cr qp
21:17	RW	0x00	h264_flt_offset_cb_qp filter offset of cb qp
16:9	RW	0x00	h264_pic_mb_h value =((pixel height+15)/16). used for frame or single field size being decoded
8:0	RW	0x000	h264_pic_mb_w value = ((pixel width + 15) /16)

VDPU_SWREG111

Address: Operational Base + offset (0x01bc)

Bit	Attr	Reset Value	Description
31:18	RO	0x0	reserved
17:16	RW	0x0	h264_wp_bslice_sel 0 : default wp be used 1 : explicit wp be used 2 : implicit wp be used
15:5	RO	0x0	reserved
4:0	RW	0x00	h264_max_refnum this value is for decoded picture buffer

VDPU_SWREG112

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Address: Operational Base + offset (0x01c0)

Bit	Attr	Reset Value	Description
31	RW	0x0	h264_dblk_ctrl_flag to indicates if the slice header will have the deblocking filter's extra variables controlling characteristics
30	RW	0x0	h264_rpcp_flag to specifies whether redundant picture count syntax elements
29:21	RO	0x0	reserved
20:16	RW	0x00	h264_curfrm_len H.264: Bit length of frame_num in data stream
15:0	RW	0x0000	h264_curfrm_num it may be use for reference picture reordering and identify short-term reference frames

VDPU_SWREG113

Address: Operational Base + offset (0x01c4)

Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved
26:16	RW	0x000	h264_mk_len use for decoded reference picture
15:0	RW	0x0000	h264_idrp_id instantaneous decoding refresh picture id

VDPU_SWREG114

Address: Operational Base + offset (0x01c8)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	h264_pps_id it identifies the slice header will have the id of picture parameter set
23:19	RW	0x00	h264_max_refidx1 it will be used in decoding inter predicted macro blocks
18:14	RW	0x00	h264_max_refidx0 it will be used in decoding inter predicted macro blocks
13:8	RO	0x0	reserved
7:0	RW	0x00	h264_pocf_len the length of picture order count field in stream

VDPU_SWREG115

Address: Operational Base + offset (0x01cc)

Bit	Attr	Reset Value	Description
31:9	RO	0x0	reserved
8	RW	0x0	h264_idr_pic_flag instantaneous decoding refresh picture flag
7	RW	0x0	h264_dlmv_method_en with B_skip, B_Direct_16x16 and B_direct_8x8_inference_flag

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Bit	Attr	Reset Value	Description
6	RW	0x0	h264_monochr_en sampling format , 0 : 4:2:0 1 : 4:0:0
5	RW	0x0	h264_cabac_en enable for cabac
4	RW	0x0	h264_pslice_wp_en enable flag of Weighted prediction for P slices
3	RW	0x0	h264_nimb_intra_en 0 : neighbouring inter macroblocks are used in intra prediction process 1 : neighbouring intra macroblocks are used
2	RW	0x0	h264_tranf_flag_en_8x8 8x8 transform flag enable for stream decoding
1	RW	0x0	h264_scl_matrix_en 0 : normal transform 1 : use scaling matrix for transform
0	RW	0x0	h264_fieldpic_flag_exist Flag for streamd that field_pic_flag exists in stream

VDPU_SWREG120

Address: Operational Base + offset (0x01e0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mfr_reg0 MPEG4/JPEG/VC-1/MPEG2/VP7/VP: [31:2] RLC mode: Base address for RLC data VLC mode: Stream start address VP7: [31:2] This base address is used as sw_dct_strm0_base including DCT stream for MB rows 0,2n

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VDPU_SWREG121

Address: Operational Base + offset (0x01e4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mfr_reg1 vc-1: [31] : bitplane mode enable for corresponding element0 [30] : bitplane mode enable for corresponding element1 [29] : bitplane mode enable for corresponding element2 [28:24] : alemative PQUANT. [23:20] : weather dq_profile will be set to picture edges [19] : TTMB or TTFRM sel [18:14] : qpindex value [12] : enable for bilinear motion compensation ena [11] : enable for iform quantizer e [10] : enable for HALFQP [9:8] : frame level transform type sel [7] : the 2st byte of the stream emulation byte [6] : enable for antization parameter change inside frame [5] : enable for VC-1 advanced profile JPEG: [26:0] : progressive JPEG MPEG2 : [12] : enable for bilinear motion compensation VP7: [31:26] : DCT stream partition index 1 of start bit [25:20] : DCT stream partition index 2 of start bit [13] : rominance motion vector resolution for VP7/8 [12] : enable for bilinear motion compensation [11:9] : 0st count for DC prediction mach [8:6] : 1st count for DC prediction mach

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VDPU_SWREG122

Address: Operational Base + offset (0x01e8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mfr_reg2 MPEG4: [31:26] : Exact bit of stream start word [25] : enable for sync markers [24] : enable for Type 1 quantization [23:19] : the offset of Qp filter [18:14] : the offset of Qp filter for cr [0] : filed_pic_flag exists in stream JPEG : [31:26] : Exact bit of stream start word [25] : enable for sync markers [12:11] : total of Quantization tables [10:8] : the sampling format for input pic [7] : JPEG width [6] : weather current strem buffer contain the end of a JPEG image [5:0] : vlc table VC-1 : [31:26] : Exact bit of stream start word [25] : enable for sync markers [24] : Quantisation profile [23] : each mb take on quantization step size or not [22] : range reduced [20] : chrominance interpolation accuracy information [17:13] : select tables which be used to dec [12:10] : select mode syntax element table [9:7] : select mv table [6:4] : select CPBCY table [3:0] : block pattern table select

VDPU_SWREG123

Address: Operational Base + offset (0x01ec)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mfr_reg3 JPEG: [15:0] : start marker frequency. vc-1: [31:24] : B picture scl factor [23:19] : FWD direction reference distance [18:14] : BWD direction reference distance VP7/VP : [31:16] : value 0 for inital dc predictor [15:0] : value 1 for inital dc predictor

VDPU_SWREG124

Address: Operational Base + offset (0x01f0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mfr_reg4 MPEG4: [31:2] : MB ctrl start address VC-1: [24] : enable for 0st intensity compensation [23:16] : iscale value [15:0] : ishift value VP7/VP : [27:24] : coeffient partitions number [23:0] : total of CTRL stream data

VDPU_SWREG125

Address: Operational Base + offset (0x01f4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mfr_reg5 JPEG: [31:2] : Cb ACDC coeff start address VP7/vp: [31:22] : prediction filter with set 5 and tap 1 [21:12] : prediction filter with set 5 and tap 2 [11:2] : prediction filter with set 5 and tap 3

VDPU_SWREG126

Address: Operational Base + offset (0x01f8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mfr_reg6 JPEG: [31:2] : Cr ACDC coeff start address VP7/vp: [31:22] : prediction filter with set 6 and tap 0 [21:12] : prediction filter with set 6 and tap 1 [11:2] : prediction filter with set 6 and tap 2

VDPU_SWREG127

Address: Operational Base + offset (0x01fc)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mfr_reg7 VP7/vp: [31:22] : prediction filter with set 6 and tap 3 [21:12] : prediction filter with set 7 and tap 0 [11:2] : prediction filter with set 7 and tap 1

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VDPU_SWREG128

Address: Operational Base + offset (0x0200)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mfr_reg8 VP7/VP: [31:22] : prediction filter with set 7 and tap 2 [21:12] : prediction filter with set 7 and tap 3 [11:10] : extra prediction filter with set 2 and tap -1 [9:8] : extra prediction filter with set 2 and tap 4 [7:6] : extra prediction filter with set 4 and tap -1 [5:4] : extra prediction filter with set 4 and tap 4 [3:2] : extra prediction filter with set 6 and tap -1 [1:0] : extra prediction filter with set 6 and tap 4

VDPU_SWREG129

Address: Operational Base + offset (0x0204)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mfr_reg9

VDPU_SWREG130

Address: Operational Base + offset (0x0208)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mfr_reg10 VP7: [21:11] : QP0 for VP7 [10:0] : QP1 for VP7

VDPU_SWREG131

Address: Operational Base + offset (0x020c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mfr_reg11 MPEG4/H263/VC-1/VP7: [31:2] : reference pic0 start address JPEG: [31:2] : the ch decoder output start address

VDPU_SWREG132

Address: Operational Base + offset (0x0210)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mfr_reg12 VP7: [31] : type of loop filter [30:28] : sharpness of loop filter [27:21] : MB type0 adjustment of filter level [20:14] : MB type1 adjustment of filter level [13:7] : MB type2 adjustment of filter level [6:0] : MB type3 adjustment of filter level

VDPU_SWREG133

Address: Operational Base + offset (0x0214)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mfr_reg13 VP7: [27:21] : reference frame type0 adjustment of filter level [20:14] : reference frame type1 adjustment of filter level [13:7] : reference frame type2 adjustment of filter level [6:0] : reference frame type3 adjustment of filter level

VDPU_SWREG134

Address: Operational Base + offset (0x0218)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mfr_reg14 MPEG4/vc1/MEPG2: [31:2] : reference pic2 start address JPEG: [30:24] : code words of length 6 [21:16] : code words of length 5 [15:11] : code words of length 4 [10:7] : code words of length 3 [5:3] : code words of length 2 [1:0] : code words of length 1

VDPU_SWREG135

Address: Operational Base + offset (0x021c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mfr_reg15 MPEG4/vc1/MEPG2: [31:2] : reference pic3 start address JPEG: [30:24] : code words of length 10 [23:16] : code words of length 9 [15:8] : code words of length 8 [7:0] : code words of length 7

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VDPU_SWREG136

Address: Operational Base + offset (0x0220)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mfr_reg16 VP7 [31:2] : golden reference pic start address(PIC_ID 4) [0] : golden reference pic siggn bias(VP7/VP8) VC-1: [31:16] : length of picture header [13] : 1/4 MV/MB sel [11] : enable for ref pic range reduce [10:9] : max different mv length [7:6] : select range for mv [5] : enable for overlap smoothing [4:3] : MB overlap smoothing method MPEG4/MPEG2: [19] : alternalte scan flag [18:15] : HRZ AXI's bit amount for representing FWD MV [14:11] : VRZ AXI's bit amount for representing FWD MV [10:7] : HRZ AXI's bit amount for representing BWD MV [6:3] : VRZ AXI's bit amount for representing BWD MV [2] : FWD MV Y resolution [1] : the ctrl bit for rounding(MPEG4),BWD MV Y resolution(MPEG2) [0] : pic type of previous anchor(MPEG4) JPEG: [30:24] : code words of length 14 [23:16] : code words of length 13 [15:8] : code words of length 12 [7:0] : code words of length 11

VDPU_SWREG137

Address: Operational Base + offset (0x0224)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mfr_reg17 MPEG4: [26:0] : reference distance syntax for delta value0 be used JPEG: [31:27] : tab2:code words of length 4 [26:23] : tab2:code words of length 3 [21:19] : tab2:code words of length 2 [17:16] : tab2:code words of length 1 [15:8] : tab1:code words of length 16 [7:0] : tab1:code words of length 15 VC-1: [24] : enable for intensity compensation 3 [23:16] : intensity compensation's iscale value [15:0] : intensity compensation's ishift value VP7: [29:24] : 1st coef of scan read index [23:18] : 2st coef of scan read index [17:12] : 3st coef of scan read index [11:6] : 4st coef of scan read index [5:0] : 5st coef of scan read index

VDPU_SWREG138

Address: Operational Base + offset (0x0228)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mfr_reg18 MPEG4: [26:0] : reference distance syntax for delta value -1 be used JPEG: [31:24] : tab2:code words of length 8 [23:16] : tab2:code words of length 7 [14:8] : tab2:code words of length 6 [5:0] : tab2:code words of length 5 VC-1: [24] : enable for intensity compensation 4 [23:16] : intensity compensation's iscale value [15:0] : intensity compensation's shift value VP7: [29:24] : 6st coef of scan read index [23:18] : 7st coef of scan read index [17:12] : 8st coef of scan read index [11:6] : 9st coef of scan read index [5:0] : 10st coef of scan read index

VDPU_SWREG139

Address: Operational Base + offset (0x022c)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mfr_reg19 MPEG4: [26:0] : reference distance syntax for delta value1 be used JPEG: [31:24] : tab2:code words of length 12 [23:16] : tab2:code words of length 11 [15:8] : tab2:code words of length 10 [7:0] : tab2:code words of length 9 VP7: [29:24] : 11st coef of scan read index [23:18] : 12st coef of scan read index [17:12] : 13st coef of scan read index [11:6] : 14st coef of scan read index [5:0] : 15st coef of scan read index

VDPU_SWREG140

Address: Operational Base + offset (0x0230)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mfr_reg20 JPEG: [31:24] : tab2:code words of length 16 [23:16] : tab2:code words of length 15 [15:8] : tab2:code words of length 14 [7:0] : tab2:code words of length 13 VP7: [31:2] : DCT stream MB row 2,2n+1 start address

VDPU_SWREG141

Address: Operational Base + offset (0x0234)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mfr_reg21 JPEG: [31:28] : tab1:code words of length 8 [27:24] : tab1:code words of length 7 [23:20] : tab1:code words of length 6 [19:16] : tab1:code words of length 5 [15:12] : tab1:code words of length 4 [11:8] : tab1:code words of length 3 [6:4] : tab1:code words of length 2 [1:0] : tab1:code words of length 1 VP7 [31:2] : DCT stream MB row 2,2n+2 start address

VDPU_SWREG142

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Address: Operational Base + offset (0x0238)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mfr_reg22 JPEG: [31:28] : tab1:code words of length 16 [27:24] : tab1:code words of length 15 [23:20] : tab1:code words of length 14 [19:16] : tab1:code words of length 13 [15:12] : tab1:code words of length 12 [11:8] : tab1:code words of length 11 [6:4] : tab1:code words of length 10 [1:0] : tab1:code words of length 9 VP7 [31:2] : DCT stream MB row 2,2n+3 start address

VDPU_SWREG143

Address: Operational Base + offset (0x023c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mfr_reg23 JPEG: [31:28] : tab2:code words of length 8 [27:24] : tab2:code words of length 7 [23:20] : tab2:code words of length 6 [19:16] : tab2:code words of length 5 [15:12] : tab2:code words of length 4 [11:8] : tab2:code words of length 3 [6:4] : tab2:code words of length 2 [1:0] : tab2:code words of length 1 VP7 [31:2] : DCT stream MB row 2,2n+4 start address

VDPU_SWREG144

Address: Operational Base + offset (0x0240)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mfr_reg24 JPEG: [31:28] : tab2:code words of length 16 [27:24] : tab2:code words of length 15 [23:20] : tab2:code words of length 14 [19:16] : tab2:code words of length 13 [15:12] : tab2:code words of length 12 [11:8] : tab2:code words of length 11 [6:4] : tab2:code words of length 10 [1:0] : tab2:code words of length 9 VP7 [31:2] : DCT stream MB row 2,2n+5 start address

VDPU_SWREG145

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Address: Operational Base + offset (0x0244)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mfr_reg25 JPEG: [31:28] : tab3:code words of length 8 [27:24] : tab3:code words of length 7 [23:20] : tab3:code words of length 6 [19:16] : tab3:code words of length 5 [15:12] : tab3:code words of length 4 [11:8] : tab3:code words of length 3 [6:4] : tab2:code words of length 2 [1:0] : tab3:code words of length 1 VC-1: [31:2] : bitplane mb ctrl start address VP7: [31:2] : ctrl data stream start address

VDPU_SWREG146

Address: Operational Base + offset (0x0248)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mfr_reg26 JPEG: [31:28] : tab3:code words of length 16 [27:24] : tab3:code words of length 15 [23:20] : tab3:code words of length 14 [19:16] : tab3:code words of length 13 [15:12] : tab3:code words of length 12 [11:8] : tab3:code words of length 11 [6:4] : tab3:code words of length 10 [1:0] : tab3:code words of length 9 VP7 [31:2] : DCT stream MB row 2,2n+6 start address

VDPU_SWREG147

Address: Operational Base + offset (0x024c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mfr_reg27 VP7 [31:2] : DCT stream MB row 2,2n+7 start address

VDPU_SWREG148

Address: Operational Base + offset (0x0250)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mfr_reg28 MPEG4/VC-1/MPEG2/VP7: [31:2] : ref pic index 1 start address JPEG: [7:0] : snapshot

VDPU_SWREG149

Address: Operational Base + offset (0x0254)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mfr_reg29 VC-1: [24] : enable for intensity compensation 1 [23:16] : intensity compensation iscale value [15:0] : intensity compensation ishift value VP7: [31:2] : the segmentation map value start address [1] : enable for segmentation map update [0] : enable for segmentation

VDPU_SWREG150

Address: Operational Base + offset (0x0258)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mfr_reg30 VC-1: [24] : enable for intensity compensation 2 [23:16] : intensity compensation iscale value [15:0] : intensity compensation ishift value VP7: [29:24] : DCT stream partition index 3 of start bit [23:18] : DCT stream partition index 4 of start bit [17:12] : DCT stream partition index 5 of start bit [11:6] : DCT stream partition index 6 of start bit [5:0] : DCT stream partition index 7 of start bit

VDPU_SWREG151

Address: Operational Base + offset (0x025c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mfr_reg31 VP7: [21:11] : QP2 for VP7 [10:0] : QP3 for VP7

VDPU_SWREG152

Address: Operational Base + offset (0x0260)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mfr_reg32 VP7: [21:11] : QP4 for VP7 [10:0] : QP5 for VP7

VDPU_SWREG153

Address: Operational Base + offset (0x0264)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mfr_reg33 VC-1/VP7: [31:22] : prediction filter with set 0,tap3 (also for mpeg4) [21:12] : prediction filter with set 1,tap0 [11:2] : prediction filter with set 1,tap1

VDPU_SWREG154

Address: Operational Base + offset (0x0268)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mfr_reg34 VC-1/VP7: [31:22] : prediction filter with set 1,tap2 [21:12] : prediction filter with set 1,tap3 [11:2] : prediction filter with set 2,tap0(no for vc-1)

VDPU_SWREG155

Address: Operational Base + offset (0x026c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mfr_reg35 VC-1/VP7: [31:22] : prediction filter with set 2,tap1 [21:12] : prediction filter with set 2,tap2 [11:2] : prediction filter with set 2,tap3

VDPU_SWREG156

Address: Operational Base + offset (0x0270)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mfr_reg36 VP7: [31:22] : prediction filter with set 3,tap0 [21:12] : prediction filter with set 3,tap1 [11:2] : prediction filter with set 3,tap2

VDPU_SWREG157

Address: Operational Base + offset (0x0274)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mfr_reg37 VP7: [31:22] : prediction filter with set 3,tap3 [21:12] : prediction filter with set 4,tap0 [11:2] : prediction filter with set 4,tap1

VDPU_SWREG158

Address: Operational Base + offset (0x0278)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mfr_reg38 VP7: [31:22] : prediction filter with set 4,tap2 [21:12] : prediction filter with set 4,tap3 [11:2] : prediction filter with set 5,tap0

VDPU_SWREG164_PERF_LATENCY_CTRL0

Address: Operational Base + offset (0x0290)

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:8	RW	0x000	sw_rd_latency_thr
7:4	RW	0x0	sw_rd_latency_id
3	RW	0x0	sw_axi_cnt_type sw_axi_cnt_type
2	RW	0x0	sw_axi_perf_frm_type 1'b0: clear by frame end 1'b1: clear by software configuration
1	W1C	0x0	sw_axi_perf_clr_e 1'b0: software clear disable 1'b1: software clear enalbe
0	RW	0x0	sw_axi_perf_work_e 1'b0: disable 1'b1: enable

VDPU_SWREG165_PERF_LATENCY_CTRL1

Address: Operational Base + offset (0x0294)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:8	RW	0x0	sw_aw_count_id sw_aw_count_id
7:4	RW	0x0	sw_ar_count_id sw_ar_count_id
3	RW	0x0	sw_aw_cnt_id_type sw_aw_cnt_id_type

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Bit	Attr	Reset Value	Description
2	RW	0x0	sw_ar_cnt_id_type sw_ar_cnt_id_type
1:0	RW	0x0	sw_addr_align_type sw_addr_align_type

VDPU_SWREG166_PERF_RD_MAX_LATENCY_NUM0

Address: Operational Base + offset (0x0298)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RO	0x0000	rd_max_latency_num_ch0

VDPU_SWREG167_PERF_RD_LATENCY_SAMP_NUM

Address: Operational Base + offset (0x029c)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rd_latency_thr_num_ch0

VDPU_SWREG168_PERF_RD_LATENCY_ACC_SUM

Address: Operational Base + offset (0x02a0)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rd_latency_acc_sum

VDPU_SWREG169_PERF_RD_AXI_TOTAL_BYTE

Address: Operational Base + offset (0x02a4)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	perf_rd_axi_total_byte perf_rd_axi_total_byte

VDPU_SWREG170_PERF_WR_AXI_TOTAL_BYTE

Address: Operational Base + offset (0x02a8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	perf_wr_axi_total_byte perf_wr_axi_total_byte

VDPU_SWREG171_PERF_WORKING_CNT

Address: Operational Base + offset (0x02ac)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	perf_working_cnt perf_working_cnt

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4.4.11 VPU121 MMU Register Summary

Name	Offset	Size	Reset Value	Description
VCODEC_MMU_DTE_ADDR	0x0000	W	0x00000000	MMU current page Table addressIt is only can be written when MMU state is disable or page fault or mmu enable stall state
VCODEC_MMU_STATUS	0x0004	W	0x00000018	MMU status register
VCODEC_MMU_COMMAND	0x0008	W	0x00000000	MMU command register
VCODEC_MMU_PAGE_FAULT_ADDR	0x000c	W	0x00000000	MMU logical address of last page fault
VCODEC_MMU_ZAP_ONE_LINE	0x0010	W	0x00000000	MMU Zap cache line register
VCODEC_MMU_INT_RAWSTAT	0x0014	W	0x00000000	MMU raw interrupt status register
VCODEC_MMU_INT_CLEAR	0x0018	W	0x00000000	MMU raw interrupt status register
VCODEC_MMU_INT_MASK	0x001c	W	0x00000000	MMU raw interrupt status register
VCODEC_MMU_INT_STATUS	0x0020	W	0x00000000	MMU raw interrupt status register
VCODEC_MMU_AUTO_GATING	0x0024	W	0x00000001	mmu auto gating

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

4.4.12 VPU121 MMU Detail Register Description

VCODEC_MMU_DTE_ADDR

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MMU_DTE_ADDR MMU current page Table address

VCODEC_MMU_STATUS

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:11	RO	0x0	reserved
10:6	RO	0x00	PAGE_FAULT_BUS_ID Index of master reponsible for last page fault
5	RO	0x0	PAGE_FAULT_IS_WRITE The direction of access for last page fault: 0 = Read 1 = Write
4	RO	0x1	REPLAY_BUFFER_EMPTY 1'b1:The MMU replay buffer is empty

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Bit	Attr	Reset Value	Description
3	RO	0x1	MMU_IDLE The MMU is idle when accesses are being translated and there are no unfinished translated accesses. 1'b1: MMU is idle
2	RO	0x0	STAIL_ACTIVE MMU stall mode currently enabled. The mode is enabled by command 1'b1: MMU is in stall active status
1	RO	0x0	PAGE_FAULT_ACTIVE MMU page fault mode currently enabled . The mode is enabled by command. 1'b1: page fault is active
0	RO	0x0	PAGING_ENABLED 1'b0: paging is disabled 1'b1: Paging is enabled

VCODEC_MMU_COMMAND

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:3	RO	0x0	reserved
2:0	WO	0x0	MMU_CMD MMU_CMD. This can be: 0: MMU_ENABLE_PAGING 1: MMU_DISABLE_PAGING 2: MMU_ENABLE_STALL 3: MMU_DISABLE_STALL 4: MMU_ZAP_CACHE 5: MMU_PAGE_FAULT_DONE 6: MMU_FORCE_RESET

VCODEC_MMU_PAGE_FAULT_ADDR

Address: Operational Base + offset (0x000c)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	PAGE_FAULT_ADDR address of last page fault

VCODEC_MMU_ZAP_ONE_LINE

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	MMU_ZAP_ONE_LINE address to be invalidated from the page table cache

VCODEC_MMU_INT_RAWSTAT

Address: Operational Base + offset (0x0014)

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Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x0	READ_BUS_ERROR read bus error status
0	RW	0x0	PAGE_FAULT page fault status

VCODEC_MMU_INT_CLEAR

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	WO	0x0	READ_BUS_ERROR write 1 to clear read bus error
0	WO	0x0	PAGE_FAULT write 1 to page fault clear

VCODEC_MMU_INT_MASK

Address: Operational Base + offset (0x001c)

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x0	READ_BUS_ERROR enable the read bus interrupt souce when this bit is set to 1'b1
0	RW	0x0	PAGE_FAULT enable the page fault interrupt souce when this bit is set to 1'b1

VCODEC_MMU_INT_STATUS

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RO	0x0	READ_BUS_ERROR 1'b1:read bus error status
0	RO	0x0	PAGE_FAULT 1'b1:page fault

VCODEC_MMU_AUTO_GATING

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x1	mmu_auto_clkgating when it is 1'b1, the mmu will auto gating it self

4.4.13 VDPU121 CACHE Register Summary

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Name	Offset	Size	Reset Value	Description
pref_cache_VERSION	0x0000	W	0xcac20101	VERSION register
pref_cache_SIZE	0x0004	W	0x06110206	L2 cache SIZE
pref_cache_STATUS	0x0008	W	0x00000000	Status register
pref_cache_COMMAND	0x0010	W	0x00000000	Command setting register
pref_cache_CLEAR_PAGE	0x0014	W	0x00000000	clear page register
pref_cache_MAX_READS	0x0018	W	0x0000001c	maximum read register
pref_cache_PERFCNT_SRC0	0x0020	W	0x00000000	performance counter 0 source register
pref_cache_PERFCNT_VAL0	0x0024	W	0x00000000	performance counter 0 value register
pref_cache_PERFCNT_SRC1	0x0028	W	0x00000000	This register holds all the possible source values for Performance Counter 00: total clock cycles1: active clock cycles2: read transactions, master3: word reads, master4: read transactions, slave5: word reads, slave6: read hit, slave7: read misses, slave8: read invalidates, slave9: cacheable read transactions, slave10: bad hit nmber, slave
pref_cache_PERFCNT_VAL1	0x002c	W	0x00000000	performance counter 1 value register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

4.4.14 VDPU121 CACHE Detail Register Description

pref_cache_VERSION

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	RO	0xcac2	PRODUCT_ID Field0000 Description
15:8	RO	0x01	VERSION_MAJOR Field0000 Description
7:0	RO	0x01	VERSION_MINOR Field0000 Description

pref_cache_SIZE

Address: Operational Base + offset (0x0004)

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Bit	Attr	Reset Value	Description
31:24	RO	0x06	External_bus_width Log2 external bus width in bits
23:16	RO	0x11	CACHE_SIZE Log2 cache size in bytes
15:8	RO	0x02	ASSOCIATIVITY Log2 associativity
7:0	RO	0x06	LINE_SIZE Log2 line size in bytes

pref_cache_STATUS

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RO	0x0	DATA_BUSY set when the cache is busy handling data
0	RO	0x0	CMD_BUSY set when the cache is busy handling commands

pref_cache_COMMAND

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5:4	RW	0x0	sw_addrb_sel 2'b00: to sel b[14:6] 2'b01: to sel b[15:9], b[7:6] 2'b10: to sel b[16:10], b[7:6] 2'b11: to sel b[17:11], b[7:6]
3	RO	0x0	reserved
2:0	WO	0x0	COMMAND The possible command is 1 = Clear entire cache

pref_cache_CLEAR_PAGE

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	CLEAR_PAGE writing an address, invlidates all lines in that page from the cache

pref_cache_MAX_READS

Address: Operational Base + offset (0x0018)

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Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4:0	RW	0x1c	MAX_READS Limit the number of outstanding read transactions to this amount

pref_cache_PERFCNT_SRC0

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3:0	RW	0x0	PERFCNT_SRC0 This register holds all the possible source values for Performance Counter 0 0: total clock cycles 1: active clock cycles 2: read transactions, master 3: word reads, master 4: read transactions, slave 5: word reads, slave 6: read hit, slave 7: read misses, slave 8: read invalidates, slave 9: cacheable read transactions, slave 10: bad hit nmber, slave

pref_cache_PERFCNT_VAL0

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PERFCNT_VAL0 Performance counter 0 value

pref_cache_PERFCNT_SRC1

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
3:0	RW	0x0	PERFCNT_SRC1 This register holds all the possible source values for Performance Counter 1 0: total clock cycles 1: active clock cycles 2: read transactions, master 3: word reads, master 4: read transactions, slave 5: word reads, slave 6: read hit, slave 7: read misses, slave 8: read invalidates, slave 9: cacheable read transactions, slave 10: bad hit nmber, slave

pref_cache_PERFCNT_VAL1

Address: Operational Base + offset (0x002c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PERFCNT_VAL1 Performance counter 1 value

4.5 Application Notes

4.5.1 HEVC Configuration flow

1.Write the hevc_vpu_sel bit in the GRF_SOC_CONx register with "1" to choose HEVC to work.
2.Prepare the data in the DDR.
3.Set the HEVC general system configuration in HEVC.swreg2, such as working mode, in/out endian.
4.Set the picture parameters with HEVC.swreg3.
5.Set the input and output data base address and HEVC reference configuration with HEVC.swreg4~HEVC.swreg43.
6.If CABAC error detection is desired, set the HEVC.swreg44 to enable the corresponding error detection.
7.Set the interrupt configuration and start the HEVC with HEVC.swreg1.
8.Wait for the frame interrupt, and then get the processed results in the target DDR
9.Clear all the interrupts, and repeat Process2~Process8 to start a new frame decoding if the decoding is not finished yet.

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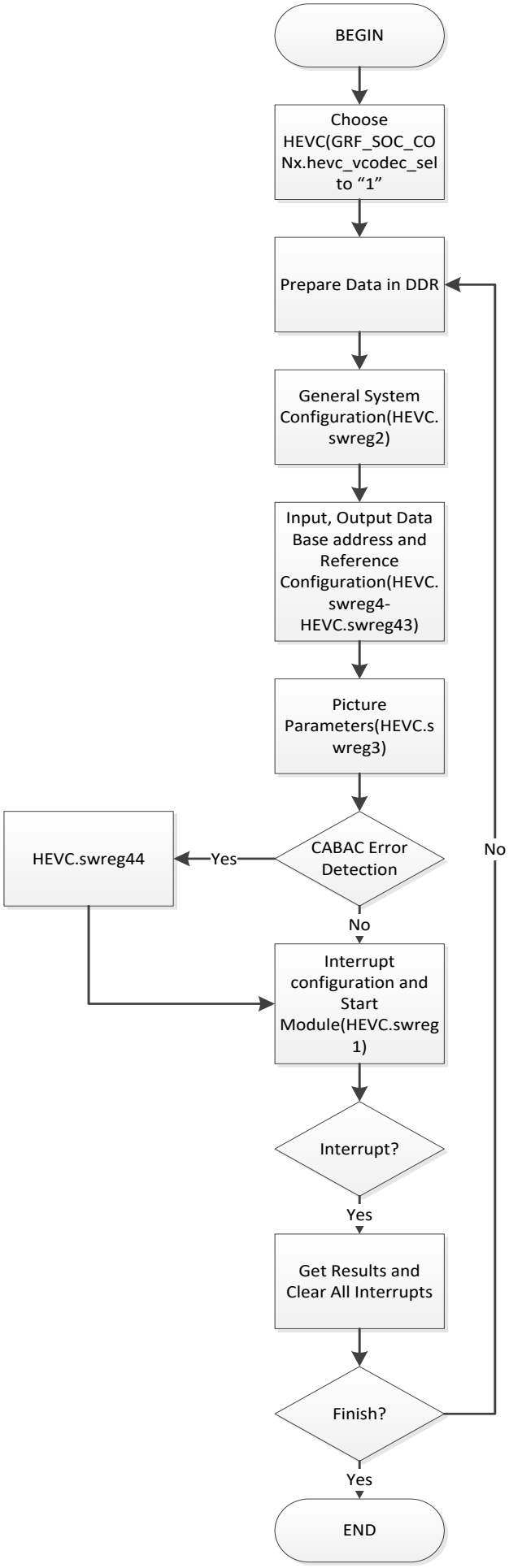

BEGIN
Choose HEVC(GRF_SOC_CONx.hevc_vcodec_sel to “1”
Prepare Data in DDR
General System Configuration(HEVC.swreg2)
Input, Output Data Base address and Reference Configuration(HEVC.swreg4-HEVC.swreg43)
Picture Parameters(HEVC.swreg3)
CABAC Error Detection
Yes
HEVC.swreg44
No
No
Interrupt configuration and Start Module(HEVC.swreg1)
Interrupt?
Yes
Get Results and Clear All Interrupts
Finish?
Yes
END

Fig. 4-6 HEVC Common Configuration Flow

4.5.2 VPU121 Configuration flow

1.Because HEVC and VPU share the same memory and ahb bus and some of axi bus, we should set the hevc_vpu_sel bit in GRF_SOC_CONx to 1'b0 to select VPU to work.
2.Prepare the decoder data in the DDR memory, And in decoder other than JPEG decoder, the input stream buffer should at least contain a slice or a frame data, otherwise the decoder will produce an interrupt and show error and then reset itself.
3.Config all the registers will be used. and please notice that which be list as follows:

- In encoder----- We can configure the registers to control the input picture data format (such as endian and swap), but some input data format are fixed, such as cabac_table data. And the register VEPU_SWREG64~95 are JPEG quantization registers. They are write only registers. When you want to write these registers, you should first set VEPU_SWREG14[0] to 1'b0 and VEPU_SWREG14[2:1] to 2'b10(select JPEG mode).
- In decoder---- The decoder can support ref buffer mode or cacheable mode, but they can't be both enabled. We can config the swreg57[6],swreg57[7] to enable cache and config the swreg51 to control the ref buffer.

4.You should config VDPU_SWREG1[0] as 1'b1 to enable video decoder. And config VDPU_SWREG60[0] as 1'b1 to enable pp. If pp performed in pipeline with decoder, you should config VDPU_SWREG60[1] as 1'b1 and then config VDPU_SWREG1[0] as 1'b1 to enable decoder and pp. VEPU_SWREG14[0] set to 1'b1 to enable encoder.
5.Wait for the frame interrupt,and then check if the frame decoder ready interrupt is right or not, after that,you can get the processed results in the target DDR
6.Clear all the interrupts,repeat step 2~5 to start a new frame decoder or encoder.

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Chapter 5 Video Input Processor (VIP)

5.1 Overview

The Video Input Processor, receives the data from Camera or CCIR656 encoder, and transfers the data into system main memory by AXI bus.
The Video Input Processor supports following features:

- Support YCbCr422 8bit input
- Support Raw 8bit/10bit/12bit input
- Support CCIR656(PAL/NTSC) input
- Support JPEG input
- Support YCbCr422/420 output
- Support UYVY/VYUY/YUYV/YVYU configurable
- Support up to 8192x8192 resolution source
- Support picture in picture
- Support arbitrary size window crop
- Support error/terminate interrupt and combined interrupt output
- Support clk/vsync/href polarity configurable
- Support one frame stop/ping-pong mode
- Support mmu

5.2 Block Diagram

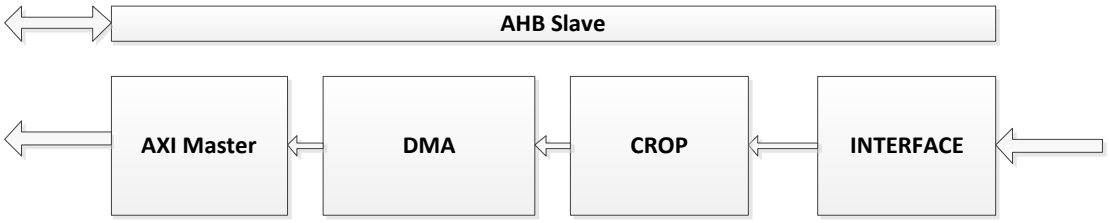


Fig. 5-1 VIP block diagram

The VIP comprises with:

- AHB Slave
- Host configure the registers via the AHB Slave
- AXI Master
- Transmit the data to chip memory via the AXI Master
- INTERFACE
- Translate the input video data into the requisite data format
- CROP
- Bypass or crop the source video data to a smaller size destination
- DMA
- Control the operation of AXI Master

5.3 Function Description

This chapter is used to illustrate the operational behavior of how VIP works. If YUV422 or ccir656 signal is received from external devices, VIP translate it into YUV422/420 data, and separate the data to Y and UV data, then store them to different memory via AXI bus separately. But if raw data is received, there are not any translations happened, the 8 data is considered as 16bit data and write directly to memory.

5.3.1 Support Vsync high active or low active

- Vsync Low active as below

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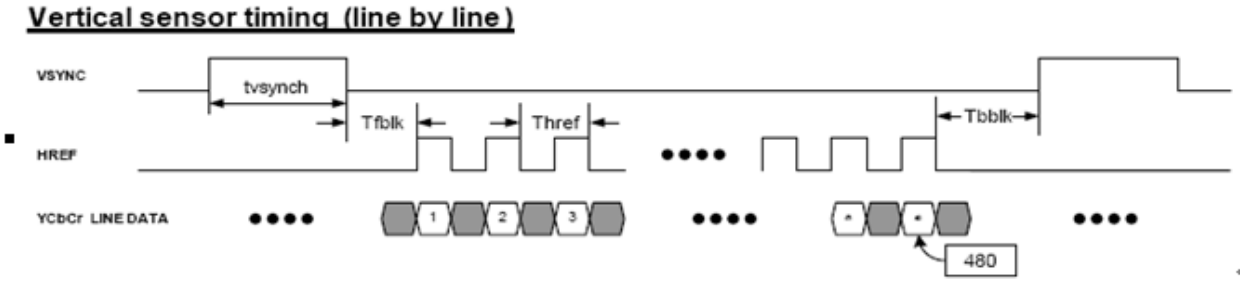


Fig. 5-2 Timing diagram for VIP when vsync low active

- Vsync High active

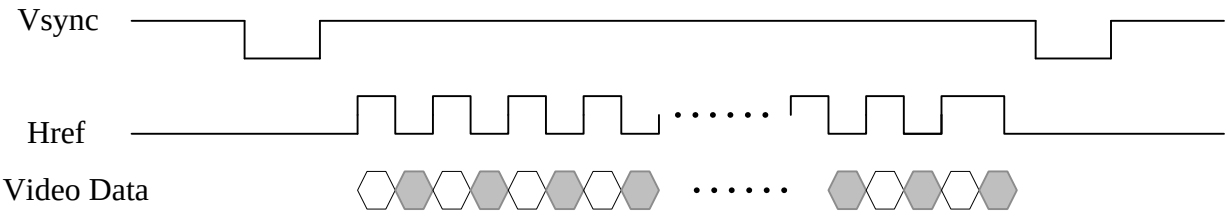


Fig. 5-3 Timing diagram for VIP when vsync high active

5.3.2 Support href high active or low active

- Href high active

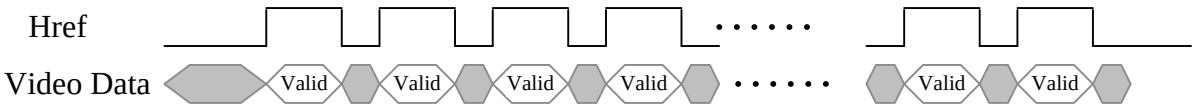


Fig. 5-4 Timing diagram for VIP when href high active

- Href Low active

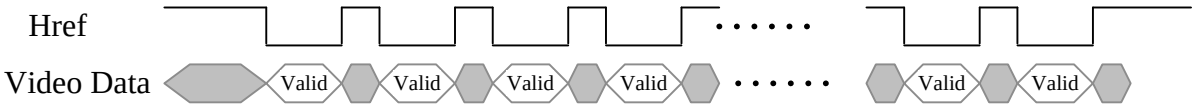


Fig. 5-5 Timing diagram for VIP when href low active

- Y first

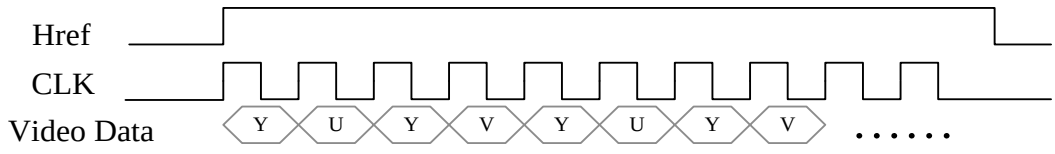


Fig. 5-6 Timing diagram for VIP when Y data first

- U first

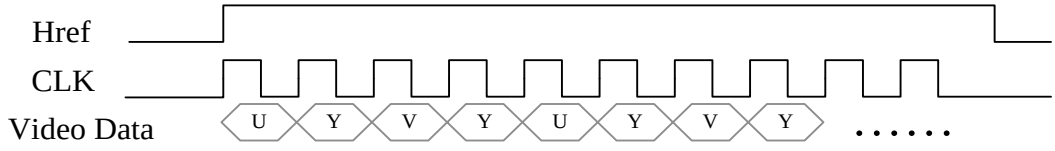


Fig. 5-7 Timing diagram for VIP when U data first

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5.3.3 Support CCIR656 (NTSC and PAL)

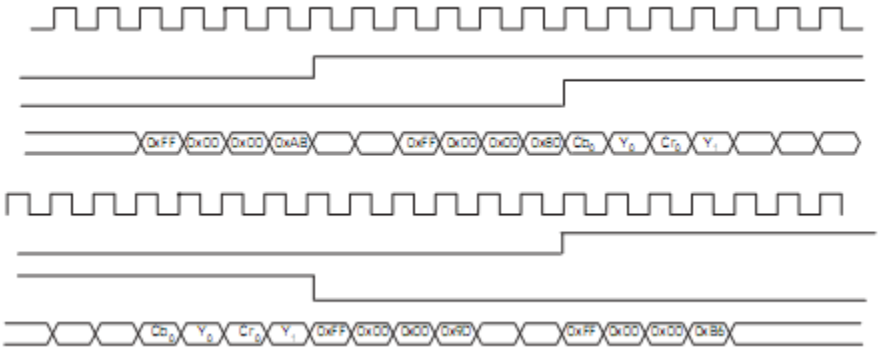


Fig. 5-8 CCIR656 timing

5.3.4 Support Raw data (8-bit) or JPEG

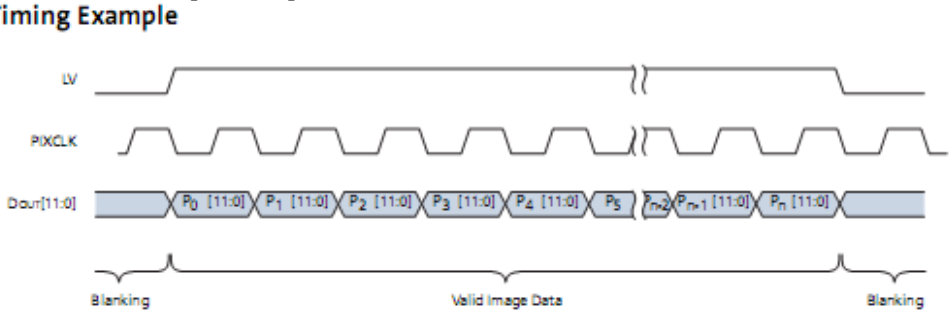


Fig. 5-9 Raw Data or JPEG Timing

VIP module can work in three modes: one frame stop mode, ping-pong mode.

One frame stop mode

In this mode, configure the parameter WORK_MODE to one frame stop mode. After one frame captured, VIP will automatic stop. After capturing, the image Y, UV data will be stored at main memory location defined by VIP_FRM0_ADDR_Y, FRM0_ADDR_UV separately.

Ping-Pong mode

After one frame(F1) captured, VIP will start to capture the next frame(F2) automatically, and host must assign new address pointer of frame1 and clear the frame1 status, thus VIP will capture the third frame automatically(by new F1 address) without any stop and so on for the following frames. But if host did not update the frame buffer address, the VIP will cover the pre-frame data stored in the memory with the following frame data.

Storage

Difference between the YUV mode and raw mode is that in the YUV mode or ccir656 mode, data will be storage in the Y data buffer and UV data buffer; but in the raw or jpeg mode, RGB data will be storage in the same buffer. In addition, in the yuv mode, the width of Y, U or V data is a byte in memory; in Raw or JPEGE mode, the width is a halfword no matter the data source is 8 bit.

CROP

The parameter START_Y and START_X defines the coordinate of crop start point. And the frame size after cropping is following the value of SET_WIDTH and SET_HEIGHT.

5.4 Register Description

5.4.1 Registers Summary

Name	Offset	Size	Reset Value	Description
VIP_CTRL	0x0000	W	0x00000000	VIP control
VIP_INTEN	0x0004	W	0x00000000	VIP interrupt status
VIP_INTSTAT	0x0008	W	0x00000000	VIP interrupt status

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Name	Offset	Size	Reset Value	Description
VIP_FOR	0x000c	W	0x00000000	VIP format
VIP_FRM0_ADDR_Y	0x0014	W	0x00000000	VIP frame0 y address
VIP_FRM0_ADDR_UV	0x0018	W	0x00000000	VIP frame0 uv address
VIP_FRM1_ADDR_Y	0x001c	W	0x00000000	VIP frame1 y address
VIP_FRM1_ADDR_UV	0x0020	W	0x00000000	VIP frame1 uv address
VIP_VIR_LINE_WIDTH	0x0024	W	0x00000000	VIP virtual line width
VIP_SET_SIZE	0x0028	W	0x000002d0	VIP frame set size
VIP_CROP	0x0044	W	0x00000000	VIP crop start point
VIP_SCL_CTRL	0x0048	W	0x00000000	CIF scale control
VIP_FIFO_ENTRY	0x0054	W	0x00000000	VIP FIFO entry
VIP_FRAME_STATUS	0x0060	W	0x00000000	VIP frame status
VIP_CUR_DST	0x0064	W	0x00000000	VIP current destination address
VIP_LAST_LINE	0x0068	W	0x00000000	VIP last frame line number
VIP_LAST_PIX	0x006c	W	0x00000000	VIP last line pixel number
VIP_DTE_ADDR	0x0800	W	0x00000000	MMU current page Table address.It is only can be written when MMU state is disable or page fault or mmu enable stall state
VIP_STATUS	0x0804	W	0x00000000	MMU status register
VIP_COMMAND	0x0808	W	0x00000000	MMU command register
VIP_PAGE_FAULT_ADDR	0x080c	W	0x00000000	MMU logical address of last page fault
VIP_ZAP_ONE_LINE	0x0810	W	0x00000000	MMU Zap cache line register
VIP_INT_RAWSTAT	0x0814	W	0x00000000	MMU raw interrupt status register
VIP_INT_CLEAR	0x0818	W	0x00000000	MMU raw interrupt status register
VIP_INT_MASK	0x081c	W	0x00000000	MMU raw interrupt status register
VIP_INT_STATUS	0x0820	W	0x00000000	MMU raw interrupt status register
VIP_AUTO_GATING	0x0824	W	0x00000000	MMU auto gating

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

5.4.2 Detail Register Description

VIP_CTRL

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:12	RW	0x0	AXI_BURST_TYPE Axi master burst byte. 4'h0-4'hf : burst1~16
11:3	RO	0x0	reserved

Bit	Attr	Reset Value	Description
2:1	RW	0x0	WORK_MODE Working mode. 2'b00 : one frame stop mode 2'b01 : ping-pong mode 2'b10 : line loop mode 2'b11 : reserved
0	RW	0x0	CAP_EN Capture enable. 1'b0 : disable 1'b1 : enable

VIP_INTEN

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:10	RO	0x0	reserved
9	RW	0x0	PST_INF_FRAME_END_EN Frame end after interface FIFO interrupt enable. 1'b0 : disable 1'b1 : enable
8	RW	0x0	PRE_INF_FRAME_END_EN Frame end before interface FIFO interrupt enable. 1'b0 : disable 1'b1 : enable
7	RO	0x0	reserved
6	W1C	0x0	BUS_ERR_EN Axi master or ahb slave response error interrupt enable. 1'b0 : disable 1'b1 : enable
5	RW	0x0	DFIFO_OF_EN DMA FIFO overflow interrupt enable. 1'b0 : disable 1'b1 : enable
4	RW	0x0	IFIFO_OF_EN Interface FIFO overflow interrupt enable. 1'b0 : disable 1'b1 : enable
3	W1C	0x0	PIX_ERR_EN The pixel number of last line not equal to the set height interrupt enable. 1'b0 : disable 1'b1 : enable

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Bit	Attr	Reset Value	Description
2	W1C	0x0	LINE_ERR_EN The line number of last frame not equal to the set height interrupt enable. 1'b0 : disable 1'b1 : enable
1	W1C	0x0	LINE_END_EN Line end interrupt enable. 1'b0 : disable 1'b1 : enable
0	RW	0x0	DMA_FRAME_END_EN DMA frame end interrupt enable. 1'b0 : disable 1'b1 : enable

VIP_INTSTAT

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:10	RO	0x0	reserved
9	RW	0x0	PST_INF_FRAME_END Frame end after interface FIFO interrupt. 1'b0 : no interrupt 1'b1 : interrupt
8	RW	0x0	PRE_INF_FRAME_END Frame end before interface FIFO interrupt. 1'b0 : no interrupt 1'b1 : interrupt
7	RO	0x0	reserved
6	W1C	0x0	BUS_ERR Axi master or ahb slave response error interrupt. 1'b0 : no interrupt 1'b1 : interrupt
5	RW	0x0	DFIFO_OF DMA FIFO overflow interrupt. 1'b0 : no interrupt 1'b1 : interrupt
4	RW	0x0	IFIFO_OF Interface FIFO overflow interrupt. 1'b0 : no interrupt 1'b1 : interrupt
3	W1C	0x0	PIX_ERR The pixel number of last line not equal to the set height interrupt. 1'b0 : no interrupt 1'b1 : interrupt

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Bit	Attr	Reset Value	Description
2	W1C	0x0	LINE_ERR The line number of last frame not equal to the set height interrupt. 1'b0 : no interrupt 1'b1 : interrupt
1	W1C	0x0	LINE_END Line end interrupt. 1'b0 : no interrupt 1'b1 : interrupt
0	W1C	0x0	DMA_FRAME_END DMA frame end interrupt. 1'b0 : no interrupt 1'b1 : interrupt

VIP_FOR

Address: Operational Base + offset (0x000c)

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19	RW	0x0	UV_STORE_ORDER UV storage order. 1'b0 : UVUV 1'b1 : VUVU
18	RW	0x0	RAW_END Raw data endian. 1'b0 : little end 1'b1 : big end
17	RW	0x0	OUT_420_ORDER Output 420 order. 1'b0 : UV in the even line 1'b1 : UV in the odd line Note: The first line is even line(line 0)
16	RW	0x0	OUTPUT_420 Output 420 or 422. 1'b0 : output is 422 1'b1 : output is 420
15	RO	0x0	reserved
14:13	RW	0x0	MIPI_MODE Mipi mode: 2'b00 : 32 bit bypass mode 2'b01 : rgb mode 2'b10 : yuv mode 2'b11 : reserve

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Bit	Attr	Reset Value	Description
12:11	RW	0x0	RAW_WIDTH Raw data width. 2'b00 : 8bit raw data 2'b01 : 10bit raw data 2'b10 : 12bit raw data 2'b11 : reserve
10	RW	0x0	JPEG_MODE JPEG mode. 1'b0 : other mode 1'b1 : mode1
9	RW	0x0	FIELD_ORDER CCIR input order. 1'b0 : odd field first 1'b1 : even field first
8	RW	0x0	IN_420_ORDER 420 input order. 1'b0 : UV in the even line 1'b1 : UV in the odd line Note: The first line is even line(line 0)
7	RW	0x0	INPUT_420 Input 420 or 422. 1'b0 : 422 1'b1 : 420
6:5	RW	0x0	YUV_IN_ORDER YUV input order: 2'b00 : UYVY 2'b01 : YVYU 2'b10 : VYUY 2'b11 : YUYV
4:2	RW	0x0	INPUT_MODE Input mode: 3'b000 : YUV 3'b010 : PAL 3'b011 : NTSC 3'b100 : RAW 3'b101 : JPEG 3'b110 : MIPI Other : invalid
1	RW	0x0	HREF_POL Href input polarity: 1'b0 : high active 1'b1 : low active

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Bit	Attr	Reset Value	Description
0	RW	0x0	VSYNC_POL Vsync input polarity: 1'b0 : low active 1'b1 : high active

VIP_FRM0_ADDR_Y

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	FRM0_ADDR_Y VIP frame0 y address

VIP_FRM0_ADDR_UV

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	FRM0_ADDR_UV VIP frame0 uv address

VIP_FRM1_ADDR_Y

Address: Operational Base + offset (0x001c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	FRM1_ADDR_Y VIP frame1 y address

VIP_FRM1_ADDR_UV

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	FRM1_ADDR_UV VIP frame1 uv address

VIP_VIR_LINE_WIDTH

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:15	RO	0x0	reserved
14:0	RW	0x0000	VIR_LINE_WIDTH VIP virtual line width

VIP_SET_SIZE

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	SET_HEIGHT Set height
15:13	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
12:0	RW	0x02d0	SET_WIDTH Set width

VIP_CROP

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	START_Y Start x point
15:13	RO	0x0	reserved
12:0	RW	0x0000	START_X Start y point

VIP_SCL_CTRL

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:7	RO	0x0	reserved
6	RW	0x0	MIPI_32B_BP Mipi 32bit bypass. 1'b0 : no bypass 1'b1 : bypass
5	RW	0x0	RAW_16B_BP Raw 16bit bypass. 1'b0 : no bypass 1'b1 : bypass
4	RW	0x0	YUV_16B_BP YUV 16bit bypass. 1'b0 : no bypass 1'b1 : bypass
3:0	RO	0x0	reserved

VIP_FIFO_ENTRY

Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:18	RO	0x0	reserved
17:9	RW	0x000	UV_FIFO_ENTRY Valid UV double word in FIFO. Write 0 clear
8:0	RO	0x000	Y_FIFO_ENTRY Valid Y double word in FIFO. Write 0 clear

VIP_FRAME_STATUS

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Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	FRAME_NUM Complete frame number. write 0 to clear
15:2	RO	0x0	reserved
1	RO	0x0	F1_STS Frame 1 status. 1'b0 : frame 1 not ready 1'b1 : frame 1 ready Write 0 clear
0	RO	0x0	F0_STS Frame 0 status. 1'b0 : frame 0 not ready 1'b1 : frame 0 ready Write 0 clear

VIP_CUR_DST

Address: Operational Base + offset (0x0064)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	CUR_DST Current destination address. Maybe not the current, because the clock synchronization

VIP_LAST_LINE

Address: Operational Base + offset (0x0068)

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12:0	RO	0x0000	LAST_LINE_NUM Line number of last frame

VIP_LAST_PIX

Address: Operational Base + offset (0x006c)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0000	LAST_UV_NUM Y number of last line
15:13	RO	0x0	reserved
12:0	RO	0x0000	LAST_Y_NUM Y number of last line

VIP_DTE_ADDR

Address: Operational Base + offset (0x0800)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MMU_DTE_ADDR MMU current page Table address

VIP_STATUS

Address: Operational Base + offset (0x0804)

Bit	Attr	Reset Value	Description
31:11	RO	0x0	reserved
10:6	RO	0x00	PAGE_FAULT_BUS_ID Page fault bus id. Index of master reponsible for last page fault
5	RO	0x0	PAGE_FAULT_IS_WRITE Page fault access. The direction of access for last page fault: 1'b0 = Read 1'b1 = Write
4	RO	0x0	REPLAY_BUFFER_EMPTY Replay buffer empty status. 1'b1:The MMU replay buffer is empty
3	RO	0x0	MMU_IDLE MMU idle status. The MMU is idle when accesses are being translated and there are no unfinished translated accesses. 1'b1: MMU is idle
2	RO	0x0	STAIL_ACTIVE Stall active status. MMU stall mode currently enabled. The mode is enabled by command. 1'b1: MMU is in stall active status
1	RO	0x0	PAGE_FAULT_ACTIVE Page fault active status.MMU page fault mode currently enabled . The mode is enabled by command. 1'b1: page fault is active
0	RW	0x0	PAGING_ENABLED Paging enabled status. 1'b0: paging is disabled 1'b1: Paging is enabled

VIP_COMMAND

Address: Operational Base + offset (0x0808)

Bit	Attr	Reset Value	Description
31:3	RO	0x0	reserved

Bit	Attr	Reset Value	Description
2:0	RW	0x0	MMU_CMD MMU cmd.This can be: 3'h0: MMU_ENABLE_PAGING 3'h1: MMU_DISABLE_PAGING 3'h2: MMU_ENABLE_STALL 3'h3: MMU_DISABLE_STALL 3'h4: MMU_ZAP_CACHE 3'h5: MMU_PAGE_FAULT_DONE 3'h6: MMU_FORCE_RESET

VIP_PAGE_FAULT_ADDR

Address: Operational Base + offset (0x080c)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	PAGE_FAULT_ADDR Page fault addr. Address of last page fault

VIP_ZAP_ONE_LINE

Address: Operational Base + offset (0x0810)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	MMU_ZAP_ONE_LINE Zap one line. Address to be invalidated from the page table cache

VIP_INT_RAWSTAT

Address: Operational Base + offset (0x0814)

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x0	READ_BUS_ERROR Read bus error status
0	RW	0x0	PAGE_FAULT Page fault status

VIP_INT_CLEAR

Address: Operational Base + offset (0x0818)

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	WO	0x0	READ_BUS_ERROR Read bus error. Write 1'b1 to clear read bus error
0	RW	0x0	PAGE_FAULT Page fault clear. Write 1'b1 to page fault clear

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VIP_INT_MASK

Address: Operational Base + offset (0x081c)

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x0	READ_BUS_ERROR Read bus error.Enable the read bus interrupt souce when this bit is set to 1'b1
0	RW	0x0	PAGE_FAULT Page faule mask.Enable the page fault interrupt souce when this bit is set to 1'b1

VIP_INT_STATUS

Address: Operational Base + offset (0x0820)

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RO	0x0	READ_BUS_ERROR Read bus error status. 1'b1:read bus error status
0	RO	0x0	PAGE_FAULT Page fault status. 1'b1:page fault

VIP_AUTO_GATING

Address: Operational Base + offset (0x0824)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	MMU_AUTO_CLKGATING When it is 1'b1, the mmu will auto gating it self

5.5 Interface Description

Module Pin	Dir	Pad Name	IOMUX Setting
vip_clkout	O	IO_CIFclkoutm0_CLKout_ethernet_GPIO2B3vccio3	GRF_GPIO2B_IOMUX_L[14:12]=3'b1
	O	IO_LCDCd20_PDMsdi1_CIFclkoutm1_GPIO3D0vccio4	GRF_GPIO3D_IOMUX_L[2:0]=3'b11
vip_clkin	I	IO_CIFclkinm0_RMIIclk_GPIO2B2vccio3	GRF_GPIO2B_IOMUX_L[10:8]=3'b1
	I	IO_LCDCd23_PDMsdi0m0_CIFclkinm1_ISPfl_trig _GPIO3D3vccio4	GRF_GPIO3D_IOMUX_L[14:12]=3'b11
vip_href	I	IO_CIFhrefm0_RMIImdc_GPIO2B1vccio3	GRF_GPIO2B_IOMUX_L[6:4]=3'b1
	I	IO_LCDCd22_PDMsdi3_CIFhrefm1_ISPflash_trig _GPIO3D2vccio3	GRF_GPIO3D_IOMUX_L[10:8]=3'b11
vip_vsync	I	IO_CIFvsyncm0_GPIO2B0 vccio3	GRF_GPIO2B_IOMUX_L[2:0]=3'b1
	I	IO_LCDCd21_PDMsdi2_CIFvsyncm1_ISPprelight_trig _GPIO3D1vccio4	GRF_GPIO3D_IOMUX_L[6:4]=3'b11
vip_data0	I	IO_CIFd0m0_ART2txm1_GPIO2B4vccio3	GRF_GPIO2B_IOMUX_H[2:0]=3'b1
	I	IO_LCDChsyncm0_I2S22ch_mclk_CIFd0m1_UART5rx_GPIO3A1vccio4	GRF_GPIO3A_IOMUX_L[6:4]=3'b11
vip_data1	I	IO_CIFd1m0_UARTrxm1_GPIO2B6vccio3	GRF_GPIO2B_IOMUX_H[10:8]=3'b1
	I	IO_LCDCvsyncm0_I2S22ch_sclk_CIFd1m1_UART5tx_GPIO3A2vccio4	GRF_GPIO3A_IOMUX_L[10:8]=3'b11

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Module Pin	Dir	Pad Name	IOMUX Setting
vip_data2	I	IO_CIFd2m0_RMIItxen_GPIO2A0vccio3	GRF_GPIO2A_IOMUX_L[2:0]=3'b1
	I	IO_LCDCdenm0_I2S22ch_lrck_CIFd2m1_UART5cts_GPIO3A3vccio4	GRF_GPIO3A_IOMUX_L[14:12]=3'b11
vip_data3	I	IO_CIFd3m0_RMIItxd1_GPIO2A1vccio3	GRF_GPIO2A_IOMUX_L[6:4]=3'b1
	I	IO_LCDCd1m0_I2S22ch_sdi_CIFd3m1_UART5rts_GPIO3A5vccio4	GRF_GPIO3A_IOMUX_H[6:4]=3'b11
vip_data4	I	IO_CIFd4m0_RMIItxd0_GPIO2A2vccio3	GRF_GPIO2A_IOMUX_L[10:8]=3'b1
	I	IO_LCDCd3m0_I2S22ch_sdo_CIFd4m1_GPIO3A7vccio4	GRF_GPIO3A_IOMUX_H[14:12]=3'b11
vip_data5	I	IO_CIFd5m0_RMIIrxd0_GPIO2A3vccio3	GRF_GPIO2A_IOMUX_L[14:12]=3'b1
	I	IO_LCDCd4m0_I2S08ch_sdi3_CIFd5m1_GPIO3B0vccio4	GRF_GPIO3B_IOMUX_L[2:0]=3'b11
vip_data6	I	IO_CIFd6m0_RMIIrxd1_GPIO2A4vccio3	GRF_GPIO2A_IOMUX_H[2:0]=3'b1
	I	IO_LCDCd5m0_I2S08ch_sdi2_CIFd6m1_SPI1csn_GPIO3B1vccio4	GRF_GPIO3B_IOMUX_L[6:4]=3'b11
vip_data7	I	IO_CIFd7m0_RMIIrxer_GPIO2A5vccio3	GRF_GPIO2A_IOMUX_H[6:4]=3'b1
	I	IO_LCDCd8m0_I2S08ch_sclkrx_CIFd7m1_SPI1mosi_GPIO3B4vccio4	GRF_GPIO3B_IOMUX_H[2:0]=3'b11
vip_data8	I	IO_CIFd8m0_RMIIrxdv_GPIO2A6vccio3	GRF_GPIO2A_IOMUX_H[10:8]=3'b1
	I	IO_LCDCd10m0_I2S08ch_sdo3_CIFd8m1_SPI1miso_GPIO3B6vccio4	GRF_GPIO3B_IOMUX_H[10:8]=3'b11
vip_data9	I	IO_CIFd9m0_RMIImdio_GPIO2A7vccio3	GRF_GPIO2A_IOMUX_H[14:12]=3'b1
	I	IO_LCDCd11m0_I2S08ch_sdo2_CIFd9m1_SPI1clk_GPIO3B7vccio4	GRF_GPIO3B_IOMUX_H[14:12]=3'b11
vip_data10	I	IO_CIFd10m0_I2C2scl_GPIO2B7vccio3	GRF_GPIO2B_IOMUX_H[14:12]=3'b1
	I	IO_LCDCd18_PDMclk0m0_CIFd10m1_GPIO3C6vccio4	GRF_GPIO3C_IOMUX_H[10:8]=3'b11
vip_data11	I	IO_CIFd11m0_I2C2sda_GPIO2C0vccio3	GRF_GPIO2C_IOMU_L[2:0]=3'b1
	I	IO_LCDCd19_PDMclk1_CIFd11m1_GPIO3C7vccio4	GRF_GPIO3C_IOMUX_H[14:12]=3'b11

5.6 Application Notes

The biggest configuration requirement of all operations is the CAP_EN bit must be set after all the mode selection is ready. The configuration order of the input/output data format, YUV order, the address, frame size/width, AXI burst length and other options do not need to care.

There are many debug registers to make it easy to read the internal operation information of VIP. The valid pixel number of scale result in FIFO can be known by read VIP_SCL_VALID_NUM. The line number of last frame and the pixel number of last line can be also known by read the VIP_LAST_LINE and VIP_LAST_PIX.

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Chapter 6 Video Output Processor (VOP_BIG)

6.1 Overview

Video Output Processor is a video process engine and a display interface from memory frame buffer to display device(LCD panel, MIPI, LVDS, RGB, ect). VOP is connected to an AHB bus through an AHB slave and AXI bus through an AXI master. The register setting is configured through the AHB slave interface and the display frame data is read through the AXI master interface.

6.1.1 Features

The features listed below which may or may not be present in actual product, may be subject to the third party licensing requirements. Please contact Rockchip for actual product feature configurations and licensing requirements.

VOP_BIG supports the following features:

- Display interface
  - Parallel RGB LCD Interface: 24-bit(RGB888),18-bit(RGB666), 16-bit(RGB565)
  - Display interface
    - Parallel Display interface
    - MIPI_DSI_TX
    - LVDS
  - Max output resolution
    - 1280x800 with CABC enable
    - 1920x1080 with CABC disable
- Display process
  - Background layer
    - programmable 24-bit color
  - Win0 layer
    - RGB888, ARGB888, RGB565, YCbCr422, YCbCr420, YCbCr444
    - 1/8 to 8 scaling-down and scaling-up engine
    - Support virtual display
    - 256 level alpha blending (pre-multiplied alpha support)
    - Transparency color key
    - YCbCr2RGB(rec601-mpeg/ rec601-jpeg/rec709)
    - RGB2YCbCr(BT601/BT709)
  - Win1 layer
    - RGB888, ARGB888, RGB565
    - Support virtual display
    - 256 level alpha blending (pre-multiplied alpha support)
    - Transparency color key
    - RGB2YCbCr(BT601/BT709)
    - Support AFBCD
  - Win2 layer
    - RGB888, ARGB888, RGB565
    - Support virtual display
    - 256 level alpha blending (pre-multiplied alpha support)
    - Transparency color key
    - RGB2YCbCr(BT601/BT709)
    - Support multi-region
      - HWC layer
        - Support 8BPP only
        - Size : 32x32 or 64x64
    - 256 level alpha blending (pre-multiplied alpha support)
    - RGB2YCbCr(BT601/BT709)
- Others
  - Win0 layer , Win1 layer and Win2 layer overlay exchangeable
  - Support RGB or YUV domain overlay

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- BCSH(Brightness, Contrast, Saturation, Hue adjustment)
- BCSH:YCbCr2RGB(rec601-mpeg/ rec601-jpeg/rec709)
- BCSH:RGB2YCbCr(BT601/BT709)
- Support Gamma adjust for PAD
- Support CABC
- Support dither down allegro RGB888to666 RGB888to565 & dither down frc (configurable) RGB888to666
- Blank and black display
- Standby mode
- Support QoS request for higher bus priority for win1/HWC
- Support NOC hurry for higher bus priority for win0
- Support all layers reg_done separately

6.2 Block Diagram

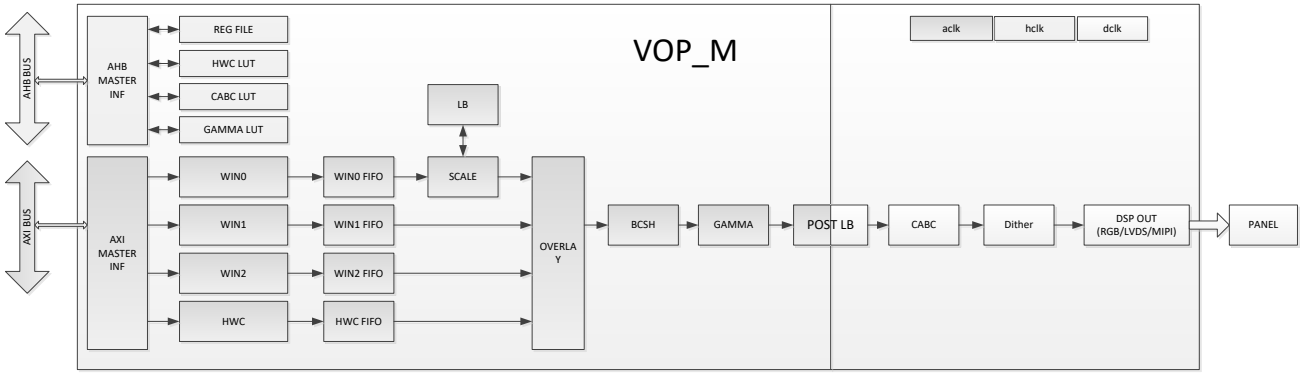


Fig. 6-1 VOP Block Diagram

6.3 Function Description

6.3.1 Data Format

VOP master read the frame data from the frame buffer in the system memory. There are total 6 formats supported in three layers.

- Win0: RGB888, ARGB888, RGB565, YCbCr422_SP, YCbCr420_SP, YCbCr444_SP
- Win1: RGB888, ARGB888, RGB565;
  AFBCD_ARGB8888,AFBCD_RGB888,AFBCD_RGB565
- Win2: RGB888, ARGB888, RGB565
- HWC: 8BPP

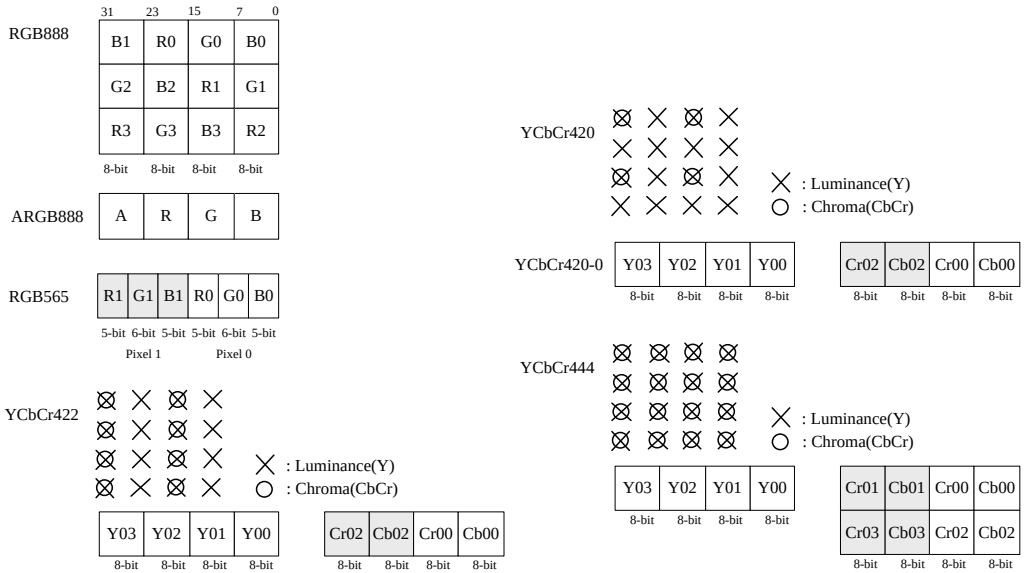


Fig. 6-2 VOP Frame Buffer Data Format

	D[31:24]	D[23:16]	D[15:8]	D[7:0]
000H	P1	P2	P3	P4
004H	P5	P6	P7	P8
008H	P9	P10	P11	P12
...				

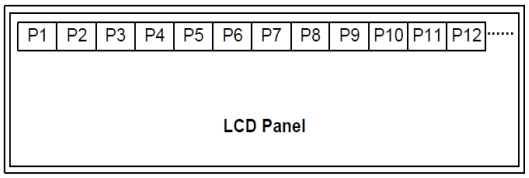


Fig. 6-3 VOP HWC Palette (8bpp)

Data SWAP function

There are several swap options for different frame data formats..
All the data swap types are in the following table.

Table 6-1 VOP Data Swap of Win0 and Win1

Data-swap	RB swap	Alpha swap	Y-M8 swap	CbCr swap
Win0	yes	yes	yes	yes
Win1	yes	yes	No	No

6.3.2 Data path

There are two data input path for VOP to get display layers' pixel data. One is internal DMA; the other is direction path interface.

1.Internal DMA

Internal DMA can fetch the pixel data through AXI bus from system memory (DDR) for all the display layers. Data fetching is driven by display output requirement.

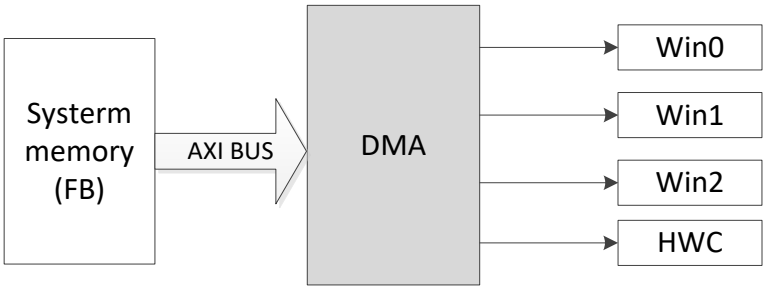


Fig. 6-4 VOP Internal DMA

6.3.3 Virtual display

Virtual display is supported in Win0 , Win1 , Win2. The active image is part of the virtual (original) image in frame buffer memory. The virtual width is indicated by setting WIN0/WIN1_VIR_STRIDE for different data format.
The virtual stride should be multiples of word (32-bit). That means dummy bytes in the end of virtual line if the real pixels are not 32-bit aligned.

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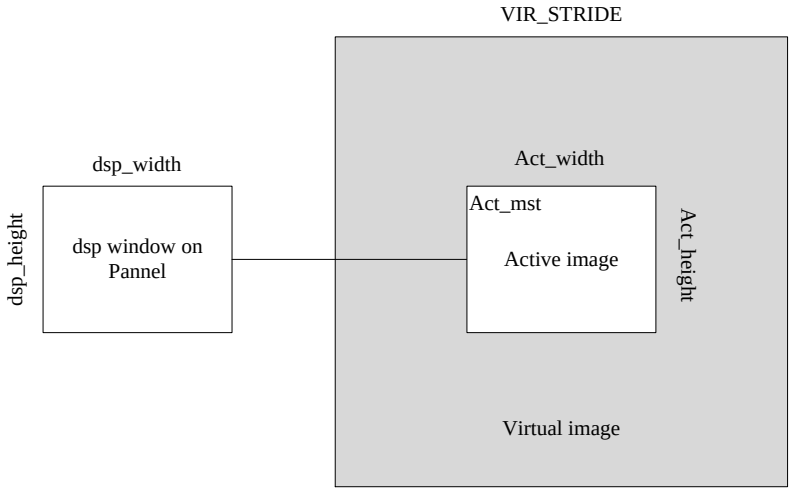


Fig. 6-5 VOP Virtual Display Mode

6.3.4 Scaling

The scaling operation is the image resizing process of data transfer from the frame buffer memory to LCD panel or TV set.

Horizontal and vertical scaling factor should be set according the window scaling ratio.

1. Scaling factor

Because the Chroma data may have different sampling rate with Luma data in the memory format of YCbCr422/YCbCr420. The scaling factor of Win0 has two couples of factor registers:

VOP_WIN0_SCL_FACTOR_Y/VOP_WIN0_SCL_FACTOR_CBR

Software calculates the scaling factor value using the following equations:

$$y_rgb_vertical_factor = (\frac{VOP_WIN0_ACT_INFO[31:16]}{VOP_WIN0_DSP_INFO[31:16]}) \times 2^{12}$$

$$y_rgb_horizontal_factor = (\frac{VOP_WIN0_ACT_INFO[15:0]}{VOP_WIN0_DSP_INFO[15:0]}) \times 2^{12}$$

$$yuv422_yuv444_Cbr_vertical_factor = (\frac{VOP_WIN0_ACT_INFO[31:16]}{VOP_WIN0_DSP_INFO[31:16]}) \times 2^{12}$$

$$yuv420_Cbr_vertical_factor = (\frac{VOP_WIN0_ACT_INFO[31:16]/2}{VOP_WIN0_DSP_INFO[31:16]}) \times 2^{12}$$

$$yuv444_Cbr_horizontal_factor = (\frac{VOP_WIN0_ACT_INFO[15:0]}{VOP_WIN0_DSP_INFO[15:0]}) \times 2^{12}$$

$$yuv422_yuv420_Cbr_horizontal_factor = (\frac{VOP_WIN0_ACT_INFO[15:0]/2}{VOP_WIN0_DSP_INFO[15:0]}) \times 2^{12}$$

2. Scaling start point offset

The x and y start point of the generated pixels can be adjusted, the offset value is in the range of 0 to 0.99.

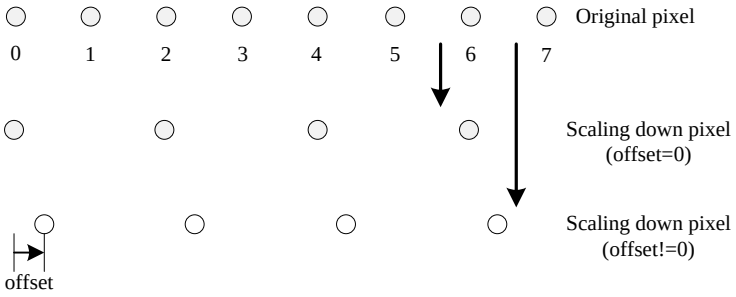


Fig. 6-6 VOP Scaling Down Offset

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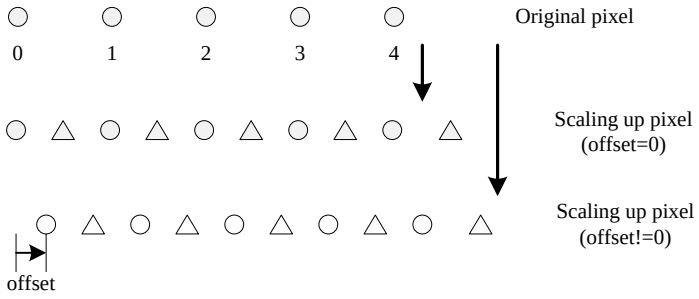


Fig. 6-7 VOP Scaling Up Offset

Table 6-2 VOP Scaling Start Point Offset Registers

scaling down/up start point offset	Offset variable	Register
Win0 YRGB vertical scaling offset	Win0_YRGB_vscl_offset	Win0_SCL_OFFSET [32:24]
Win0 YRGB horizontal scaling offset	Win0_YRGB_hscl_offset	Win0_SCL_OFFSET [23:16]
Win0 Cbr vertical scaling offset	Win0_CBR_vscl_offset	Win0_SCL_OFFSET [15:8]
Win0 Cbr horizontal scaling offset	Win0_CBR_hscl_offset	Win0_SCL_OFFSET [7:0]

6.3.5 Overlay

1. Overlay display

There are totally 5 layers for overlay display: Background, Win0, Win1,Win2 and Hwc. The background is a programmable solid color layer, which is always the bottom of the display screen.

Hwc is a 32x32 or 64x64 8BPP color palette layer, which is the top layer of the display screen. dsp_hwc_data[23:0] come from the HWC_LUT, which input is a 8BPP data format and output is 24 bits dsp_hwc_data.

Win0 , Win1 and Win2 are exchangeable by configure sw_dsp_layer1_sel , sw_dsp_layer2_sel and sw_dsp_layer3_sel .

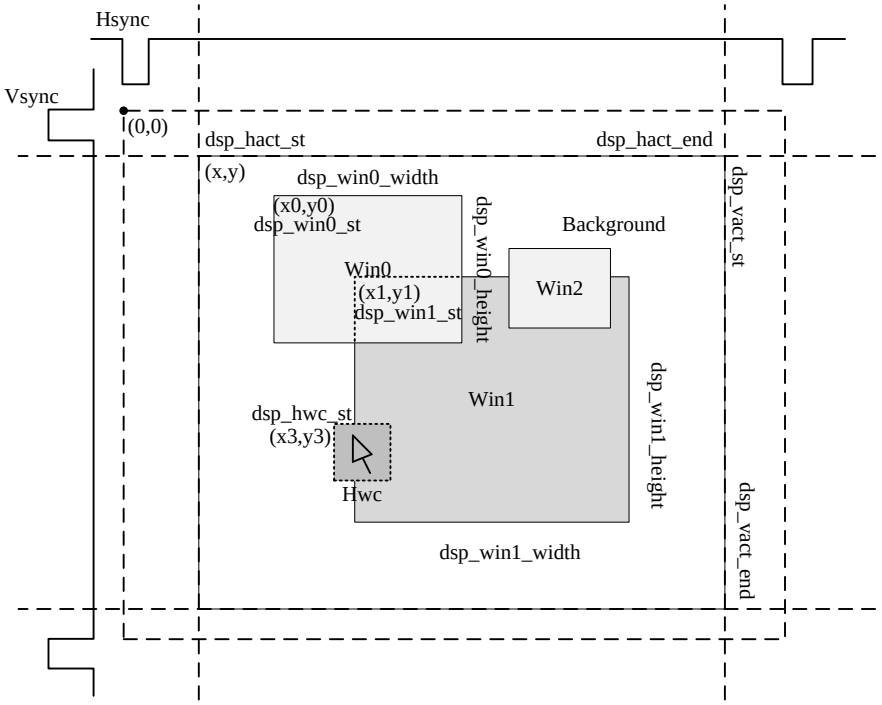


Fig. 6-8 VOP Overlay Display

2. Transparency color key

There are specific registers(VOP_WIN0_COLOR_KEY,VOP_WIN1_COLOR_KEY) for Win0 ,Win1 and Win2 layer to configure the colorkey value.The two transparency color keycan be active at the same time.

The pixel color value is compared to the transparency color key before final display. The transparency color key value defines the pixel data considered asthe transparent pixel. The pixel values with the source color key value are pixels not visibleon the screen, and the under layer pixel values or solid background color are visible.

Transparency color key is done after the scaling module . So transparency color key can only be used in non-scaling mode.

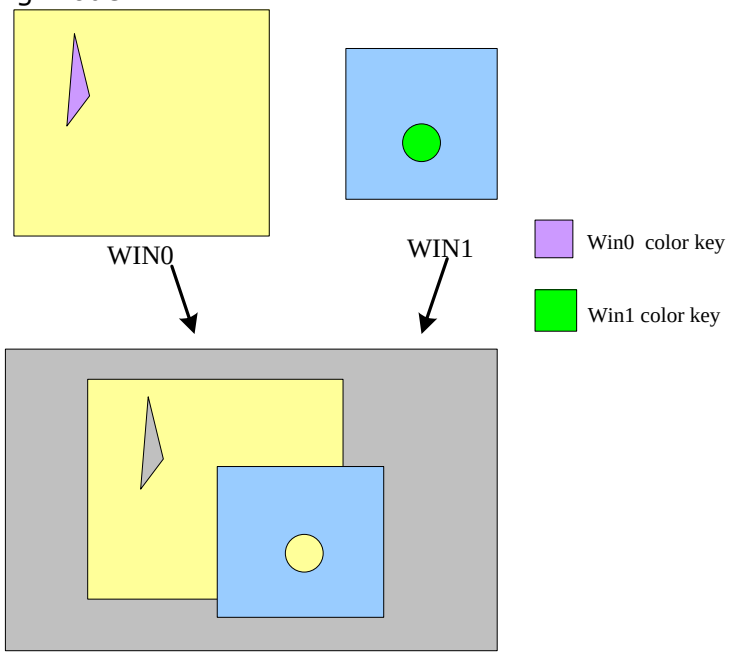


Fig. 6-9 VOP Transparency Color Key

3. Alpha Blending

Two blending modes are supported. One is per-pixel (ARGB) mode; the other is user-specified mode. In ARGB mode, the alpha value is in the ARGB data (Win0 and Win1 normal mode only). In user-specified mode, the alpha value comes from the register (WINX_ALPHA_CTRL[11: 4]).

Pre-multiplied alpha are supported for per-pixel alpha in Win0 and Win 1, for Pre-multiplied alpha, the SRC data has already been multiplied with alpha value.

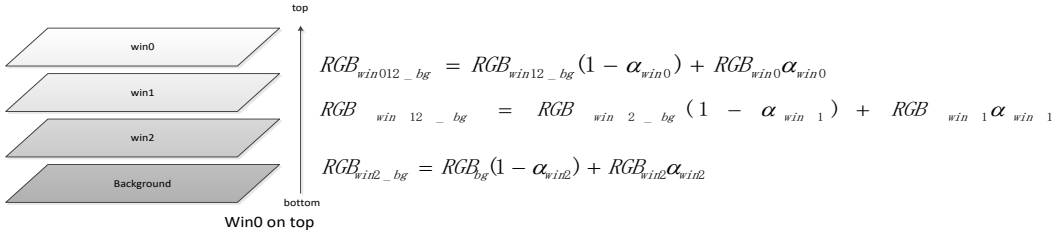


Fig. 6-10 VOP Alpha blending

4. RGB OVERLAY and YCbCr OVERLAY

VOP has a signal named sw_overlay_mode at DSP_CTRL2[4] to decide overlay in RGB or YUV color space.

RGB OVERLAY

All layers overlay in RGB color space. If win0 is YUV420/422/444, it can be converted to RGB888 by YUV2RGB use MPEG,JPEG and HDTV formula.

YCbCr OVERLAY

All layers overlay in YCbCr color space .When win0/1 input picture format is RGB, it can be converted to YUV444 using BT601 or BT709.

Since HWC supports BPP8, we can directly use AYUV444 LUT instead of ARGB888 LUT.

6.3.6 BCSH

The BCSH block is used for brightness, contrast, saturation and hue adjustment to YCbCr

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format image.
The following diagram shows the BCSH adjustment processing. All the factors should be set in the VOP registers.

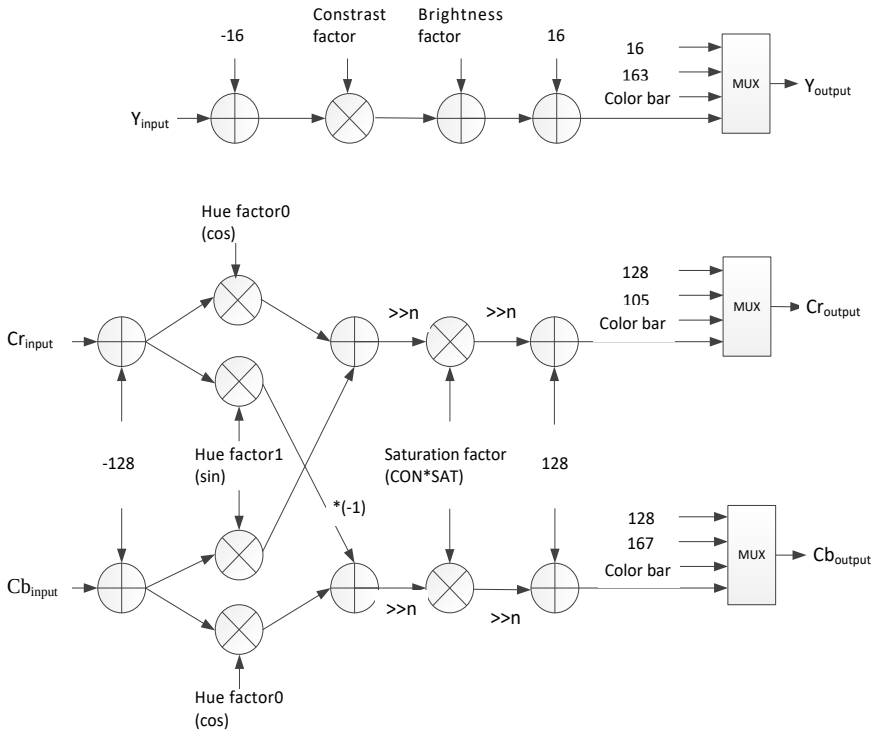


Fig. 6-51 VOP BCSH Diagram

6.3.7 Gamma Correction

Gamma correction is necessary because most monitors don't have a linear relationship between the voltage and the brightness, which results in your scene looking like it has too much contrast and the light falling off from the source outward, happens too quickly. The result can also be problematic if you are going into a composition program.
You can correct this by "Gamma Correction", which allows you to display the images and textures on your computer in an accurate manner.
Your screen is not linear, in that it displays the brightness unevenly. As a result, the image looks to be more high contrast than it should, you end up adding more lights or turning up the intensity, or you don't use the lighting in a realistic way that matches well with live action scenes. It also creates problems for you if you use compositing software.
It consumes 256x8bit LUT for each channel. You can write gamma correction LUT through register" DSP_LUT_ADDR" one by one after set dsp_lut_en = 0.

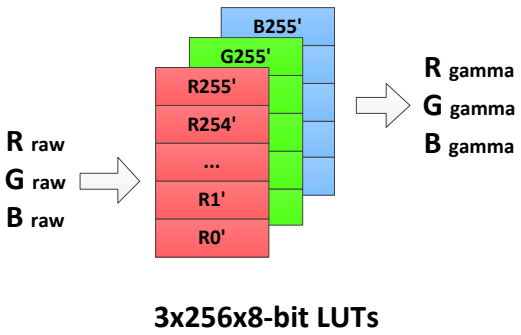


Fig. 6-12 VOP Gamma LUTs

6.3.8 Replication and dither down

1 Replication (dither up)

If the interface data bus is wider than the pixel format size, by programming the pixel

components replication active/inactive, the MSB is replicated to the LSB of the interface data bus or the LSB is filled with 0s.

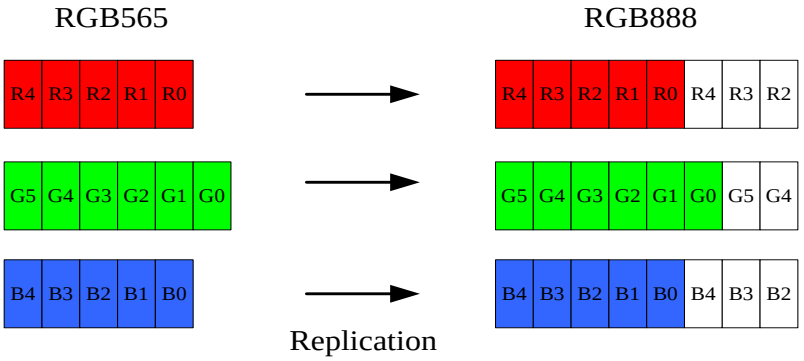


Fig. 6-13 VOP Replication

Dithering is used to improve the quality of display the pixel data in a lower color depth on the LCD panel. The Dithering algorithm is based on the (x,y) pixel position, the value of removed bits and frame counter.

2 Dither down

Here we support three kinds of dithering arithmetic. RGB888 to RGB666 has two ways, one is allegro, the other is FRC. RGB888 to RGB565 has only one arithmetic, which is allegro. When Dithering is not enabled, the MSBs of the pixel color components are output on the interface data bus if the interface data bus is smaller than the pixel format size.

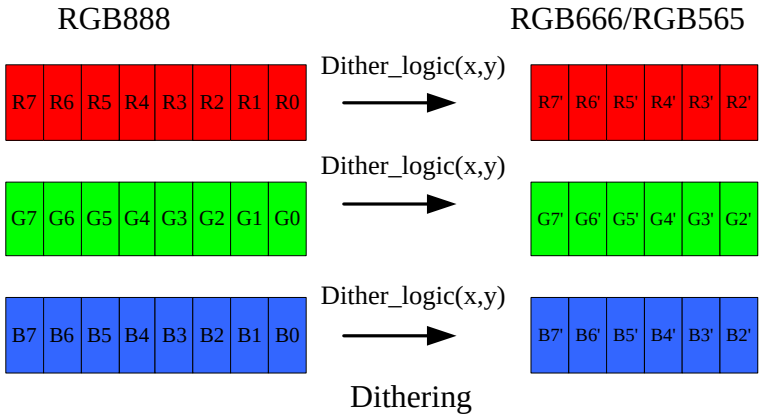


Fig. 6-14 vop dithering

The following figure is the recommended pattern picture in vop, you can config different value of reg 0x170~0x184，to change the pattern picture.(default value is recommended values below)

6.3.9 CABC

CABC(Content Adaptive Backlight Control) is used to increase the contrast of such LCD-screens the backlight can be (globally) dimmed when the image to be displayed is dark (i.e. not comprising high intensity image data) while the image data is numerically corrected and adapted to the reduced backlight intensity.

There are 3x7 Gaussian filter tables in reg 0x1d0~0x1e4.

default value as follow:

0x1c8 : 0x15110903
0x1cc : 0x00030911
0x1d0 : 0x1a150b04
0x1d4 : 0x00040b15
0x1d8 : 0x15110903
0x1dc : 0x00030911

program guide：

step1: Config the panel total pixel number to register CABC_CTRL0 [26:4],and config the calc pixel num to register CABC_CTRL1 [26:4].
(typical: calc_pixel_num / total_pixel_num = 95% ~98%).
step2: Config pwm_config_mode ,cabc_handle_en to register CABC_CTRL0 .
step3: Config CABC_CTRL2 and CABC_CTRL3 register.

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step4: write pwm gamma lut to CABC_GAMMA_LUT_ADDR (vop_base_addr + 0x1800),typical gamma value = 2.2(typical)
step5: Config cabc_lut_en and cabc_en to register CABC_CTRL1 [0] and CABC_CTRL0 [0].
step6: Config done.

6.3.10 AFBCD

This compression format is designed to be used for textures and frame buffers. It has been optimized to decrease external bandwidth as well as being random access and decodable at line speed for the texture cache.
The AFBCD has the following feature/limitations:

- Lossless compression
- Only WIN1 support AFBCD
- Support AFBC_ARGB8888，AFBC_RGB888,AFBC_RGB565
- Only support half mode
- Don't support split mode
- Support x_offset and y_offset in pixel
- Support header virtual stride
- AFBCD_PIC_PTR must be 128-bit alignment

6.3.11 Multi-region display

The multi-region display of win2 has the following limitations:

- There is only one region in the same line
- There is not overlap region between different regions
- When display one region , region0 must be enable .When display two regions , region0 and region1 must be enable , and so on

Multi-region display application is shown as follows :

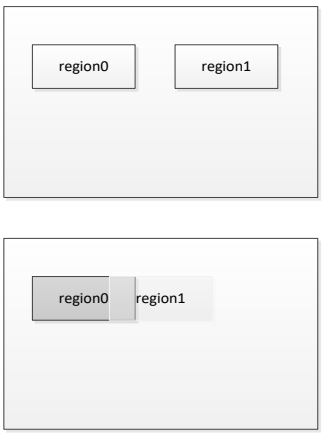


Fig. 6-15 Limitations of multi-region display of win2

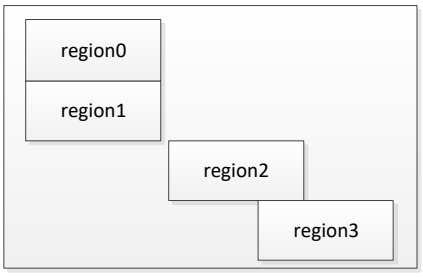


Fig. 6-16 Correct application of multi-region display of win2

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6.4 Register Description

6.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

6.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
VOP_BIG_REG_CFG_DONE	0x0000	W	0x00000000	Register config done flag
VOP_BIG_VERSION	0x0004	W	0x00000000	Version for vop
VOP_BIG_DSP_BG	0x0008	W	0x00000000	Display control register
VOP_BIG_MCU	0x000c	W	0x00000000	MCU control register
VOP_BIG_SYS_CTRL0	0x0010	W	0x00000000	System control register
VOP_BIG_SYS_CTRL1	0x0014	W	0x00000000	System control register
VOP_BIG_SYS_CTRL2	0x0018	W	0x00006000	System control register
VOP_BIG_POST_LB_CTRL	0x001c	W	0x00000000	Post lb control register
VOP_BIG_DSP_CTRL0	0x0020	W	0x00000101	Display register
VOP_BIG_DSP_CTRL1	0x0024	W	0x00000000	Display register
VOP_BIG_DSP_CTRL2	0x0028	W	0x00004000	Display register
VOP_BIG_VOP_STATUS	0x002c	W	0x00000000	Some vop module status
VOP_BIG_LINE_FLAG	0x0030	W	0x00000000	Line flag config register
VOP_BIG_INTR_EN	0x0034	W	0x00000000	Interrupt enable register
VOP_BIG_INTR_CLEAR	0x0038	W	0x00000000	Interrupt clear register
VOP_BIG_INTR_STATUS	0x003c	W	0x00000000	Interrupt raw status and interrupt status
VOP_BIG_WIN0_CTRL0	0x0050	W	0x00000000	Win0 ctrl register
VOP_BIG_WIN0_CTRL1	0x0054	W	0x00021220	Win0 ctrl register
VOP_BIG_WIN0_COLOR_KEY	0x0058	W	0x00000000	Win0 color key register
VOP_BIG_WIN0_VIR	0x005c	W	0x01400140	Win0 virtual stride
VOP_BIG_WIN0_YRGB_MST0	0x0060	W	0x00000000	Win0 YRGB memory start address 0
VOP_BIG_WIN0_CBR_MST0	0x0064	W	0x00000000	Win0 Cbr memory start address 0
VOP_BIG_WIN0_ACT_INFO	0x0068	W	0x00ef013f	Win0 active window width/height
VOP_BIG_WIN0_DSP_INFO	0x006c	W	0x00ef013f	Win0 display width/height on panel
VOP_BIG_WIN0_DSP_ST	0x0070	W	0x0000000a	Win0 display start point on panel
VOP_BIG_WIN0_SCL_FACTOR_YRGB	0x0074	W	0x10001000	Win0 YRGB scaling factor
VOP_BIG_WIN0_SCL_FACTOR_CBR	0x0078	W	0x10001000	Win0 CBR scaling factor

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Name	Offset	Size	Reset Value	Description
VOP_BIG_WIN0_SCL_OFFSET	0x007c	W	0x00000000	Win0 scaling start point offset
VOP_BIG_WIN0_ALPHA_CTRL	0x0080	W	0x00000000	Blending control register
VOP_BIG_WIN1_CTRL0	0x0090	W	0x00000000	Win1 ctrl register
VOP_BIG_WIN1_CTRL1	0x0094	W	0x00000500	Win1 ctrl register
VOP_BIG_WIN1_VIR	0x0098	W	0x00000000	Win1 virtual stride
VOP_BIG_WIN1_MST	0x00a0	W	0x00000000	Win1 memory start address
VOP_BIG_WIN1_DSP_INFO	0x00a4	W	0x00ef013f	Win1 display width/height on panel
VOP_BIG_WIN1_DSP_ST	0x00a8	W	0x0000000a	Win1 display start point on panel
VOP_BIG_WIN1_COLOR_KEY	0x00ac	W	0x00000000	Win1 color key register
VOP_BIG_WIN1_ALPHA_CTRL	0x00bc	W	0x00000000	Blending control register
VOP_BIG_HWC_CTRL0	0x00e0	W	0x00000000	Hwc ctrl register
VOP_BIG_HWC_MST	0x00e8	W	0x00000000	Hwc memory start address
VOP_BIG_HWC_DSP_ST	0x00ec	W	0x00000000	Hwc display start point on panel
VOP_BIG_HWC_ALPHA_CTRL	0x00f0	W	0x00000000	Blending control register
VOP_BIG_DSP_HTOTAL_HS_END	0x0100	W	0x014a000a	Panel scanning horizontal width and hsync pulse end point
VOP_BIG_DSP_HACT_ST_END	0x0104	W	0x000a0000	Panel active horizontal scanning start point and end point
VOP_BIG_DSP_VTOTAL_VS_END	0x0108	W	0x00fa000a	Panel scanning vertical height and vsync pulse end point
VOP_BIG_DSP_VACT_ST_END	0x010c	W	0x000a00fa	Panel active vertical scanning start point and end point
VOP_BIG_DSP_VS_ST_END_F1	0x0110	W	0x00000000	Vertical scanning start point and vsync pulse end point of even file
VOP_BIG_DSP_VACT_ST_END_F1	0x0114	W	0x00000000	Vertical scanning active start point and end point of even filed in interlac
VOP_BIG_BCSH_CTRL	0x0160	W	0x00000000	Brightness/Contrast enhancement/Saturation/Hue contrl
VOP_BIG_BCSH_COL_BAR	0x0164	W	0x00000000	vedio mode equals 2,then output color bar yuv 24bits value
VOP_BIG_BCSH_BCS	0x0168	W	0x00000000	Brightness/Contrast enhancement/Saturation
VOP_BIG_BCSH_H	0x016c	W	0x00000000	Hue
VOP_BIG_FRC_LOWER01_0	0x0170	W	0x12844821	Frc algorithm configuration register

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Name	Offset	Size	Reset Value	Description
VOP_BIG_FRC_LOWER01_1	0x0174	W	0x21488412	Frc algorithm configuration register
VOP_BIG_FRC_LOWER10_0	0x0178	W	0xa55a9696	Frc algorithm configuration register
VOP_BIG_FRC_LOWER10_1	0x017c	W	0x5aa56969	Frc algorithm configuration register
VOP_BIG_FRC_LOWER11_0	0x0180	W	0xdeb77bed	Frc algorithm configuration register
VOP_BIG_FRC_LOWER11_1	0x0184	W	0xed7bb7de	Frc algorithm configuration register
VOP_BIG_MCU_RW_BYPASS_PORT	0x018c	W	0x00000000	MCU panel write data
VOP_BIG_DBG_REG_SCAN_LINE	0x0190	W	0x00000000	Current line number of dsp timing
VOP_BIG_WIN2_CTRL0	0x0190	W	0x00000000	win2 ctrl register
VOP_BIG_WIN2_CTRL1	0x0194	W	0x003a0000	win2 ctrl register
VOP_BIG_WIN2_VIR0_1	0x0198	W	0x01400140	Win2 virtual stride0 and virtaul stride1
VOP_BIG_WIN2_VIR2_3	0x019c	W	0x01400140	Win2 virtual stride2 and virtaul stride3
VOP_BIG_WIN2_MST0	0x01a0	W	0x00000000	Win2 memory start address0
VOP_BIG_WIN2_DSP_INFO0	0x01a4	W	0x00ef013f	Win2 display width0/height0 on panel
VOP_BIG_WIN2_DSP_ST0	0x01a8	W	0x000a000a	Win2 display start point0 on panel
VOP_BIG_WIN2_COLOR_KEY	0x01ac	W	0x00000000	Win2 color key register
VOP_BIG_WIN2_MST1	0x01b0	W	0x00000000	Win2 memory start address1
VOP_BIG_WIN2_DSP_INFO1	0x01b4	W	0x00ef013f	Win2 display width1/height1 on panel
VOP_BIG_WIN2_DSP_ST1	0x01b8	W	0x000a000a	Win2 display start point1 on panel
VOP_BIG_WIN2_ALPHA_CTRL	0x01bc	W	0x00000000	Win2 alpha source control register
VOP_BIG_WIN2_MST2	0x01c0	W	0x00000000	Win2 memory start address2
VOP_BIG_WIN2_DSP_INFO2	0x01c4	W	0x00ef013f	Win2 display width2/height2 on panel
VOP_BIG_WIN2_DSP_ST2	0x01c8	W	0x000a000a	Win2 display start point2 on panel
VOP_BIG_WIN2_MST3	0x01d0	W	0x00000000	Win2 memory start address3
VOP_BIG_WIN2_DSP_INFO3	0x01d4	W	0x00ef013f	Win2 display width3/height3 on panel
VOP_BIG_WIN2_DSP_ST3	0x01d8	W	0x000a000a	Win2 display start point3 on panel
VOP_BIG_BLANKING_VALUE	0x01f4	W	0x00000000	The value of vsync blanking

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Name	Offset	Size	Reset Value	Description
VOP_BIG_FLAG_REG_FRM_VALID	0x01f8	W	0x00000000	Flag reg value after frame valid
VOP_BIG_FLAG_REG	0x01fc	W	0x00000000	Flag reg value before frame valid
VOP_BIG_CABC_CTRL0	0x0200	W	0x00000000	Content Adaptive Backlight Control register0
VOP_BIG_CABC_CTRL1	0x0204	W	0x00000000	Content Adaptive Backlight Control register1
VOP_BIG_CABC_CTRL2	0x0208	W	0x00000000	Content Adaptive Backlight Control register2
VOP_BIG_CABC_CTRL3	0x020c	W	0x00000000	Content Adaptive Backlight Control register3
VOP_BIG_CABC_GAUSS_LINE0_0	0x0210	W	0x00000000	CABC gauss line config register
VOP_BIG_CABC_GAUSS_LINE0_1	0x0214	W	0x00000000	CABC gauss line config register
VOP_BIG_CABC_GAUSS_LINE1_0	0x0218	W	0x00000000	CABC gauss line config register
VOP_BIG_CABC_GAUSS_LINE1_1	0x021c	W	0x00000000	CABC gauss line config register
VOP_BIG_CABC_GAUSS_LINE2_0	0x0220	W	0x00000000	CABC gauss line config register
VOP_BIG_CABC_GAUSS_LINE2_1	0x0224	W	0x00000000	CABC gauss line config register
VOP_BIG_PWM_CTRL	0x0230	W	0x00000000	PWM Control Register , The register provides the cotrol of PWM
VOP_BIG_PWM_PERIOD_HPR	0x0234	W	0x00000000	PWM Period Register/High Polarity Capture Register
VOP_BIG_PWM_DUTY_LPR	0x0238	W	0x00000000	PWM Duty Register/Low Polarity Capture Register
VOP_BIG_PWM_CNT	0x023c	W	0x00000000	PWM Counter Register
VOP_BIG_AFBCD_CTRL	0x0240	W	0x00000000	AFBCD control register
VOP_BIG_AFBCD_HDR_PTR	0x0244	W	0x00000000	AFBC header memory start address
VOP_BIG_AFBCD_PIC_SIZE	0x0248	W	0x00000000	AFBCD picture size
VOP_BIG_AFBCD_PIC_OFFSET	0x024c	W	0x00000000	AFBCD picture offset
VOP_BIG_AFBCD_AXI_CTRL	0x0250	W	0x00000000	AFBCD axi control register
VOP_BIG_AFBCD_DBG0	0x0254	W	0x00000000	AFBCD debug register
VOP_BIG_CABC_LUT_ADDR	0x0400	W	0x00000000	note: used for CABC , base address: 0x400 -- 0x5FF

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Name	Offset	Size	Reset Value	Description
VOP_BIG_HWC_LUT_ADDR	0x0600	W	0x00000000	note: used for HWC BPP format , base address: 0x600 -- 0x9FF
VOP_BIG_GAMMA_LUT_ADDR	0x0a00	W	0x00000000	note: SIZE: 24X256 used for panel GAMMA adjustment, base address: 0x0a00 -- 0x0dff
VOP_BIG_MMU_DTE_ADDR	0x0f00	W	0x00000000	MMU current page Table address
VOP_BIG_MMU_STATUS	0x0f04	W	0x00000000	MMU status register
VOP_BIG_MMU_COMMAND	0x0f08	W	0x00000000	MMU command register
VOP_BIG_MMU_PAGE_FAULT_ADDR	0x0f0c	W	0x00000000	MMU logical address of last page fault
VOP_BIG_MMU_ZAP_ONE_LINE	0x0f10	W	0x00000000	MMU Zap cache line register
VOP_BIG_MMU_INT_RAWSTAT	0x0f14	W	0x00000000	MMU raw interrupt status register
VOP_BIG_MMU_INT_CLEAR	0x0f18	W	0x00000000	MMU raw interrupt status register
VOP_BIG_MMU_INT_MASK	0x0f1c	W	0x00000000	MMU raw interrupt status register
VOP_BIG_MMU_INT_STATUS	0x0f20	W	0x00000000	MMU raw interrupt status register
VOP_BIG_MMU_AUTO_GATING	0x0f24	W	0x00000000	mmu auto gating
VOP_BIG_MMU_CFG_DONE	0x0f28	W	0x00000000	mmu config done reg

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

6.4.3 Detail Register Description

VOP_BIG_REG_CFG_DONE

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_mask When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:6	RO	0x0	reserved
5	RW	0x0	reg_load_sys_en In the first setting of the register, the new value was saved into the mirror register. When all the system register config finish(all reg except win0 win1 hwc iep), writing this register to enable the copyright of the mirror register to real register. Then register would be updated at the start of every frame

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Bit	Attr	Reset Value	Description
4	RW	0x0	reg_load_iep_en In the first setting of the register, the new value was saved into the mirror register. When all the iep register config finish(only 2 signals direct_path_en,direct_path_layer_sel), writing this register to enable the copyright of the mirror register to real register. Then register would be updated at the start of every frame
3	RW	0x0	reg_load_hwc_en In the first setting of the register, the new value was saved into the mirror register. When all the hwc register config finish, writing this register to enable the copyright of the mirror register to real register. Then register would be updated at the start of every frame
2	RW	0x0	reg_load_win1_en In the first setting of the register, the new value was saved into the mirror register. When all the win1 register config finish, writing this register to enable the copyright of the mirror register to real register. Then register would be updated at the start of every frame
1	RW	0x0	reg_load_win0_en In the first setting of the register, the new value was saved into the mirror register. When all the win0 register config finish, writing this register to enable the copyright of the mirror register to real register. Then register would be updated at the start of every frame
0	WO	0x0	reg_load_global_en In the first setting of the register, the new value was saved into the mirror register. When all the register config finish, writing this register to enable the copyright of the mirror register to real register. Then register would be updated at the start of every frame

VOP_BIG_VERSION

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	major used for IP structure
23:16	RO	0x00	minor big feature change under same structure
15:0	RO	0x0000	build rtl current svn number

VOP_BIG_DSP_BG

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:16	RW	0x00	dsp_bg_red Background Red color
15:8	RW	0x00	dsp_bg_green Background Green color
7:0	RW	0x00	dsp_bg_blue Background Blue color

VOP_BIG_MCU

Address: Operational Base + offset (0x000c)

Bit	Attr	Reset Value	Description
31	RW	0x0	mcu_type MCU LCD output SELECT
30	RW	0x0	mcu_bypass MCU LCD BYPASS MODE Select
29	RW	0x0	mcu_rs MCU LCD RS Select 1'b0 : command 1'b1 : data
28	RW	0x0	mcu_frame_st Write"1" : MCU HOLD Mode Frame Start Read : MCU/LCDC standby HOLD status
27	RW	0x0	mcu_hold_mode MCU HOLD Mode Select
26	RW	0x0	mcu_clk_sel 1'b1 : MCU BYPASS sync with DCLK 1'b0 : MCU BYPASS sync with HCLK
25:20	RW	0x00	mcu_rw_pend MCU_RW signal end point (0-63)
19:16	RW	0x0	mcu_rw_pst MCU_RW signal start point (0-15)
15:10	RW	0x00	mcu_cs_pend MCU_CS signal end point (0-63)
9:6	RW	0x0	mcu_cs_pst MCU_CS signal start point (0-15)
5:0	RW	0x00	mcu_pix_total MCU LCD Interface writing period (1-63)

VOP_BIG_SYS_CTRL0

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	reserved Reserved

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VOP_BIG_SYS_CTRL1

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:21	RO	0x0	reserved
20:16	RW	0x00	sw_axi_max_outstand_num axi max outstanding number
15:13	RO	0x0	reserved
12	RW	0x0	sw_axi_max_outstand_en 1'b0: disable 1'b1: enable
11:8	RW	0x0	sw_noc_hurry_threshold noc hurry threshold
7	RO	0x0	reserved
6:5	RW	0x0	sw_noc_hurry_value noc hurry value
4	RW	0x0	sw_noc_hurry_en 1'b0: disable 1'b1: enable
3	RO	0x0	reserved
2:1	RW	0x0	sw_noc_qos_value noc qos value
0	RW	0x0	sw_noc_qos_en 1'b0: disable 1'b1: enable

VOP_BIG_SYS_CTRL2

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15	RW	0x0	dcf_idle_en 1'b0 : dcf idle disable 1'b1 : dcf idle enable
14	RW	0x1	fs_addr_mask_en 1'b0: disable 1'b1: enable
13	RW	0x1	imd_global_regdone_en 1'b0: DISABLE 1'b1: ENALBE
12	RW	0x0	imd_dsp_timing_imd 1'b0: timing reg valid immediatly 1'b1: timing reg valid after frame start
11	RW	0x0	imd_edpi_frm_st wms_fs

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Bit	Attr	Reset Value	Description
10	RW	0x0	imd_edpi_ctrl_mode 1'b0 : wms is enable by te and wms_fs 1'b1 : wms is enable by te only
9	RW	0x0	imd_edpi_te_en 1'b0 : disable TE 1'b1 : enable TE
8	RO	0x0	reserved
7	RW	0x0	sw_io_pad_clk_sel 1'b0: normal dclk out 1'b1: gating dclk out
6	RW	0x0	imd_dsp_data_out_mode 1'b0: normal output mode 1'b1: output 24'b0
5	RO	0x0	reserved
4	RW	0x0	imd_yuv_clip 1'b0: disable, YCbCr no clip 1'b1: enable, YCbCr clip before YCbCr2RGB *Y clip: 16~235, CBCR clip: 16~239
3	RW	0x0	imd_dsp_out_zero 1'b0 : normal output 1'b1 : output '0' means:hsync,vsync,den =000
2	RW	0x0	imd_vop_dma_stop 1'b0: disable 1'b1: enable * If DMA is working, the stop mode would not be active until current bus transfer is finished
1	RW	0x0	imd_vop_standby_en Writing "1" to turn VOP into standby mode, All the layer would disable and the data transfer from frame buffer memory would stop at the end of current frame. The output would be blank. When writing "0" to this bit, standby mode would disable and the VOP go back to work immediately. 1'b0: disable 1'b1: enable * Black display is recommended before setting standby mode enable
0	RW	0x0	imd_auto_gating_en 1'b0: disable 1'b1: enable

VOP_BIG_POST_LB_CTRL

Address: Operational Base + offset (0x001c)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x0	post_lb_almost_empty_threshold post lb almost empty threshold
3:0	RW	0x0	post_lb_almost_full_threshold post lb almost full threshold

VOP_BIG_DSP_CTRL0

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28	RW	0x0	mipi_den_pol 1'b0: positive 1'b1: negative when this channel dclk_en = 0, this signal used for contrl corresponding bit
27	RW	0x0	mipi_vsync_pol 1'b0: negative 1'b1: positive when this channel dclk_en = 0, this signal used for contrl corresponding bit
26	RW	0x0	mipi_hsync_pol 1'b0: negative 1'b1: positive when this channel dclk_en = 0, this signal used for contrl corresponding bit
25	RW	0x0	mipi_dclk_pol 1'b0:mipi dclk inv disable 1'b1:mipi dclk inv enable
24	RW	0x0	mipi_dclk_en 1'b0:mipi dclk disable 1'b1:mipi dclk enable
23:15	RO	0x0	reserved
14	RW	0x0	sw_hdmi_clk_i_sel 1'b0: select dclk to hdmi io 1'b1: select dclk_core to hdmi io
13	RW	0x0	sw_core_clk_sel 1'b0: select dclk sclk 1'b1: select dclk_div sclk_div
12	RW	0x0	hdmi_den_pol 1'b0: positive 1'b1: negative when this channel dclk_en = 0, this signal used for contrl corresponding bit

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Bit	Attr	Reset Value	Description
11	RW	0x0	hdmi_vsync_pol 1'b0: negative 1'b1: positive when this channel dclk_en = 0, this signal used for contrl corresponding bit
10	RW	0x0	hdmi_hsync_pol 1'b0: negative 1'b1: positive when this channel dclk_en = 0, this signal used for contrl corresponding bit
9	RW	0x0	hdmi_dclk_pol 1'b0:hdmi dclk inv disable 1'b1:hdmi dclk inv enable
8	RW	0x1	hdmi_dclk_en 1'b0:hdmi dclk disable 1'b1:hdmi dclk enable
7:5	RO	0x0	reserved
4	RW	0x0	rgb_den_pol 1'b0: positive 1'b1: negative when this channel dclk_en = 0, this signal used for contrl corresponding bit
3	RW	0x0	rgb_vsync_pol 1'b0: negative 1'b1: positive when this channel dclk_en = 0, this signal used for contrl corresponding bit
2	RW	0x0	rgb_hsync_pol 1'b0: negative 1'b1: positive when this channel dclk_en = 0, this signal used for contrl corresponding bit
1	RW	0x0	rgb_dclk_pol 1'b0:rgb dclk inv disable 1'b1:rgb dclk inv enable
0	RW	0x1	rgb_dclk_en 1'b0:rgb dclk disable 1'b1:rgb dclk enable

VOP_BIG_DSP_CTRL1

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	reserved Reserved

VOP_BIG_DSP_CTRL2

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:26	RW	0x0	dsp_layer3_sel Layer3 select 2'b00 : select WIN0 2'b01 : select WIN1 2'b10 : select WIN2
25:24	RW	0x0	dsp_layer2_sel Layer2 select 2'b00 : select WIN0 2'b01 : select WIN1 2'b10 : select WIN2
23:22	RW	0x0	dsp_layer1_sel Layer1 select 2'b00 : select WIN0 2'b01 : select WIN1 2'b10 : select WIN2
21	RO	0x0	reserved
20	RW	0x0	post_lb_mode 1'b0 : 1920x3 1'b1 : 1280x4
19:16	RW	0x0	dsp_out_mode 4'b0000: Parallel 24-bit RGB888 output R[7:0],G[7:0],B[7:0] 4'b0001: Parallel 18-bit RGB666 output 6'b0,R[5:0],G[5:0],B[5:0] 4'b0010: Parallel 16-bit RGB565 output 8'b0,R[4:0],G[5:0],B[4:0] Others: Reserved
15	RW	0x0	dsp_black_en When this bit enable, the pixel data output is all black (0x000000)
14	RW	0x1	dsp_blank_en When this bit enable, the hsync/vsync/den output is blank. means:hsync,vsync,den =110
13	RO	0x0	reserved
12	RW	0x0	dsp_rg_swap 1'b0: RGB 1'b1: GRB
11	RW	0x0	dsp_rb_swap 1'b0: RGB 1'b1: BGR
10	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
9	RW	0x0	dsp_bg_swap 1'b0: RGB 1'b1: RBG
8	RW	0x0	dither_down 1'b0: disable 1'b1: enable
7	RW	0x0	dither_down_sel 1'b0: allegro 1'b1: FRC
6	RW	0x0	dither_down_mode 1'b0: RGB888 to RGB565 1'b1: RGB888 to RGB666
5	RW	0x0	dsp_lut_en 1'b0: disable 1'b1: enable *This bit should be "0" when CPU updates the LUT, and should be "1" when Display LUT mode enable
4	RW	0x0	sw_overlay_mode 1'b0: overlay in rgb domain 1'b1: overlay in yuv domain
3	RW	0x0	dsp_win0_top 1'b0: win1 on the top of win0 1'b1: win0 on the top of win1
2	RW	0x0	dither_up 1'b0: disable 1'b1: enable
1	RW	0x0	interlace_field_pol 1'b0: normal 1'b1: invert
0	RW	0x0	dsp_interlace 1'b0: disable 1'b1: enable *This mode is related to the TVE output, the display timing of odd field must be set correctly. (vop_dsp_vs_st_end_f1/vop_dsp_vact_end_f1)

VOP_BIG_VOP_STATUS

Address: Operational Base + offset (0x002c)

Bit	Attr	Reset Value	Description
31:14	RO	0x0	reserved
13	RW	0x0	intr_post_lb_almost_emtpy_mux 1'b0 : interrupt0 1'b1 : interrupt1

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Bit	Attr	Reset Value	Description
12	RW	0x0	intr_post_lb_almost_full_mux 1'b0 : interrupt0 1'b1 : interrupt1
11	RO	0x0	reserved
10	RW	0x0	intr_line_flag1_mux 1'b0 : interrupt0 1'b1 : interrupt1
9	RW	0x0	intr_line_flag0_mux 1'b0 : interrupt0 1'b1 : interrupt1
8	RW	0x0	intr_dma_finish_mux 1'b0 : interrupt0 1'b1 : interrupt1
7:5	RO	0x0	reserved
4	RO	0x0	dma_stop_valid vop dma stop status
3	RO	0x0	reserved
2	RO	0x0	int_raw_dma_finish dma finish raw singal 1:finish 0:not finish
1	RO	0x0	idle_mmu_ff1 mmu idle status 1:idle 0:busy
0	RO	0x0	dsp_blanking_en_async_aff2 1:blanking enable 0:blanking disable

VOP_BIG_LINE_FLAG

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	dsp_line_flag1_num The display line number when the flag interrupt 1 occur, the range is (0~ DSP_VTOTAL-1)
15:12	RO	0x0	reserved
11:0	RW	0x000	dsp_line_flag0_num The display line number when the flag interrupt occur, the range is (0~ DSP_VTOTAL-1)

VOP_BIG_INTR_EN

Address: Operational Base + offset (0x0034)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_mask When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	mmu_irq_intr_en 1'b0: DISABLE 1'b1: ENABLE
14	RO	0x0	reserved
13	RW	0x0	post_lb_almost_empty_intr_en 1'b0: DISABLE 1'b1: ENABLE
12	RW	0x0	post_lb_almost_full_intr_en 1'b0: DISABLE 1'b1: ENABLE
11	RW	0x0	post_empty_intr_en 1'b0: DISABLE 1'b1: ENABLE
10	RO	0x0	reserved
9	RW	0x0	dma_frm_fsh_intr_en 1'b0: DISABLE 1'b1: ENABLE
8	RW	0x0	dsp_hold_valid_intr_en 1'b0: DISABLE 1'b1: ENABLE
7	RW	0x0	win1_empty_intr_en 1'b0: DISABLE 1'b1: ENABLE
6	RW	0x0	win0_empty_intr_en 1'b0: DISABLE 1'b1: ENABLE
5	RW	0x0	bus_error_intr_en 1'b0: DISABLE 1'b1: ENABLE
4	RW	0x0	line_flag1_intr_en 1'b0: DISABLE 1'b1: ENABLE
3	RW	0x0	line_flag0_intr_en 1'b0: DISABLE 1'b1: ENABLE
2	RW	0x0	addr_same_intr_en 1'b0: DISABLE 1'b1: ENABLE
1	RW	0x0	fs1_intr_en 1'b0: DISABLE 1'b1: ENABLE

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Bit	Attr	Reset Value	Description
0	RW	0x0	fs0_intr_en 1'b0: DISABLE 1'b1: ENABLE

VOP_BIG_INTR_CLEAR

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15	RW	0x0	mmu_irq_intr_clr 1'b0: DISABLE 1'b1: ENABLE
14	RO	0x0	reserved
13	RW	0x0	post_lb_almost_empty_intr_clr 1'b0: DISABLE 1'b1: ENABLE
12	RW	0x0	post_lb_almost_full_intr_clr 1'b0: DISABLE 1'b1: ENABLE
11	RW	0x0	post_empty_intr_clr 1'b0: DISABLE 1'b1: ENABLE
10	RO	0x0	reserved
9	RW	0x0	dma_frm_fsh_intr_clr 1'b0: DISABLE 1'b1: ENABLE
8	W1C	0x0	dsp_hold_valid_intr_clr 1'b0: DISABLE 1'b1: ENABLE
7	W1C	0x0	win1_empty_intr_clr 1'b0: DISABLE 1'b1: ENABLE
6	W1C	0x0	win0_empty_intr_clr 1'b0: DISABLE 1'b1: ENABLE
5	W1C	0x0	bus_error_intr_clr 1'b0: DISABLE 1'b1: ENABLE
4	W1C	0x0	line_flag1_intr_clr 1'b0: DISABLE 1'b1: ENABLE
3	W1C	0x0	line_flag0_intr_clr 1'b0: DISABLE 1'b1: ENABLE

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Bit	Attr	Reset Value	Description
2	W1C	0x0	addr_same_intr_clr 1'b0: DISABLE 1'b1: ENABLE
1	W1C	0x0	fs1_intr_clr 1'b0: DISABLE 1'b1: ENABLE
0	W1C	0x0	fs0_intr_clr 1'b0: DISABLE 1'b1: ENABLE

VOP_BIG_INTR_STATUS

Address: Operational Base + offset (0x003c)

Bit	Attr	Reset Value	Description
31	RW	0x0	mmu_intr_raw_status mmu interrupt raw status
30	RO	0x0	reserved
29	RW	0x0	post_lb_almost_empty_intr_raw_sts post lb almost empty interrupt raw status
28	RW	0x0	post_lb_almost_full_intr_raw post lb almost full interrupt raw status
27	RW	0x0	post_empty_intr_raw post lb empty interrupt raw status
26	RO	0x0	reserved
25	RO	0x0	dma_frm_fsh_intr_raw_sts dma finish interrupt raw status
24	RO	0x0	dsp_hold_valid_intr_raw_sts display hold interrupt raw status
23	RO	0x0	win1_empty_intr_raw_sts win1 empty interrupt raw status
22	RO	0x0	win0_empty_intr_raw_sts win0 empty interrupt raw status
21	RO	0x0	bus_error_intr_raw_sts bus error interrupt raw status
20	RO	0x0	line_flag1_intr_raw_sts line flag1 interrupt raw status
19	RO	0x0	line_flag0_intr_raw_sts line flag0 interrupt raw status
18	RW	0x0	addr_same_intr_raw_sts same address interrupt raw status
17	RO	0x0	fs1_intr_raw_sts new frame start interrupt raw status
16	RO	0x0	fs0_intr_raw_sts frame start interrupt raw status

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Bit	Attr	Reset Value	Description
15	RO	0x0	mmu_intr_status mmu interrupt status
14	RO	0x0	reserved
13	RW	0x0	post_lb_almost_empty_intr_sts post lb almost empty interrupt status
12	RW	0x0	post_lb_almost_full_intr post lb almost full interrupt status
11	RW	0x0	post_empty_intr_sts post lb empty interrupt status
10	RO	0x0	reserved
9	RW	0x0	dma_frm_fsh_intr_sts dma finish interrupt status
8	RO	0x0	dsp_hold_valid_intr_sts display hold interrupt status
7	RO	0x0	win1_empty_intr_sts win1 empty interrupt status
6	RO	0x0	win0_empty_intr_sts win0 empty interrupt status
5	RO	0x0	bus_error_intr_sts bus error interrupt status
4	RO	0x0	line_flag1_intr_sts line flag1 interrupt status
3	RO	0x0	line_flag0_intr_sts line flag0 interrupt status
2	RW	0x0	addr_same_intr_sts same address interrupt status
1	RW	0x0	fs1_intr_sts new frame start interrupt status
0	RO	0x0	fs0_intr_sts frame start interrupt status

VOP_BIG_WIN0_CTRL0

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19	RW	0x0	win0_cbr_deflick 1'b0: disable 1'b1: enable
18	RW	0x0	win0_yrgb_deflick 1'b0: disable 1'b1: enable
17:16	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
15	RW	0x0	win0_uv_swap 1'b0: CrCb 1'b1: CbCr
14	RW	0x0	win0_mid_swap 1'b0: Y3Y2Y1Y0 1'b1: Y3Y1Y2Y0
13	RW	0x0	win0_alpha_swap 1'b0: ARGB 1'b1: RGBA
12	RW	0x0	win0_rb_swap 1'b0: RGB 1'b1: BGR
11:10	RW	0x0	win0_csc_mode Color space conversion: 2'b00/11: mpeg 2'b01: hd 2'b10: jpeg reused by win0 r2y color space conversion: 2'bX0: BT601 2'bX1: BT709
9	RW	0x0	win0_no_outstanding 1'b0: enable 1'b1: disable
8	RW	0x0	win0_interlace_read 1'b0: disable 1'b1: enable
7:4	RO	0x0	reserved
3:1	RW	0x0	win0_data_fmt 3'b000 : ARGB888 3'b001 : RGB888 3'b010 : RGB565 3'b100 : YCbCr420 3'b101 : YCbCr422 3'b110 : YCbCr444 others: reserved
0	RW	0x0	win0_en 1'b0: Win0 layer disable 1'b1: Win0 layer enable

VOP_BIG_WIN0_CTRL1

Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:16	RW	0x2	sw_win0_cbr0_rid

Bit	Attr	Reset Value	Description
15:12	RW	0x1	sw_win0_yrgb0_rid
11:8	RW	0x2	win0_cbr_axi_gather_num
7:4	RW	0x2	win0_yrgb_axi_gather_num
3:2	RW	0x0	win0_dma_burst_length 2'b00: burst16 (burst 15 in rgb888 pack mode) 2'b01: burst8 (burst 12 in rgb888 pack mode) 2'b10: burst4 (burst 6 in rgb888 pack mode)
1	RW	0x0	win0_cbr_axi_gather_en 1'b0: disable 1'b1: enable
0	WO	0x0	win0_yrgb_axi_gather_en 1'b0: disable 1'b1: enable

VOP_BIG_WIN0_COLOR_KEY

Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24	RW	0x0	win0_key_en 1'b0: disable 1'b1: enable
23:0	RW	0x000000	win0_key_color win0 color key

VOP_BIG_WIN0_VIR

Address: Operational Base + offset (0x005c)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x0140	win0_cbr_vir_stride UV420 : ceil(win0_cbr_vir_stride/4) UV422 : ceil(win0_cbr_vir_stride/4) UV444 : ceil(win0_cbr_vir_stride/2)
15:13	RO	0x0	reserved
12:0	RW	0x0140	win0_yrgb_vir_stride Number of words of Win0 Virtual width ARGB888 : win0_yrgb_vir_stride RGB888 : (win0_yrgb_vir_stride*3/4) + win0_yrgb_vir_stride%3) RGB565 : ceil(win0_yrgb_vir_stride/2) YUV : ceil(win0_yrgb_vir_stride/4)

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VOP_BIG_WIN0_YRGB_MST0

Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	win0_yrgb0_mst win0 yrgb memory start address

VOP_BIG_WIN0_CBR_MST0

Address: Operational Base + offset (0x0064)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	win0_cbr0_mst win0 cbcr memory start address

VOP_BIG_WIN0_ACT_INFO

Address: Operational Base + offset (0x0068)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x00ef	win0_act_height win_act_height = (win0 vertical size -1)
15:13	RO	0x0	reserved
12:0	RW	0x013f	win0_act_width win_act_width = (win0 horizontial size -1)

VOP_BIG_WIN0_DSP_INFO

Address: Operational Base + offset (0x006c)

Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved
26:16	RW	0x0ef	dsp_win0_height win0_dsp_height = (win0 vertical size -1)
15:11	RO	0x0	reserved
10:0	RW	0x13f	dsp_win0_width win0_dsp_width = (win0 horizontial size -1)

VOP_BIG_WIN0_DSP_ST

Address: Operational Base + offset (0x0070)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	dsp_win0_yst win0 y-axis start point
15:12	RO	0x0	reserved
11:0	RW	0x00a	dsp_win0_xst win0 x-axis start point

VOP_BIG_WIN0_SCL_FACTOR_YRGB

Address: Operational Base + offset (0x0074)

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Bit	Attr	Reset Value	Description
31:16	RW	0x1000	win0_vs_factor_yrgb factor=((VOP_WIN0_ACT_INFO[31:16])/(VOP_WIN0_DSP_INFO[31:16]))*2^12
15:0	RW	0x1000	win0_hs_factor_yrgb factor=((VOP_WIN0_ACT_INFO[15:0])/(VOP_WIN0_DSP_INFO[15:0]))*2^12

VOP_BIG_WIN0_SCL_FACTOR_CBR

Address: Operational Base + offset (0x0078)

Bit	Attr	Reset Value	Description
31:16	RW	0x1000	win0_vs_factor_cbr YCbCr420: factor=((VOP_WIN0_ACT_INFO[31:16]/ 2)/(VOP_WIN0_DSP_INFO[31:16]))*2^12 YCbCr422,YCbCr444: factor=((VOP_WIN0_ACT_INFO[31:16])/(VOP_WIN0_DSP_INFO[31:16]))*2^12
15:0	RW	0x1000	win0_hs_factor_cbr YCbCr422,YCbCr420: factor=((VOP_WIN0_ACT_INFO[15:0]/2)/(VOP_WIN0_DSP_INFO[15:0]))*2^12 YCbCr444: factor=((VOP_WIN0_ACT_INFO[15:0])/(VOP_WIN0_DSP_INFO[15:0]))*2^12

VOP_BIG_WIN0_SCL_OFFSET

Address: Operational Base + offset (0x007c)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	win0_vs_offset_cbr (0x00~0xff)/0x100 = 0~0.99
23:16	RW	0x00	win0_vs_offset_yrgb (0x00~0xff)/0x100 = 0~0.99
15:8	RW	0x00	win0_hs_offset_cbr (0x00~0xff)/0x100 = 0~0.99
7:0	RW	0x00	win0_hs_offset_yrgb (0x00~0xff)/0x100 = 0~0.99

VOP_BIG_WIN0_ALPHA_CTRL

Address: Operational Base + offset (0x0080)

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Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:4	RW	0x00	win0_alpha_value win0 global alpha value
3	RW	0x0	win0_alpha_sat_mode 1'b0 : alpha value no change 1'b1 : alpha = alpha + alpha[7]
2	RW	0x0	win0_alpha_pre_mul 1'b0 : Non-premultiplied alpha 1'b1 : Premultiplied alpha
1	RW	0x0	win0_alpha_mode 1'b0: user-defined alpha 1'b1: per-pixel alpha
0	RW	0x0	win0_alpha_en 1'b0: disable 1'b1: enable

VOP_BIG_WIN1_CTRL0

Address: Operational Base + offset (0x0090)

Bit	Attr	Reset Value	Description
31:14	RO	0x0	reserved
13	RW	0x0	win1_alpha_swap 1'b0: ARGB 1'b1: RGBA
12	RW	0x0	win1_rb_swap 1'b0: RGB 1'b1: BGR
11:10	RO	0x0	reserved
9	RW	0x0	win1_no_outstanding 1'b0: enable 1'b1: disable
8	RW	0x0	win1_interlace_read 1'b0: disable 1'b1: enable
7	RO	0x0	reserved
6:4	RW	0x0	win1_data_fmt 3'b000 : ARGB888 3'b001 : RGB888 3'b010 : RGB565 others: reserved
3:1	RO	0x0	reserved
0	RW	0x0	win1_en 1'b0: Win1 layer disable 1'b1: Win1 layer enable

VOP_BIG_WIN1_CTRL1

Address: Operational Base + offset (0x0094)

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Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:8	RW	0x5	sw_win1_rid win1 axi read id
7:4	RW	0x0	win1_axi_gather_num win1 axi gather_num gather number
3:2	RW	0x0	win1_dma_burst_length 2'b00: burst16 (burst 15 in rgb888 pack mode) 2'b01: burst8 (burst 12 in rgb888 pack mode) 2'b10: burst4 (burst 6 in rgb888 pack mode)
1	RO	0x0	reserved
0	RW	0x0	win1_axi_gather_en 1'b0: disable 1'b1: enable

VOP_BIG_WIN1_VIR

Address: Operational Base + offset (0x0098)

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12:0	RW	0x0000	win1_vir_stride Number of words of Win1 Virtual width ARGB888 : win1_vir_width RGB888 : (win1_vir_width*3/4) + (win1_vir_width%3) RGB565 : ceil(win1_vir_width/2)

VOP_BIG_WIN1_MST

Address: Operational Base + offset (0x00a0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	win1_mst

VOP_BIG_WIN1_DSP_INFO

Address: Operational Base + offset (0x00a4)

Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved
26:16	RW	0x0ef	dsp_win1_height win1_dsp_height = (win1 dsp vertical size -1)
15:11	RO	0x0	reserved
10:0	RW	0x13f	dsp_win1_width win1_dsp_width = (win1 dsp horizontial size -1)

VOP_BIG_WIN1_DSP_ST

Address: Operational Base + offset (0x00a8)

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Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	dsp_win1_yst win1 y-axis start point
15:12	RO	0x0	reserved
11:0	RW	0x00a	dsp_win1_xst win1 x-axis start point

VOP_BIG_WIN1_COLOR_KEY

Address: Operational Base + offset (0x00ac)

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24	RW	0x0	win1_key_en 1'b0: disable 1'b1: enable
23:0	RW	0x000000	win1_key_color win1 color key

VOP_BIG_WIN1_ALPHA_CTRL

Address: Operational Base + offset (0x00bc)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:4	RW	0x00	win1_alpha_value win1 global alpha value
3	RW	0x0	win1_alpha_sat_mode 1'b0 : alpha value no change 1'b1 : alpha = alpha + alpha[7]
2	RW	0x0	win1_alpha_pre_mul 1'b0 : Non-premultiplied alpha 1'b1 : Premultiplied alpha
1	RW	0x0	win1_alpha_mode 1'b0: user-defined alpha 1'b1: per-pixel alpha
0	RW	0x0	win1_alpha_en 1'b0: disable 1'b1: enable

VOP_BIG_HWC_CTRL0

Address: Operational Base + offset (0x00e0)

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Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x0	sw_hwc_rid hwc axi read id
3	RW	0x0	hwc_lut_en 1'b0: disable 1'b1: enable *This bit should be "0" when CPU updates the LUT, and should be "1" when hwc LUT mode enable
2	RW	0x0	hwc_load_en 1'b0: disable 1'b1: enable *Setting this bit would reload the Hwc data. It would be auto cleared after reload finish
1	RW	0x0	hwc_size 1'b0: 32x32 1'b1: 64x64
0	RW	0x0	hwc_en 1'b0: Hwc layer disable 1'b1: Hwc layer enable

VOP_BIG_HWC_MST

Address: Operational Base + offset (0x00e8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	hwc_mst hwc memory start address

VOP_BIG_HWC_DSP_ST

Address: Operational Base + offset (0x00ec)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	dsp_hwc_yst hwc y-axis start point
15:12	RO	0x0	reserved
11:0	RW	0x000	dsp_hwc_xst hwc x-axis start point

VOP_BIG_HWC_ALPHA_CTRL

Address: Operational Base + offset (0x00f0)

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Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:4	RW	0x00	hwc_alpha_value hwc global alpha value
3	RW	0x0	hwc_alpha_sat_mode 1'b0 : alpha value no change 1'b1 : alpha = alpha + alpha[7]
2	RW	0x0	hwc_alpha_pre_mul 1'b0 : Non-premultiplied alpha 1'b1 : Premultiplied alpha
1	RW	0x0	hwc_alpha_mode 1'b0: user-defined alpha 1'b1: per-pixel alpha
0	RW	0x0	hwc_alpha_en 1'b0: disable 1'b1: enable

VOP_BIG_DSP_HTOTAL_HS_END

Address: Operational Base + offset (0x0100)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x14a	dsp_htotal dsp_htotal
15:12	RO	0x0	reserved
11:0	RW	0x00a	dsp_hs_end dsp_hs_end

VOP_BIG_DSP_HACT_ST_END

Address: Operational Base + offset (0x0104)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x00a	dsp_hact_st dsp_hact_st
15:12	RO	0x0	reserved
11:0	RW	0x000	dsp_hact_end dsp_hact_end

VOP_BIG_DSP_VTOTAL_VS_END

Address: Operational Base + offset (0x0108)

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Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x0fa	dsp_vtotal dsp_vtotal
15:12	RO	0x0	reserved
11:0	RW	0x00a	dsp_vs_end dsp_vs_end

VOP_BIG_DSP_VACT_ST_END

Address: Operational Base + offset (0x010c)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x00a	dsp_vact_st dsp_vact_st
15:12	RO	0x0	reserved
11:0	RW	0x0fa	dsp_vact_end dsp_vact_end

VOP_BIG_DSP_VS_ST_END_F1

Address: Operational Base + offset (0x0110)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	dsp_vs_st_f1 Panel display scanning vertical vsync start point of 2nd field (interlace display mode)
15:12	RO	0x0	reserved
11:0	RW	0x000	dsp_vs_end_f1 Panel display scanning vertical vsync end point of 2nd field(interlace display mode)

VOP_BIG_DSP_VACT_ST_END_F1

Address: Operational Base + offset (0x0114)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	dsp_vact_st_f1 Panel display scanning vertical active start point of 2nd field (interlace display mode)
15:12	RO	0x0	reserved
11:0	RW	0x000	dsp_vact_end_f1 Panel display scanning vertical active end point of 2nd field (interlace display mode)

VOP_BIG_BCSH_CTRL

Address: Operational Base + offset (0x0160)

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Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7	RW	0x0	sw_bcsh_r2y_en 1'b0:bypass 1'b1:enable
6	RW	0x0	sw_bcsh_y2r_en 1'b0:bypass 1'b1:enable
5:4	RW	0x0	sw_bcsh_y2r_csc_mode Color space conversion: 2'b00/11: mpeg 2'b01: hd 2'b10: jpeg
3:2	RW	0x0	video_mode 2'b00 : black 2'b01 : blue 2'b10 : color bar 2'b11 : normal video
1	RW	0x0	sw_bcsh_r2y_csc_mode Color space conversion: 1'b0: BT601 1'b1: BT709
0	RW	0x0	bcsh_en 1'b0 : bcsh bypass 1'b1 : bcsh enable

VOP_BIG_BCSH_COL_BAR

Address: Operational Base + offset (0x0164)

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:16	RW	0x00	color_bar_v v component of color bar
15:8	RW	0x00	color_bar_u u component of color bar
7:0	RW	0x00	color_bar_y y component of color bar

VOP_BIG_BCSH_BCS

Address: Operational Base + offset (0x0168)

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Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x000	sat_con Saturation*Contrast*256 : 0,1.992*1.992
19:17	RO	0x0	reserved
16:8	RW	0x000	contrast Contrast*256 : 0,1.992
7	RO	0x0	reserved
6:0	RW	0x00	brightness Brightness : -128,127

VOP_BIG_BCSH_H

Address: Operational Base + offset (0x016c)

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24:16	RW	0x000	cos_hue cos_hue
15:9	RO	0x0	reserved
8:0	RW	0x000	sin_hue sin_hue

VOP_BIG_FRC_LOWER01_0

Address: Operational Base + offset (0x0170)

Bit	Attr	Reset Value	Description
31:16	RW	0x1284	lower01_frm1 lower01_frm1
15:0	RW	0x4821	lower01_frm0 lower01_frm0

VOP_BIG_FRC_LOWER01_1

Address: Operational Base + offset (0x0174)

Bit	Attr	Reset Value	Description
31:16	RW	0x2148	lower01_frm3 lower01_frm3
15:0	RW	0x8412	lower01_frm2 lower01_frm2

VOP_BIG_FRC_LOWER10_0

Address: Operational Base + offset (0x0178)

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Bit	Attr	Reset Value	Description
31:16	RW	0xa55a	lower10_frm1 lower10_frm1
15:0	RW	0x9696	lower10_frm0 lower10_frm0

VOP_BIG_FRC_LOWER10_1

Address: Operational Base + offset (0x017c)

Bit	Attr	Reset Value	Description
31:16	RW	0x5aa5	lower10_frm3 lower10_frm3
15:0	RW	0x6969	lower10_frm2 lower10_frm2

VOP_BIG_FRC_LOWER11_0

Address: Operational Base + offset (0x0180)

Bit	Attr	Reset Value	Description
31:16	RW	0xdeb7	lower11_frm1 lower11_frm1
15:0	RW	0x7bed	lower11_frm0 lower11_frm0

VOP_BIG_FRC_LOWER11_1

Address: Operational Base + offset (0x0184)

Bit	Attr	Reset Value	Description
31:16	RW	0xed7b	lower11_frm3 lower11_frm3
15:0	RW	0xb7de	lower11_frm2 lower11_frm2

VOP_BIG_MCU_RW_BYPASS_PORT

Address: Operational Base + offset (0x018c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mcu_write_data_bypass mcu write bypass data

VOP_BIG_DBG_REG_SCAN_LINE

Address: Operational Base + offset (0x0190)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RO	0x000	scan_line_num

VOP_BIG_WIN2_CTRL0

Address: Operational Base + offset (0x0190)

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Bit	Attr	Reset Value	Description
31	RW	0x0	win2_endian_swap3 1'b0 : Big-endian 1'b1 : Little-endian
30	RW	0x0	win2_alpha_swap3 1'b0 : ARGB 1'b1 : RGBA
29	RW	0x0	win2_rb_swap3 1'b0 : RGB 1'b1 : BGR
28	RW	0x0	win2_endian_swap2 1'b0 : Big-endian 1'b1 : Little-endian
27	RW	0x0	win2_alpha_swap2 1'b0 : ARGB 1'b1 : RGBA
26	RW	0x0	win2_rb_swap2 1'b0 : RGB 1'b1 : BGR
25	RW	0x0	win2_endian_swap1 1'b0 : Big-endian 1'b1 : Little-endian
24	RW	0x0	win2_alpha_swap1 1'b0 : ARGB 1'b1 : RGBA
23	RW	0x0	win2_rb_swap1 1'b0 : RGB 1'b1 : BGR
22	RW	0x0	win2_endian_swap0 1'b0 : Big-endian 1'b1 : Little-endian
21	RW	0x0	win2_alpha_swap0 1'b0 : ARGB 1'b1 : RGBA
20	RW	0x0	win2_rb_swap0 1'b0 : RGB 1'b1 : BGR
19	RO	0x0	reserved
18:17	RW	0x0	win2_data_fmt3 2'b00 : ARGB888 2'b01 : RGB888 2'b10 : RGB565 2'b11 : 8bpp
16	RW	0x0	win2_mst3_en 1'b0 : disable 1'b1 : enable

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15	RO	0x0	reserved
14:13	RW	0x0	win2_data_fmt2 2'b00 : ARGB888 2'b01 : RGB888 2'b10 : RGB565 2'b11 : 8bpp
12	RW	0x0	win2_mst2_en 1'b0 : disable 1'b1 : enable
11	RO	0x0	reserved
10:9	RW	0x0	win2_data_fmt1 2'b00 : ARGB888 2'b01 : RGB888 2'b10 : RGB565 2'b11 : 8bpp
8	RW	0x0	win2_mst1_en 1'b0 : disable 1'b1 : enable
7	RO	0x0	reserved
6:5	RW	0x0	win2_data_fmt0 2'b00 : ARGB888 2'b01 : RGB888 2'b10 : RGB565 2'b11 : 8bpp
4	RW	0x0	win2_mst0_en 1'b0 : disable 1'b1 : enable
3:2	RW	0x0	win2_csc_mode Color space conversion: 2'b00: BT601_L 2'b01: BT709_L 2'b10: BT601_F 2'b11: BT2020
1	RW	0x0	win2_interlace_read 1'b0 : disable 1'b1 : enable
0	RW	0x0	win2_en 1'b0 : disable 1'b1 : enable

VOP_BIG_WIN2_CTRL1

Address: Operational Base + offset (0x0194)

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Bit	Attr	Reset Value	Description
31:22	RO	0x0	reserved
21:17	RW	0x1d	win2_axi_max_outstanding_num win2 axi max outstanding number
16	RW	0x0	win2_axi_max_outstanding_en 1'b0 : disable 1'b1 : enable
15	RW	0x0	win2_y_mir_en 1'b0 : no y_mirror 1'b1 : y_mirror
14	RW	0x0	win2_no_outstanding 1'b0 : enable 1'b1 : disable
13:12	RO	0x0	reserved
11:8	RW	0x0	win2_rid axi read id of win2 channel
7:4	RW	0x0	win2_axi_gather_num win2 axi gather transfer number
3:2	RW	0x0	win2_dma_burst_length 2'b00 : burst16 (burst 15 in rgb888 pack mode) 2'b01 : burst8 (burst 12 in rgb888 pack mode) 2'b10 : burst4 (burst 6 in rgb888 pack mode) 2'b11 : reserved
1	RO	0x0	reserved
0	RW	0x0	win2_axi_gather_en 1'b0 : disable 1'b1 : enable

VOP_BIG_WIN2_VIR0_1

Address: Operational Base + offset (0x0198)

Bit	Attr	Reset Value	Description
31:16	RW	0x0140	win2_vir_stride1 Number of words of Win2 Virtual1 width ARGB888 : win2_vir_width1 RGB888 : (win2_vir_width1 * 3/4) + (win2_vir_width1 % 3) RGB565 : ceil(win2_vir_width1 / 2) 8BPP : ceil(win2_vir_width1 / 4) 4BPP : ceil(win2_vir_width1 / 8) 2BPP : ceil(win2_vir_width1 / 16) 1BPP : ceil(win2_vir_width1 / 32)

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Bit	Attr	Reset Value	Description
15:0	RW	0x0140	win2_vir_stride0 Number of words of Win2 Virtual0 width ARGB888 : win2_vir_width0 RGB888 : (win2_vir_width0 * 3/4) + (win2_vir_width0 % 3) RGB565 : ceil(win2_vir_width0 / 2) 8BPP : ceil(win2_vir_width0 / 4) 4BPP : ceil(win2_vir_width0 / 8) 2BPP : ceil(win2_vir_width0 / 16) 1BPP : ceil(win2_vir_width0 / 32)

VOP_BIG_WIN2_VIR2_3

Address: Operational Base + offset (0x019c)

Bit	Attr	Reset Value	Description
31:16	RW	0x0140	win2_vir_stride3 Number of words of Win2 Virtual3 width ARGB888 : win2_vir_width3 RGB888 : (win2_vir_width3 * 3/4) + (win2_vir_width3 % 3) RGB565 : ceil(win2_vir_width3 / 2) 8BPP : ceil(win2_vir_width3 / 4) 4BPP : ceil(win2_vir_width3 / 8) 2BPP : ceil(win2_vir_width3 / 16) 1BPP : ceil(win1_vir_width3 / 32)
15:0	RW	0x0140	win2_vir_stride2 Number of words of Win2 Virtual2 width ARGB888 : win2_vir_width2 RGB888 : (win2_vir_width2 * 3/4) + (win2_vir_width2 % 3) RGB565 : ceil(win2_vir_width2 / 2) 8BPP : ceil(win2_vir_width2 / 4) 4BPP : ceil(win2_vir_width2 / 8) 2BPP : ceil(win2_vir_width2 / 16) 1BPP : ceil(win1_vir_width2 / 32)

VOP_BIG_WIN2_MST0

Address: Operational Base + offset (0x01a0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	win2_mst0 must be alianed to 8byte address

VOP_BIG_WIN2_DSP_INFO0

Address: Operational Base + offset (0x01a4)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x0ef	win2_dsp_height0 win2_dsp_height0 = size -1

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Bit	Attr	Reset Value	Description
15:12	RO	0x0	reserved
11:0	RW	0x13f	win2_dsp_width0 win2_dsp_width = size -1

VOP_BIG_WIN2_DSP_ST0

Address: Operational Base + offset (0x01a8)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x000a	win2_dsp_yst0 Win2 vertical start point(y) of the Panel scanning
15:13	RO	0x0	reserved
12:0	RW	0x000a	win2_dsp_xst0 Win2 horizontal start point(x) of the Panel scanning

VOP_BIG_WIN2_COLOR_KEY

Address: Operational Base + offset (0x01ac)

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24	RW	0x0	win2_key_en 1'b0 : disable 1'b1 : enable
23:0	RW	0x000000	win2_key_color Win2 key color

VOP_BIG_WIN2_MST1

Address: Operational Base + offset (0x01b0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	win2_mst1 *must be alianed to 8byte address

VOP_BIG_WIN2_DSP_INFO1

Address: Operational Base + offset (0x01b4)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x0ef	win2_dsp_height1 win2_dsp_height0 = size -1
15:12	RO	0x0	reserved
11:0	RW	0x13f	win2_dsp_width1 win2_dsp_width = size -1

VOP_BIG_WIN2_DSP_ST1

Address: Operational Base + offset (0x01b8)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x000a	win2_dsp_yst1 Win2 vertical start point(y) of the Panel scanning
15:13	RO	0x0	reserved
12:0	RW	0x000a	win2_dsp_xst1 Win2 horizontal start point(x) of the Panel scanning

VOP_BIG_WIN2_ALPHA_CTRL

Address: Operational Base + offset (0x01bc)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:4	RW	0x00	win2_alpha_value win2 global alpha value
3	RW	0x0	win2_alpha_sat_mode 1'b0:alpha value no change 1'b1:alpha=alpha + alpha[7]
2	RW	0x0	win2_alpha_pre_mul 1'b0:Non-premultiplied alpha 1'b1:Premultiplied alpha
1	RW	0x0	win2_alpha_mode 1'b0:user-defined alpha 1'b1:per-pixel alpha
0	RW	0x0	win2_alpha_en 1'b0:disable 1'b1:enable

VOP_BIG_WIN2_MST2

Address: Operational Base + offset (0x01c0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	win2_mst2 *must be alianed to 8byte address

VOP_BIG_WIN2_DSP_INFO2

Address: Operational Base + offset (0x01c4)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x0ef	win2_dsp_height2 win2_dsp_height0 = size -1
15:12	RO	0x0	reserved
11:0	RW	0x13f	win2_dsp_width2 win2_dsp_width = size -1

VOP_BIG_WIN2_DSP_ST2

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Address: Operational Base + offset (0x01c8)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x000a	win2_dsp_yst2 Win2 vertical start point(y) of the Panel scanning
15:13	RO	0x0	reserved
12:0	RW	0x000a	win2_dsp_xst2 Win2 horizontal start point(x) of the Panel scanning

VOP_BIG_WIN2_MST3

Address: Operational Base + offset (0x01d0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	win2_mst3 *must be alianed to 8byte address

VOP_BIG_WIN2_DSP_INFO3

Address: Operational Base + offset (0x01d4)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x0ef	win2_dsp_height3 win2_dsp_height0 = size -1
15:12	RO	0x0	reserved
11:0	RW	0x13f	win2_dsp_width3 win2_dsp_width = size -1

VOP_BIG_WIN2_DSP_ST3

Address: Operational Base + offset (0x01d8)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RW	0x000a	win2_dsp_yst3 Win2 vertical start point(y) of the Panel scanning
15:13	RO	0x0	reserved
12:0	RW	0x000a	win2_dsp_xst3 Win2 horizontal start point(x) of the Panel scanning

VOP_BIG_BLANKING_VALUE

Address: Operational Base + offset (0x01f4)

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24	RW	0x0	blanking_value_config_en 1'b0 : disable 1'b1 : enable
23:0	WO	0x000000	sw_blanking_value blank value

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VOP_BIG_FLAG_REG_FRM_VALID

Address: Operational Base + offset (0x01f8)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	flag_reg_frm_valid valid by frame start

VOP_BIG_FLAG_REG

Address: Operational Base + offset (0x01fc)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	flag_reg

VOP_BIG_CABC_CTRL0

Address: Operational Base + offset (0x0200)

Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved
26:4	RW	0x000000	cabc_calc_pixel_num cabc calc pixel numbers = x % * cabc_total_num
3	RW	0x0	cabc_handle_en cabc control pwm
2:1	RW	0x0	pwm_config_mode 2'b00 : last frame pwm value 2'b01 : cur frame pwm value 2'b1x : stage by stage
0	RW	0x0	cabc_en 1'b0 : cabc disable 1'b1 : cabc enable

VOP_BIG_CABC_CTRL1

Address: Operational Base + offset (0x0204)

Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved
26:4	RW	0x000000	cabc_total_num cabc totala numbers = h_vd * v_vd
3:1	RO	0x0	reserved
0	RW	0x0	cabc_lut_en cabc pwm lut enable

VOP_BIG_CABC_CTRL2

Address: Operational Base + offset (0x0208)

Bit	Attr	Reset Value	Description
31	RW	0x0	max_scale_cfg_enable 1'b0 : disable 1'b1 : enable

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Bit	Attr	Reset Value	Description
30:29	RO	0x0	reserved
28:20	RW	0x000	max_scale_cfg_value The max scale value
19	RW	0x0	cabc_stage_up_mode 1'b0: mul mode 1'b1: add mode
18:17	RO	0x0	reserved
16:8	RW	0x000	cabc_stage_up when mul mode ,scale stage up (1~1.5 * 256). when add mode ,scale stage up (0x00~0xff)
7:0	RW	0x00	cabc_stage_down when mul mode ,scale stage down (0.667~1 * 256). when add mode ,scale stage down (0x00~0xff)

VOP_BIG_CABC_CTRL3

Address: Operational Base + offset (0x020c)

Bit	Attr	Reset Value	Description
31:9	RO	0x0	reserved
8	RW	0x0	cabc_global_dn_limit_en cabc global scale down limit enable
7:0	RW	0x00	cabc_global_dn cabc global scale down value

VOP_BIG_CABC_GAUSS_LINE0_0

Address: Operational Base + offset (0x0210)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	t_line0_3 gauss parameter t_line0_3
23:16	RW	0x00	t_line0_2 gauss parameter t_line0_2
15:8	RW	0x00	t_line0_1 gauss parameter t_line0_1
7:0	RW	0x00	t_line0_0 gauss parameter t_line0_0

VOP_BIG_CABC_GAUSS_LINE0_1

Address: Operational Base + offset (0x0214)

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:16	RW	0x00	t_line0_6 gauss parameter t_line0_6
15:8	RW	0x00	t_line0_5 gauss parameter t_line0_5

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	t_line0_4 gauss parameter t_line0_4

VOP_BIG_CABC_GAUSS_LINE1_0

Address: Operational Base + offset (0x0218)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	t_line1_3 gauss parameter t_line1_3
23:16	RW	0x00	t_line1_2 gauss parameter t_line1_2
15:8	RW	0x00	t_line1_1 gauss parameter t_line1_1
7:0	RW	0x00	t_line1_0 gauss parameter t_line1_0

VOP_BIG_CABC_GAUSS_LINE1_1

Address: Operational Base + offset (0x021c)

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:16	RW	0x00	t_line1_6 gauss parameter t_line1_6
15:8	RW	0x00	t_line1_5 gauss parameter t_line1_5
7:0	RW	0x00	t_line1_4 gauss parameter t_line1_4

VOP_BIG_CABC_GAUSS_LINE2_0

Address: Operational Base + offset (0x0220)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	t_line2_3 gauss parameter t_line2_3
23:16	RW	0x00	t_line2_2 gauss parameter t_line2_2
15:8	RW	0x00	t_line2_1 gauss parameter t_line2_1
7:0	RW	0x00	t_line2_0 gauss parameter t_line2_0

VOP_BIG_CABC_GAUSS_LINE2_1

Address: Operational Base + offset (0x0224)

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:16	RW	0x00	t_line2_6 gauss parameter t_line2_6

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Bit	Attr	Reset Value	Description
15:8	RW	0x00	t_line2_5 gauss parameter t_line2_5
7:0	RW	0x00	t_line2_4 gauss parameter t_line2_4

VOP_BIG_PWM_CTRL

Address: Operational Base + offset (0x0230)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	rpt This field defines the repeated effective periods of output waveform in one-shot mode. The value N means N+1 repeated effective periods
23:16	RW	0x00	scale This fields defines the scale factor applied to prescaled clock. The value N means the clock is divided by 2*N. If N is 0, it means that the clock is divided by 512(2*256)
15	RO	0x0	reserved
14:12	RW	0x0	prescale This field defines the prescale factor applied to input clock. The value N means that the input clock is divided by 2^N
11:10	RO	0x0	reserved
9	RW	0x0	clk_sel 1'b0: non-scaled clock is selected as PWM clock source. It means that the prescale clock is directly used as the PWM clock source 1'b1: scaled clock is selected as PWM clock source
8	RW	0x0	lp_en 1'b0: disabled 1'b1: enabled When PWM channel is inactive state and Low Power Mode is enabled, the path to PWM Clock prescale module is blocked to reduce power consumption
7:6	RO	0x0	reserved
5	RW	0x0	output_mode 1'b0: left aligned mode 1'b1: center aligned mode
4	RW	0x0	inactive_pol This defines the output waveform polarity when PWM channel is in inactive state. The inactive state means that PWM finishes the complete waveform in one-shot mode or PWM channel is disabled. 1'b0: negative 1'b1: positive

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Bit	Attr	Reset Value	Description
3	RW	0x0	duty_pol This defines the polarity for duty cycle. PWM starts the output waveform with duty cycle. 1'b0: negative 1'b1: positive
2:1	RW	0x0	pwm_mode 2'b00: One shot mode. PWM produces the waveform within the repeated times defined by PWMx_CTRL_rpt . 2'b01: Continuous mode. PWM produces the waveform continuously 2'b10: Capture mode. PWM measures the cycles of high/low polarity of input waveform. 2'b11: reserved
0	RW	0x0	pwm_en 1'b0: disabled 1'b1: enabled. If the PWM is worked the one-shot mode, this bit will be cleared at the end of operation

VOP_BIG_PWM_PERIOD_HPR

Address: Operational Base + offset (0x0234)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pwm_period If PWM is operated at the continuous mode or one-shot mode, this value defines the period of the output waveform. Note that, if the PWM is operated at the center-aligned mode, the period should be an even one, and therefore only the bit [31:1] is taken into account and bit [0] always considered as 0. If PWM is operated at the capture mode, this value indicates the effective high polarity cycles of input waveform. This value is based on the PWM clock. The value ranges from 0 to (2^32-1)

VOP_BIG_PWM_DUTY_LPR

Address: Operational Base + offset (0x0238)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pwm_duty If PWM is operated at the continuous mode or one-shot mode, this value defines the duty cycle of the output waveform. The PWM starts the output waveform with duty cycle. Note that, if the PWM is operated at the center-aligned mode, the period should be an even one, and therefore only the [31:1] is taken into account. If PWM is operated at the capture mode, this value indicates the effective low polarity cycles of input waveform. This value is based on the PWM clock. The value ranges from 0 to (2^32-1)

VOP_BIG_PWM_CNT

Address: Operational Base + offset (0x023c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pwm_cnt The 32-bit indicates current value of PWM Channel 0 counter. The counter runs at the rate of PWM clock. The value ranges from 0 to (2^32-1)

VOP_BIG_AFBCD_CTRL

Address: Operational Base + offset (0x0240)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	pic_vir_width afbc header virtual stride
15:8	RO	0x0	reserved
7:4	RW	0x0	afbcd_format 4'b0000 : AFBC_R5G6B5 4'b0100 : AFBC_R8G8B8 4'b0101 : AFBC_R8G8B8A8
3	RW	0x0	rb_swap 1'b0:ARGB 1'b1:ABGR
2	RW	0x0	alpha_swap 1'b0 : ARGB 1'b1:RGBA
1	RW	0x0	endian_swap 1'b0 : ARGB8888 1'b1 : BGRA8888
0	RW	0x0	afbcd_en 1'b0 : disable 1'b1 : enable

VOP_BIG_AFBCD_HDR_PTR

Address: Operational Base + offset (0x0244)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	afbcd_hdr_ptr AFBC header memory start address

VOP_BIG_AFBCD_PIC_SIZE

Address: Operational Base + offset (0x0248)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	afbcd_pic_height afbc pic height , real -1
15:0	RW	0x0000	afbcd_pic_width afbc pic width , real -1

VOP_BIG_AFBCD_PIC_OFFSET

Address: Operational Base + offset (0x024c)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	afbcd_pic_yoffset AFBC pic y-offset
15:0	RW	0x0000	afbcd_pic_xoffset AFBC pic x-offset

VOP_BIG_AFBCD_AXI_CTRL

Address: Operational Base + offset (0x0250)

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:20	RW	0x0	afbcd_hdr_gather_num
19:16	RW	0x0	afbcd_pld_outstanding_num
15:12	RW	0x0	afbcd_hdr_outstanding_num
11	RO	0x0	reserved
10	RW	0x0	afbcd_hdr_gather_en
9	RW	0x0	afbcd_pld_outstanding_en
8	RW	0x0	afbcd_hdr_outstanding_en
7:4	RW	0x0	afbcd_pld_rid payload axi read id
3:0	RW	0x0	afbcd_hdr_rid header axi read id

VOP_BIG_AFBCD_DBG0

Address: Operational Base + offset (0x0254)

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Bit	Attr	Reset Value	Description
31:3	RO	0x0	reserved
2	RW	0x0	afbcd_dec_resp afbcd decode respone
1	RW	0x0	afbcd_axi_rresp afbcd axi read respone
0	RW	0x0	afbcd_idle_n afbcd idle status

VOP_BIG_CABC_LUT_ADDR

Address: Operational Base + offset (0x0400)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	Field0000 Description

VOP_BIG_HWC_LUT_ADDR

Address: Operational Base + offset (0x0600)

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:0	RW	0x000000	hwc_lut_addr Field0000 Description

VOP_BIG_GAMMA_LUT_ADDR

Address: Operational Base + offset (0x0a00)

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:0	RW	0x000000	gamma_lut_addr

VOP_BIG_MMU_DTE_ADDR

Address: Operational Base + offset (0x0f00)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MMU_DTE_ADDR MMU DTE address

VOP_BIG_MMU_STATUS

Address: Operational Base + offset (0x0f04)

Bit	Attr	Reset Value	Description
31:10	RO	0x0	reserved
9:5	RW	0x00	PAGE_FAULT_BUS_ID Index of master reponsible for last page fault
4	RW	0x0	PAGE_FAULT_IS_WRITE The direction of access for last page fault: 0 = Read 1 = Write

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Bit	Attr	Reset Value	Description
3	RW	0x0	MMU_IDLE The MMU is idle when accesses are being translated and there are no unfinished translated accesses
2	RW	0x0	STAIL_ACTIVE MMU stall mode currently enabled. The mode is enabled by command
1	RW	0x0	PAGE_FAULT_ACTIVE MMU page fault mode currently enabled . The mode is enabled by command
0	RW	0x0	PAGING_ENABLED Paging is enabled

VOP_BIG_MMU_COMMAND

Address: Operational Base + offset (0x0f08)

Bit	Attr	Reset Value	Description
31:3	RO	0x0	reserved
2:0	RW	0x0	MMU_CMD MMU_CMD. This can be: 3'b000: MMU_ENABLE_PAGING 3'b001: MMU_DISABLE_PAGING 3'b010: MMU_ENABLE_STALL 3'b011: MMU_DISABLE_STALL 3'b100: MMU_ZAP_CACHE 3'b101: MMU_PAGE_FAULT_DONE 3'b110: MMU_FORCE_RESET

VOP_BIG_MMU_PAGE_FAULT_ADDR

Address: Operational Base + offset (0x0f0c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PAGE_FAULT_ADDR address of last page fault

VOP_BIG_MMU_ZAP_ONE_LINE

Address: Operational Base + offset (0x0f10)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MMU_ZAP_ONE_LINE address to be invalidated from the page table cache

VOP_BIG_MMU_INT_RAWSTAT

Address: Operational Base + offset (0x0f14)

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Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x0	READ_BUS_ERROR read bus error
0	RW	0x0	PAGE_FAULT page fault

VOP_BIG_MMU_INT_CLEAR

Address: Operational Base + offset (0x0f18)

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x0	READ_BUS_ERROR read bus error
0	RW	0x0	PAGE_FAULT page fault

VOP_BIG_MMU_INT_MASK

Address: Operational Base + offset (0x0f1c)

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x0	READ_BUS_ERROR read bus error
0	RW	0x0	PAGE_FAULT page fault

VOP_BIG_MMU_INT_STATUS

Address: Operational Base + offset (0x0f20)

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x0	READ_BUS_ERROR read bus error
0	RW	0x0	PAGE_FAULT page fault

VOP_BIG_MMU_AUTO_GATING

Address: Operational Base + offset (0x0f24)

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x0	sw_mmu_cfg_mode when it is 1'b0, the mmu reg config will valid after frame start
0	RW	0x0	mmu_auto_gating when it is 1'b1, the mmu will auto gating it self

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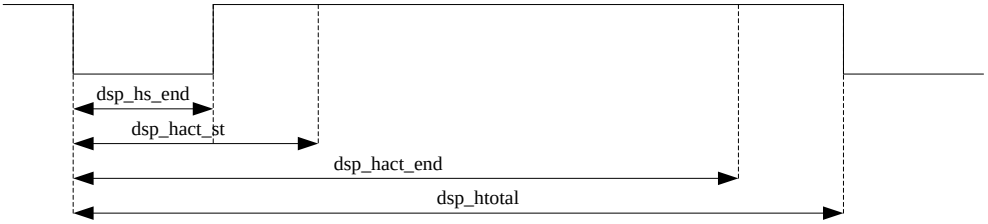
VOP_BIG_MMU_CFG_DONE

Address: Operational Base + offset (0x0f28)

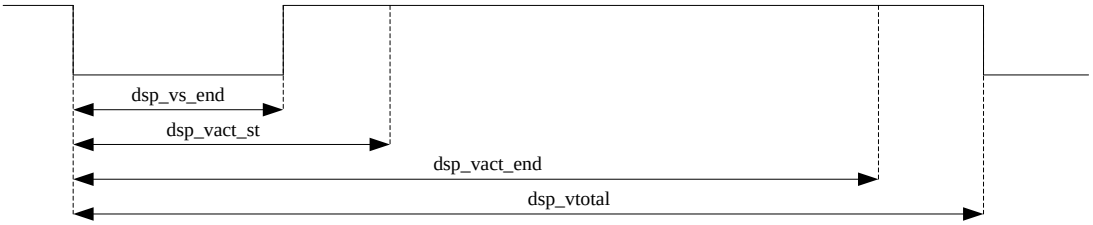
Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	reg_load_mmu_en In the first setting of the register, the new value was saved into the mirror register. When all the mmu register config finish, writing this register to enable the copyright of the mirror register to real register

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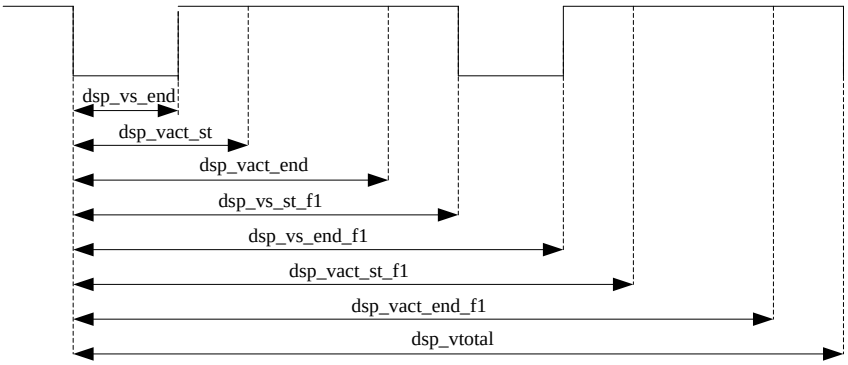
6.5 Timing Diagram



Horizontal timing



Vertical timing(Progressive mode)



Vertical timing(Interlace mode)

Fig. 6-17 VOP RGB interface timing setting

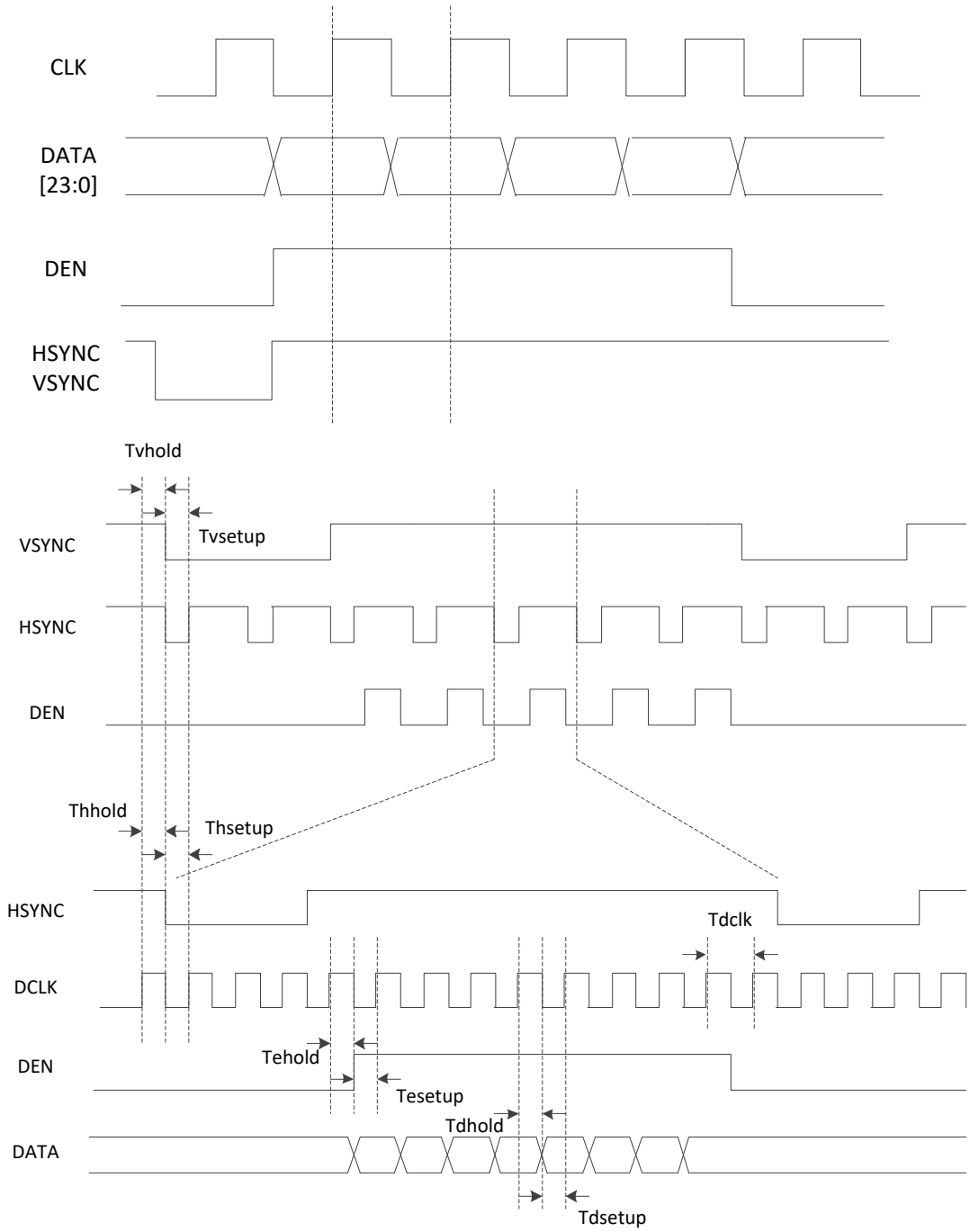


Fig. 6-18 VOP RGB Interface Timing(SDR)

6.6 Interface Description

6.6.1 VOP Outputs

VOP supports RGB, MIPI, LVDS output. VOP is suitable for different display mode by different usage, which is shown as follows.

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Table 6-3 VOP Control Pins Definition

Display mode	RGB Parallel 24-bit	RGB Parallel 18-bit	RGB Parallel 16-bit
DCLK	DCLK	DCLK	DCLK
VSYNC	VSYNC	VSYNC	VSYNC
HSYNC	HSYNC	HSYNC	HSYNC
DEN	DEN	DEN	DEN
DATA	DATA[23:0]	DATA[17:0]	DATA[15:0]

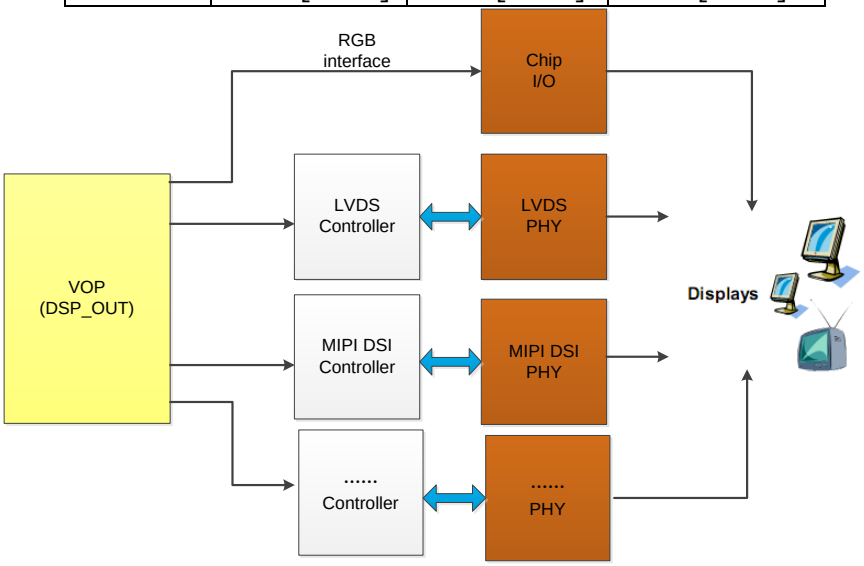


Fig. 6-19 VOP Display output for peripherals

6.7 Application Notes

6.7.1 DMA transfer mode

There are three DMA transfer modes for loading win0 or win1 frame data determined by following parameters(X=0,1):
dma_burst_length
winX_no_outstanding
winX_gather_en
winX_gather_thres

6.7.2 auto outstanding transfer mode(random transfer)

When winX_no_outstanding is 0, multi-bursts transfer command could be sent out to AXI master interface continuously if the internal memory has enough space to store new data. The continuous random burst number is in the range of 1 to 4, mainly depending on the empty level of internal memory, dma_burst_length, data format and active image width.

1. configured outstanding transfer mode(fixed transfer)

When winX_gather_en is 1, fixed-number of bursts transfer command should be sent out to AXI master interface continuously if the internal memory has enough space to store new data. The fixed-number is determined by winX_gather_thres. Since the internal memory size is limited, there is some restriction for the winX_gather_thres as follows.

Table 6-4 Gather configuration for all format

Gather Threshold	dma_burst_length =2'b00(burst16)	dma_burst_length =2'b01(burst8)	dma_burst_length =2'b10(burst4)
YCbCr420 YCbCr422 YCbCr444	0	0,1,2	0,1,2,3
ARGB888 RGB888 RGB565	0,1,2,3	0,1,2,3	0,1,2,3
8BPP	0,1,2,3	0,1,2,3	0,1,2,3

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6.7.3 GAMMA LUT

When dsp_lut_en is 0, the DSP LUT data should be refreshed by software. i.e, writing dsp lut data to the internal memory with the start address DSP_LUT_MST. The memory size is 256x24, i.e, lower 24bits valid, and the writing data number is determined by software.

6.7.4 DMA control（QoS/Hurry/Outstanding）

If you want to get higher priority for VOP to access external memory when the frame data is urgent, a QoS and hurry request can be generated and sent out basing on the configured values:

sw_noc_qos_en: SYS_CTRL1[0]
sw_noc_qos_value: SYS_CTRL1[2:1]
sw_noc_hurry_en: SYS_CTRL1[4]
sw_noc_hurry_value: SYS_CTRL1[6:5]
sw_noc_hurry_threshold: SYS_CTRL1[11:8]
sw_axi_max_outstand_en: SYS_CTRL1[12]
sw_axi_max_outstand_num: SYS_CTRL1[20:16]

QoS request for higher bus priority for win1
NOC hurry for higher bus priority for VIO when win0 needs higher priority.
Max Outstanding num is configurable.

6.7.5 Interrupt

VOP interrupt is comprised of 14 interrupt sources:

- frame start0 interrupt
- frame start1 interrupt
- address same interrupt
- line flag0 interrupt
- line flag1 interrupt
- bus error interrupt
- Win0 empty interrupt
- Win1 empty interrupt
- Display hold interrupt
- DMA finish interrupt
- Post empty interrupt
- Post lb almost full interrupt
- Post lb almost empty interrupt
- MMU interrupt

Every interrupt has independent interrupt enable signal(VOP_INT_EN),interrupt clear signal(VOP_INT_CLR) and interrupt raw status signal (VOP_INT_STATUS).
There is only one interrupt combined with all this interrupt signals to cpu , and it high active.
Dma finish interrupt is used for changing DDR frequency. This interrupt will be asserted when dma finish getting all the Pixel DATA every frame. This interrupt is asserted at the end of the frame.
Address same interrupt will be asserted at this kind of scenario that all the memory start address configured in VOP reg are same compared with the former frame. This interrupt is asserted at the beginning of frame start.
The difference between frame start0 interrupt and frame start1 interrupt is that frame start0 interrupt will be asserted every frame, while the frame start1 interrupt will be masked when all the memory start address are same.

6.7.6 RGB display mode

RGB display mode is used for RGB panel display. It is a continuous frames display mode.

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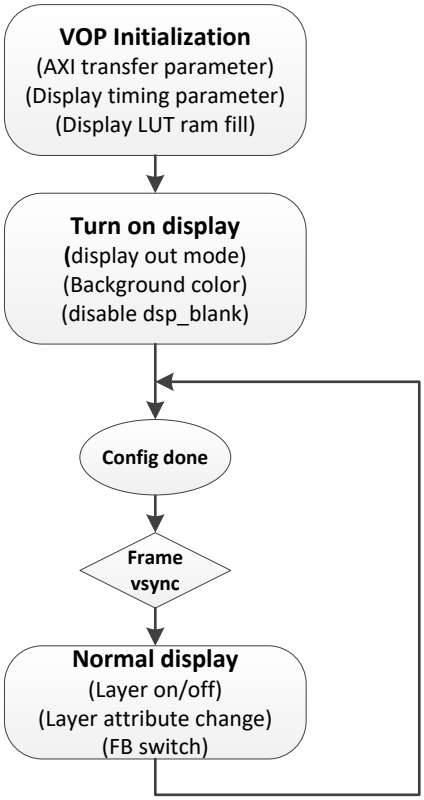


Fig. 6-20 VOP RGB Mode Programming Flow

1.VOP initialization

VOP initialization should be done before turning display on.

First, AXI bus parameter (VOP_SYS_CTRL1) should be set for DMA transfer.

Second, display panel/interface timing should be set for display output. The registers are: VOP_DSP_HTOTAL_HS_END/ VOP_DSP_HACT_ST_END/ VOP_DSP_VTOTAL_HS_END/ VOP_DSP_VACT_ST_END/ VOP_DSP_VS_ST_END_F1/ VOP_DSP_VACT_ST_END_F1

2.Background display

Before normal display, the background display could be turn on.

First, set display output mode (VOP_DSP_CTRL0/1) according to display device.

Second, disable dsp_blank mode, which would not be enable until frame synchronization.

Finally, writing '1' to "VOP_REG_CFG_DONE" register then all the frame-sync registers will be enable at the beginning of next frame.

3.Normal display

In normal display, all the display layers' attribute could be different according display scenario. So there is a programming loop in this mode.

First, configure all the display layers' attribute registers for the change of image format, location, size, scaling factor, alpha and overlay and so on. Those register would not be enable until frame synchronization.

Finally, write 1 to "VOP_REG_CFG_DONE" register then all the frame-sync registers will be enable at the beginning of next frame.

6.7.7 Immediately control register

There are two type registers in VOP , one is effective immediately, the other is effective by frame sync. Effective immediately registers list as follows, other registers are all effective by frame sync.

Table 6-5 effective immediately register table

register address	description
0x0008	background
0x0018	All display and control signal registers
0xe0~0xf4	Frc configuration bits

6.7.8 Output Polarity Control

There are four channel outputs(RGB HDMI LVDS MIPI , some may not support because SOC

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do not have the related interface) ,every channel has its own xxx_dclk_en, xxx_dclk_pol, xxx_hsync_pol, xxx_vsync_pol, xxx_den_pol.
The xxx_dclk_en should be set to 1 when output select the xxx channel, and the other channel's xxx_dclk_en should be set to 0 to gate the output clk and data.
When using RGB panel, the dclk should be tied to "0" or "1" in some scenarios.
In this case, you should enable sw_io_pad_clk_sel, to tie dclk to "0". If enable rgb_dclk_pol at the same time, the dclk will tie to "1".

6.7.9 Some special control

- The blanking value of VSYNC could be configured through reg BLANKING_VALUE;
- The current scan line number could be read through reg_addr 0x190;
- There is a FLAG_REG which is readable and writable. This FLAG_REG does not for config function , our software staff may use it in the future. After writing a meaningful 32bit value to FLAG_REG, we can read it before frame valid through reading 0x1fc value, and can get the same value after frame valid reading 0x1f8 value;

6.7.10 RGB PATH

TTL typical configuration is as follows:

```
Word32(GRF_BASE + GRF_CPIO3A_IOMUX_SEL_L) = 0x11111111 ;
Word32(GRF_BASE + GRF_CPIO3A_IOMUX_SEL_H) = 0x11111111 ;
Word32(GRF_BASE + GRF_CPIO3B_IOMUX_SEL_L) = 0x11111111 ;
Word32(GRF_BASE + GRF_CPIO3B_IOMUX_SEL_H) = 0x11111111 ;
Word32(GRF_BASE + GRF_CPIO3C_IOMUX_SEL_L) = 0x11111111 ;
Word32(GRF_BASE + GRF_CPIO3C_IOMUX_SEL_H) = 0x11111111 ;
Word32(GRF_BASE + GRF_CPIO3D_IOMUX_SEL_L) = 0x11111111 ;
```

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Chapter 7 Video Output Processor (VOP_LITE)

7.1 Overview

Video Output Processor is a video process engine and a display interface from memory frame buffer to display device(LCD panel,MIPI,LVDS,RGB,ect). VOP is connected to an AHB bus through an AHB slave and AXI bus through an AXI master. The register setting is configured through the AHB slave interface and the display frame data is read through the AXI master interface.

7.1.1 Features

VOP_LITE supports the following features:

- Display interface
  - Parallel RGB LCD Interface: 24-bit(RGB888),18-bit(RGB666), 16-bit(RGB565)
  - Display interface
    - Parallel Display interface
    - MIPI_DSI_TX
    - LVDS
  - Max input/output resolution
    - 1920x1080
- Display process
  - Background layer
    - programmable 24-bit color
  - Win1 layer
    - RGB888, ARGB888, RGB565
    - Support virtual display
    - 256 level alpha blending (pre-multiplied alpha support)
    - Transparency color key
    - RGB2YCbCr(BT601/BT709)
      - HWC layer
        - Support 8BPP only
        - Size : 32x32 or 64x64
    - 256 level alpha blending (pre-multiplied alpha support)
    - RGB2YCbCr(BT601/BT709)
- Others
  - Support RGB or YUV domain overlay
  - BCSH(Brightness,Contrast,Saturation,Hue adjustment)
  - BCSH:YCbCr2RGB(rec601-mpeg/ rec601-jpeg/rec709)
  - BCSH:RGB2YCbCr(BT601/BT709)
  - Support Gamma adjust for PAD
  - Support dither down allegro RGB888to666 RGB888to565 & dither down frc (configurable) RGB888to666
  - Blank and black display
  - Standby mode
  - Support QoS request for higher bus priority for win1/HWC
  - Support DMA stop mode
  - Support all layers reg_done separately

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7.2 Block Diagram

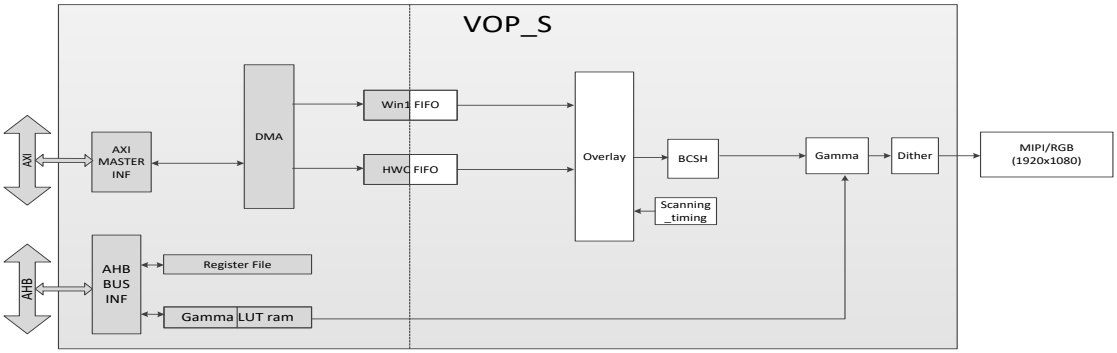


Fig. 7-1 VOP Block Diagram

7.3 Function Description

7.3.1 Data Format

VOP master read the frame data from the frame buffer in the system memory. There are total 6 formats supported in three layers.

- Win1: RGB888, ARGB888, RGB565

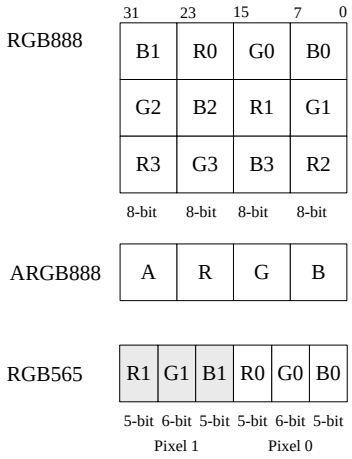


Fig. 7-2 VOP Frame Buffer Data Format

	D[31:24]	D[23:16]	D[15:8]	D[7:0]
000H	P1	P2	P3	P4
004H	P5	P6	P7	P8
008H	P9	P10	P11	P12
...				

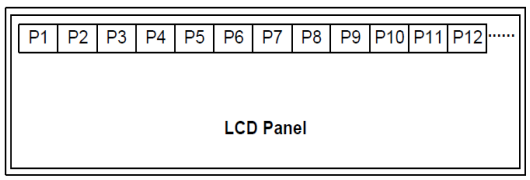


Fig. 7-3 VOP Win1 Palette (8bpp)

Data SWAP function

There are several swap options for different frame data formats..
All the data swap types are in the following table.

Table 7-1 VOP Data Swap of Win0 and Win1

Data-swap	RB swap	Alpha swap	Y-M8 swap	CbCr swap
Win1	yes	yes	No	No

7.3.2 Data path

There are two data input path for VOP to get display layers' pixel data. One is internal DMA;

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the other is direction path interface.

1.Internal DMA

Internal DMA can fetch the pixel data through AXI bus from system memory (DDR) for all the display layers. Data fetching is driven by display output requirement.

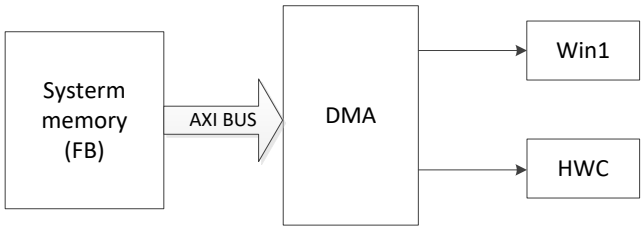


Fig. 7-4 VOP Internal DMA

7.3.3 Virtual display

Virtual display is supported in Win0 and Win1. The active image is part of the virtual (original) image in frame buffer memory. The virtual width is indicated by setting WIN0/WIN1_VIR_STRIDE for different data format.

The virtual stride should be multiples of word (32-bit). That means dummy bytes in the end of virtual line if the real pixels are not 32-bit aligned.

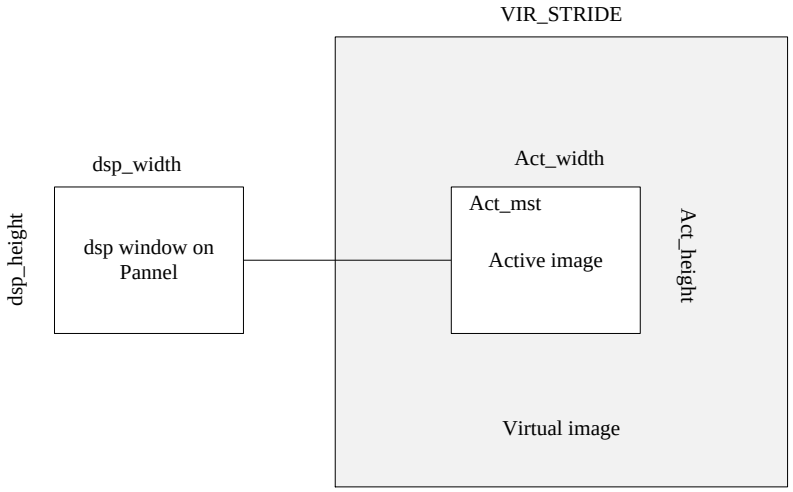


Fig. 7-5 VOP Virtual Display Mode

7.3.4 Overlay

1. Overlay display

There are totally 3 layers for overlay display: Background, Win1 and Hwc.

The background is a programmable solid color layer, which is always the bottom of the display screen.

Hwc is a 32x32 or 64x64 8BPP color palette layer, which is the top layer of the display screen. dsp_hwc_data[23:0] come from the HWC_LUT, which input is a 8BPP data format and output is 24 bits dsp_hwc_data.

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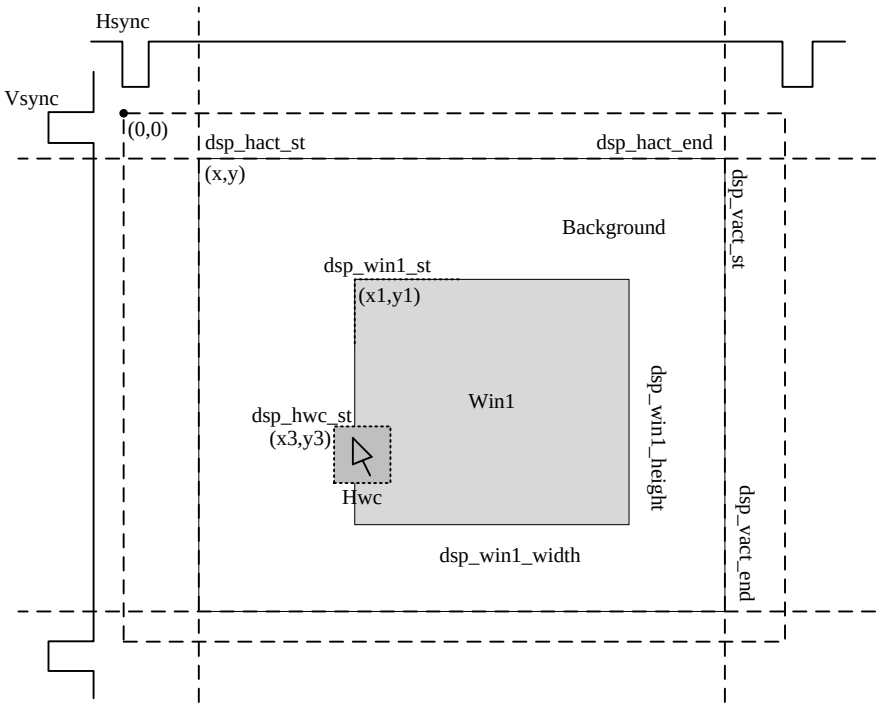


Fig. 7-6 VOP Overlay Display

2.

2. Alpha Blending

Two blending modes are supported. One is per-pixel (ARGB) mode; the other is user-specified mode. In ARGB mode, the alpha value is in the ARGB data . In user-specified mode, the alpha value comes from the register (WINX_ALPHA_CTRL[11: 4]).

Pre-multiplied alpha are supported for per-pixel alpha in Win0 and Win 1, for Pre-multiplied alpha, the SRC data has already been multiplied with alpha value.

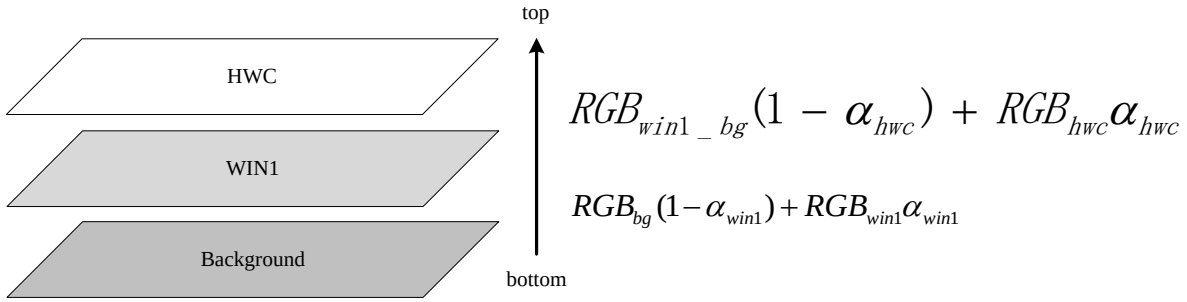


Fig. 7-7 VOP Alpha blending

7.3.5 BCSH

The BCSH block is used for brightness, contrast, saturation and hue adjustment to YCbCr format image.

The following diagram shows the BCSH adjustment processing. All the factors should be set in the VOP registers.

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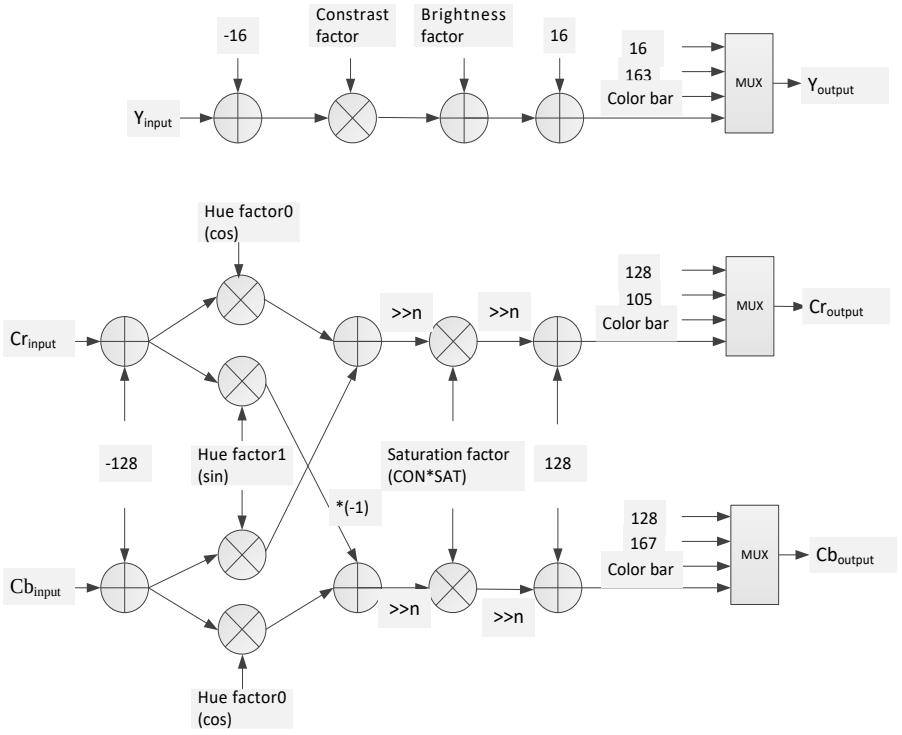


Fig. 7-8 VOP BCSH Diagram

7.3.6 Gamma Correction

Gamma correction is necessary because most monitors don't have a linear relationship between the voltage and the brightness, which results in your scene looking like it has too much contrast and the light falling off from the source outward, happens too quickly. The result can also be problematic if you are going into a composition program.

You can correct this by "Gamma Correction", which allows you to display the images and textures on your computer in an accurate manner.

Your screen is not linear, in that it displays the brightness unevenly. As a result, the image looks to be more high contrast than it should, you end up adding more lights or turning up the intensity, or you don't use the lighting in a realistic way that matches well with live action scenes. It also creates problems for you if you use compositing software.

It consumes 256x8bit LUT for each channel. You can write gamma correction LUT through register" DSP_LUT_ADDR" one by one after set dsp_lut_en = 0.

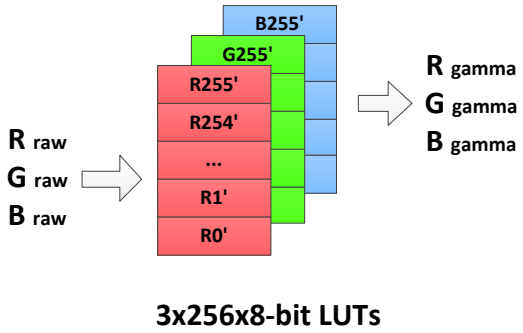


Fig. 7-8 VOP Gamma LUTs

7.3.7 Replication and dither down

1 Replication (dither up)

If the interface data bus is wider than the pixel format size, by programming the pixel components replication active/inactive, the MSB is replicated to the LSB of the interface data bus or the LSB is filled with 0s.

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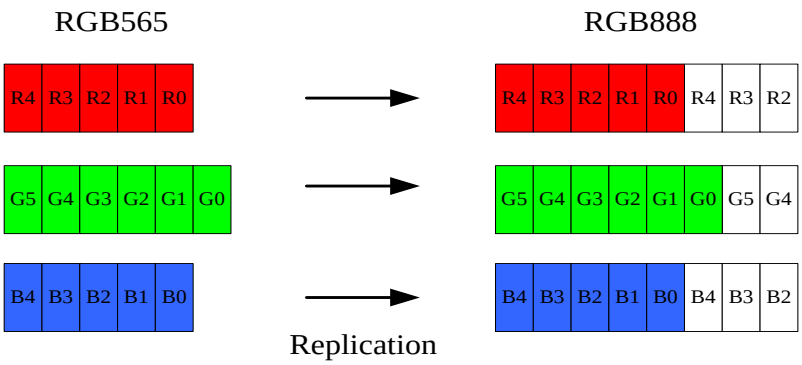


Fig. 7-9 VOP Replication

Dithering is used to improve the quality of display the pixel data in a lower color depth on the LCD panel. The Dithering algorithm is based on the (x,y) pixel position, the value of removed bits and frame counter.

2 Dither down

Here we support three kinds of dithering arithmetic. RGB888 to RGB666 has two ways, one is allegro, the other is FRC. RGB888 to RGB565 has only one arithmetic, which is allegro. When Dithering is not enabled, the MSBs of the pixel color components are output on the interface data bus if the interface data bus is smaller than the pixel format size.

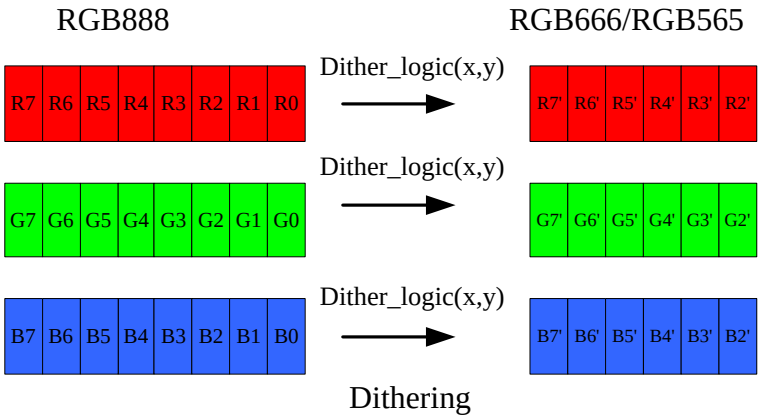


Fig. 7-10 vop dithering

The following figure is the recommended pattern picture in vop, you can config different value of reg 0x170~0x184，to change the pattern picture.(default value is recommended values below)

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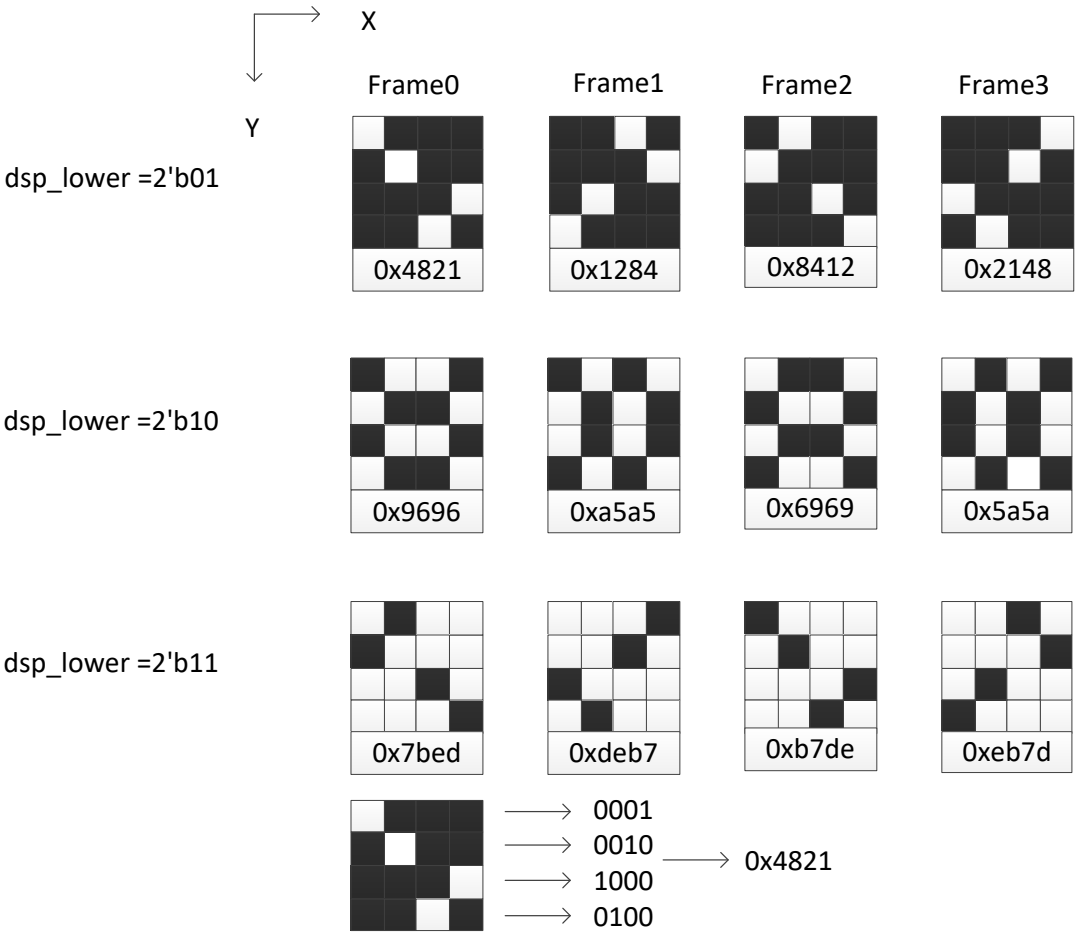


Fig. 7-11 frc pattern diagram

Recommended pattern:
0x170 : 0x12844821
0x174 : 0x21488412
0x178 : 0x55aaaa55
0x17f : 0x55aaaa55
0x180 : 0xdeb77bed
0x184 : 0xed7bb7de

7.4 Register Description

7.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

7.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
VOP_LITE_REG_CFG_DONE	0x0000	W	0x00000000	Register config done flag
VOP_LITE_VERSION	0x0004	W	0x00000000	Version for vop
VOP_LITE_DSP_BG	0x0008	W	0x00000000	Display control register
VOP_LITE_MCU	0x000c	W	0x00000000	MCU control register
VOP_LITE_SYS_CTRL0	0x0010	W	0x00000000	System control register
VOP_LITE_SYS_CTRL1	0x0014	W	0x00000000	System control register
VOP_LITE_SYS_CTRL2	0x0018	W	0x00006000	System control register

Name	Offset	Size	Reset Value	Description
VOP_LITE_DSP_CTRL0	0x0020	W	0x00000101	Display register
VOP_LITE_DSP_CTRL1	0x0024	W	0x00000000	Display register
VOP_LITE_DSP_CTRL2	0x0028	W	0x00004000	Display register
VOP_LITE_VOP_STATUS	0x002c	W	0x00000000	Some vop module status
VOP_LITE_LINE_FLAG	0x0030	W	0x00000000	Line flag config register
VOP_LITE_INTR_EN	0x0034	W	0x00000000	Interrupt enable register
VOP_LITE_INTR_CLEAR	0x0038	W	0x00000000	Interrupt clear register
VOP_LITE_INTR_STATUS	0x003c	W	0x00000000	Interrupt raw status and interrupt status
VOP_LITE_WIN1_CTRL0	0x0090	W	0x00000000	Win1 ctrl register
VOP_LITE_WIN1_CTRL1	0x0094	W	0x00000500	Win1 ctrl register
VOP_LITE_WIN1_VIR	0x0098	W	0x00000000	Win1 virtual stride
VOP_LITE_WIN1_MST	0x00a0	W	0x00000000	Win1 memory start address
VOP_LITE_WIN1_DSP_INFO	0x00a4	W	0x00ef013f	Win1 display width/height on panel
VOP_LITE_WIN1_DSP_ST	0x00a8	W	0x0000000a	Win1 display start point on panel
VOP_LITE_WIN1_COLOR_KEY	0x00ac	W	0x00000000	Win1 color key register
VOP_LITE_WIN1_ALPHA_CTRL	0x00bc	W	0x00000000	Blending control register
VOP_LITE_HWC_CTRL0	0x00e0	W	0x00000000	Hwc ctrl register
VOP_LITE_HWC_MST	0x00e8	W	0x00000000	Hwc memory start address
VOP_LITE_HWC_DSP_ST	0x00ec	W	0x00000000	Hwc display start point on panel
VOP_LITE_HWC_ALPHA_CTRL	0x00f0	W	0x00000000	Blending control register
VOP_LITE_DSP_HTOTAL_HS_END	0x0100	W	0x014a000a	Panel scanning horizontal width and hsync pulse end point
VOP_LITE_DSP_HACT_ST_END	0x0104	W	0x000a0000	Panel active horizontal scanning start point and end point
VOP_LITE_DSP_VTOTAL_VS_END	0x0108	W	0x00fa000a	Panel scanning vertical height and vsync pulse end point
VOP_LITE_DSP_VACT_ST_END	0x010c	W	0x000a00fa	Panel active vertical scanning start point and end point
VOP_LITE_DSP_VS_ST_END_F1	0x0110	W	0x00000000	Vertical scanning start point and vsync pulse end point of even file
VOP_LITE_DSP_VACT_ST_END_F1	0x0114	W	0x00000000	Vertical scanning active start point and end point of even filed in interlac
VOP_LITE_BCSH_CTRL	0x0160	W	0x00000000	Brightness/Contrast enhancement/Saturation/Hue contrl
VOP_LITE_BCSH_COL_BAR	0x0164	W	0x00000000	vedio mode equals 2,then output color bar yuv 24bits value

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Name	Offset	Size	Reset Value	Description
VOP_LITE_BCSH_BCS	0x0168	W	0x00000000	Brightness/Contrast enhancement/Saturation
VOP_LITE_BCSH_H	0x016c	W	0x00000000	Hue
VOP_LITE_FRC_LOWER01_0	0x0170	W	0x12844821	Frc algorithm configuration register
VOP_LITE_FRC_LOWER01_1	0x0174	W	0x21488412	Frc algorithm configuration register
VOP_LITE_FRC_LOWER10_0	0x0178	W	0xa55a9696	Frc algorithm configuration register
VOP_LITE_FRC_LOWER10_1	0x017c	W	0x5aa56969	Frc algorithm configuration register
VOP_LITE_FRC_LOWER11_0	0x0180	W	0xdeb77bed	Frc algorithm configuration register
VOP_LITE_FRC_LOWER11_1	0x0184	W	0xed7bb7de	Frc algorithm configuration register
VOP_LITE_MCU_RW_BYPASS_PORT	0x018c	W	0x00000000	MCU panel write data
VOP_LITE_DBG_REG_SCAN_LINE	0x0190	W	0x00000000	Current line number of dsp timing
VOP_LITE_BLANKING_VALUE	0x0194	W	0x00000000	The value of vsync blanking
VOP_LITE_FLAG_REG_FRM_VALID	0x0198	W	0x00000000	Flag reg value after frame valid
VOP_LITE_FLAG_REG	0x019c	W	0x00000000	Flag reg value before frame valid
VOP_LITE_HWC_LUT_ADDR	0x0600	W	0x00000000	note: used for HWC BPP format , base address: 0x600 -- 0x9FF
VOP_LITE_GAMMA_LUT_ADDR	0x0a00	W	0x00000000	note: SIZE: 24X256 used for panel GAMMA adjustment, base address: 0x0a00 -- 0x0dff
VOP_LITE_MMU_DTE_ADDR	0x0f00	W	0x00000000	MMU current page Table address
VOP_LITE_MMU_STATUS	0x0f04	W	0x00000000	MMU status register
VOP_LITE_MMU_COMMAND	0x0f08	W	0x00000000	MMU command register
VOP_LITE_MMU_PAGE_FAULT_ADDR	0x0f0c	W	0x00000000	MMU logical address of last page fault
VOP_LITE_MMU_ZAP_ONE_LINE	0x0f10	W	0x00000000	MMU Zap cache line register
VOP_LITE_MMU_INT_RAWSTAT	0x0f14	W	0x00000000	MMU raw interrupt status register
VOP_LITE_MMU_INT_CLEAR	0x0f18	W	0x00000000	MMU raw interrupt status register

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Name	Offset	Size	Reset Value	Description
VOP_LITE_MMU_INT_MASK	0x0f1c	W	0x00000000	MMU raw interrupt status register
VOP_LITE_MMU_INT_STATUS	0x0f20	W	0x00000000	MMU raw interrupt status register
VOP_LITE_MMU_AUTO_GATING	0x0f24	W	0x00000000	mmu auto gating
VOP_LITE_MMU_CFG_DONE	0x0f28	W	0x00000000	mmu config done reg

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

7.4.3 Detail Register Description

VOP_LITE_REG_CFG_DONE

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_mask When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:6	RO	0x0	reserved
5	RW	0x0	reg_load_sys_en In the first setting of the register, the new value was saved into the mirror register. When all the system register config finish(all reg except win0 win1 hwc iep), writing this register to enable the copyright of the mirror register to real register. Then register would be updated at the start of every frame
4	RW	0x0	reg_load_iep_en In the first setting of the register, the new value was saved into the mirror register. When all the iep register config finish(only 2 signals direct_path_en,direct_path_layer_sel), writing this register to enable the copyright of the mirror register to real register. Then register would be updated at the start of every frame
3	RW	0x0	reg_load_hwc_en In the first setting of the register, the new value was saved into the mirror register. When all the hwc register config finish, writing this register to enable the copyright of the mirror register to real register. Then register would be updated at the start of every frame
2	RW	0x0	reg_load_win1_en In the first setting of the register, the new value was saved into the mirror register. When all the win1 register config finish, writing this register to enable the copyright of the mirror register to real register. Then register would be updated at the start of every frame

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Bit	Attr	Reset Value	Description
1	RW	0x0	reg_load_win0_en In the first setting of the register, the new value was saved into the mirror register. When all the win0 register config finish, writing this register to enable the copyright of the mirror register to real register. Then register would be updated at the start of every frame
0	WO	0x0	reg_load_global_en In the first setting of the register, the new value was saved into the mirror register. When all the register config finish, writing this register to enable the copyright of the mirror register to real register. Then register would be updated at the start of every frame

VOP_LITE_VERSION

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:24	RO	0x00	major used for IP structure
23:16	RO	0x00	minor big feature change under same structure
15:0	RO	0x0000	build rtl current svn number

VOP_LITE_DSP_BG

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:16	RW	0x00	dsp_bg_red Background Red color
15:8	RW	0x00	dsp_bg_green Background Green color
7:0	RW	0x00	dsp_bg_blue Background Blue color

VOP_LITE_MCU

Address: Operational Base + offset (0x000c)

Bit	Attr	Reset Value	Description
31	RW	0x0	mcu_type MCU LCD output SELECT
30	RW	0x0	mcu_bypass MCU LCD BYPASS MODE Select

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Bit	Attr	Reset Value	Description
29	RW	0x0	mcu_rs MCU LCD RS Select 1'b0 : command 1'b1 : data
28	RW	0x0	mcu_frame_st Write"1" : MCU HOLD Mode Frame Start Read : MCU/LCDC standby HOLD status
27	RW	0x0	mcu_hold_mode MCU HOLD Mode Select
26	RW	0x0	mcu_clk_sel 1'b1 : MCU BYPASS sync with DCLK 1'b0 : MCU BYPASS sync with HCLK
25:20	RW	0x00	mcu_rw_pend MCU_RW signal end point (0-63)
19:16	RW	0x0	mcu_rw_pst MCU_RW signal start point (0-15)
15:10	RW	0x00	mcu_cs_pend MCU_CS signal end point (0-63)
9:6	RW	0x0	mcu_cs_pst MCU_CS signal start point (0-15)
5:0	RW	0x00	mcu_pix_total MCU LCD Interface writing period (1-63)

VOP_LITE_SYS_CTRL0

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	reserved Reserved

VOP_LITE_SYS_CTRL1

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:21	RO	0x0	reserved
20:16	RW	0x00	sw_axi_max_outstand_num axi max outstanding number
15:13	RO	0x0	reserved
12	RW	0x0	sw_axi_max_outstand_en 1'b0: disable 1'b1: enable
11:8	RW	0x0	sw_noc_hurry_threshold noc hurry threshold
7	RO	0x0	reserved
6:5	RW	0x0	sw_noc_hurry_value noc hurry value

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Bit	Attr	Reset Value	Description
4	RW	0x0	sw_noc_hurry_en 1'b0: disable 1'b1: enable
3	RO	0x0	reserved
2:1	RW	0x0	sw_noc_qos_value noc qos value
0	RW	0x0	sw_noc_qos_en 1'b0: disable 1'b1: enable

VOP_LITE_SYS_CTRL2

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15	RW	0x0	dcf_idle_en 1'b0 : dcf idle disable 1'b1 : dcf idle enable
14	RW	0x1	fs_addr_mask_en 1'b0: disable 1'b1: enable
13	RW	0x1	imd_global_regdone_en 1'b0: DISABLE 1'b1: ENALBE
12	RW	0x0	imd_dsp_timing_imd 1'b0: timing reg valid immediatly 1'b1: timing reg valid after frame start
11	RW	0x0	imd_edpi_frm_st wms_fs
10	RW	0x0	imd_edpi_ctrl_mode 1'b0 : wms is enable by te and wms_fs 1'b1 : wms is enable by te only
9	RW	0x0	imd_edpi_te_en 1'b0 : disable TE 1'b1 : enable TE
8	RO	0x0	reserved
7	RW	0x0	sw_io_pad_clk_sel 1'b0: normal dclk out 1'b1: gating dclk out
6	RW	0x0	imd_dsp_data_out_mode 1'b0: normal output mode 1'b1: output 24'b0
5	RO	0x0	reserved
4	RW	0x0	imd_yuv_clip 1'b0: disable, YCbCr no clip 1'b1: enable, YCbCr clip before YCbCr2RGB *Y clip: 16~235, CBCR clip: 16~239

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Bit	Attr	Reset Value	Description
3	RW	0x0	imd_dsp_out_zero 1'b0 : normal output 1'b1 : output '0' means:hsync,vsync,den =000
2	RW	0x0	imd_vop_dma_stop 1'b0: disable 1'b1: enable * If DMA is working, the stop mode would not be active until current bus transfer is finished
1	RW	0x0	imd_vop_standby_en Writing "1" to turn VOP into standby mode, All the layer would disable and the data transfer from frame buffer memory would stop at the end of current frame. The output would be blank. When writing "0" to this bit, standby mode would disable and the VOP go back to work immediately. 1'b0: disable 1'b1: enable * Black display is recommended before setting standby mode enable
0	RW	0x0	imd_auto_gating_en 1'b0: disable 1'b1: enable

VOP_LITE_DSP_CTRL0

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28	RW	0x0	mipi_den_pol 1'b0: positive 1'b1: negative when this channel dclk_en = 0, this signal used for contrl corresponding bit
27	RW	0x0	mipi_vsync_pol 1'b0: negative 1'b1: positive when this channel dclk_en = 0, this signal used for contrl corresponding bit
26	RW	0x0	mipi_hsync_pol 1'b0: negative 1'b1: positive when this channel dclk_en = 0, this signal used for contrl corresponding bit
25	RW	0x0	mipi_dclk_pol 1'b0:mipi dclk inv disable 1'b1:mipi dclk inv enable

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Bit	Attr	Reset Value	Description
24	RW	0x0	mipi_dclk_en 1'b0:mipi dclk disable 1'b1:mipi dclk enable
23:15	RO	0x0	reserved
14	RW	0x0	sw_hdmi_clk_i_sel 1'b0: select dclk to hdmi io 1'b1: select dclk_core to hdmi io
13	RW	0x0	sw_core_clk_sel 1'b0: select dclk sclk 1'b1: select dclk_div sclk_div
12	RW	0x0	hdmi_den_pol 1'b0: positive 1'b1: negative when this channel dclk_en = 0, this signal used for contrl corresponding bit
11	RW	0x0	hdmi_vsync_pol 1'b0: negative 1'b1: positive when this channel dclk_en = 0, this signal used for contrl corresponding bit
10	RW	0x0	hdmi_hsync_pol 1'b0: negative 1'b1: positive when this channel dclk_en = 0, this signal used for contrl corresponding bit
9	RW	0x0	hdmi_dclk_pol 1'b0:hdmi dclk inv disable 1'b1:hdmi dclk inv enable
8	RW	0x1	hdmi_dclk_en 1'b0:hdmi dclk disable 1'b1:hdmi dclk enable
7:5	RO	0x0	reserved
4	RW	0x0	rgb_den_pol 1'b0: positive 1'b1: negative when this channel dclk_en = 0, this signal used for contrl corresponding bit
3	RW	0x0	rgb_vsync_pol 1'b0: negative 1'b1: positive when this channel dclk_en = 0, this signal used for contrl corresponding bit

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Bit	Attr	Reset Value	Description
2	RW	0x0	rgb_hsync_pol 1'b0: negative 1'b1: positive when this channel dclk_en = 0, this signal used for contrl corresponding bit
1	RW	0x0	rgb_dclk_pol 1'b0:rgb dclk inv disable 1'b1:rgb dclk inv enable
0	RW	0x1	rgb_dclk_en 1'b0:rgb dclk disable 1'b1:rgb dclk enable

VOP_LITE_DSP_CTRL1

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	reserved Reserved

VOP_LITE_DSP_CTRL2

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:16	RW	0x0	dsp_out_mode 4'b0000: Parallel 24-bit RGB888 output R[7:0],G[7:0],B[7:0] 4'b0001: Parallel 18-bit RGB666 output 6'b0,R[5:0],G[5:0],B[5:0] 4'b0010: Parallel 16-bit RGB565 output 8'b0,R[4:0],G[5:0],B[4:0] Others: Reserved
15	RW	0x0	dsp_black_en When this bit enable, the pixel data output is all black (0x000000)
14	RW	0x1	dsp_blank_en When this bit enable, the hsync/vsync/den output is blank. means:hsync,vsync,den =110
13	RO	0x0	reserved
12	RW	0x0	dsp_rg_swap 1'b0: RGB 1'b1: GRB
11	RW	0x0	dsp_rb_swap 1'b0: RGB 1'b1: BGR
10	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
9	RW	0x0	dsp_bg_swap 1'b0: RGB 1'b1: RBG
8	RW	0x0	dither_down 1'b0: disable 1'b1: enable
7	RW	0x0	dither_down_sel 1'b0: allegro 1'b1: FRC
6	RW	0x0	dither_down_mode 1'b0: RGB888 to RGB565 1'b1: RGB888 to RGB666
5	RW	0x0	dsp_lut_en 1'b0: disable 1'b1: enable *This bit should be "0" when CPU updates the LUT, and should be "1" when Display LUT mode enable
4	RW	0x0	sw_overlay_mode 1'b0: overlay in rgb domain 1'b1: overlay in yuv domain
3	RW	0x0	dsp_win0_top 1'b0: win1 on the top of win0 1'b1: win0 on the top of win1
2	RW	0x0	dither_up 1'b0: disable 1'b1: enable
1	RW	0x0	interlace_field_pol 1'b0: normal 1'b1: invert
0	RO	0x0	reserved

VOP_LITE_VOP_STATUS

Address: Operational Base + offset (0x002c)

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4	RO	0x0	dma_stop_valid vop dma stop status
3	RO	0x0	reserved
2	RO	0x0	int_raw_dma_finish dma finish raw singal 1:finish 0:not finish

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Bit	Attr	Reset Value	Description
1	RO	0x0	idle_mmu_ff1 mmu idle status 1:idle 0:busy
0	RO	0x0	dsp_blanking_en_async_aff2 1:blanking enable 0:blanking disable

VOP_LITE_LINE_FLAG

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	dsp_line_flag1_num The display line number when the flag interrupt 1 occur, the range is (0~ DSP_VTOTAL-1)
15:12	RO	0x0	reserved
11:0	RW	0x000	dsp_line_flag0_num The display line number when the flag interrupt occur, the range is (0~ DSP_VTOTAL-1)

VOP_LITE_INTR_EN

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_mask When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	mmu_irq_intr_en 1'b0: DISABLE 1'b1: ENABLE
14:10	RO	0x0	reserved
9	RW	0x0	dma_frm_fsh_intr_en 1'b0: DISABLE 1'b1: ENABLE
8	RW	0x0	dsp_hold_valid_intr_en 1'b0: DISABLE 1'b1: ENABLE
7	RW	0x0	win1_empty_intr_en 1'b0: DISABLE 1'b1: ENABLE
6	RW	0x0	win0_empty_intr_en 1'b0: DISABLE 1'b1: ENABLE

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Bit	Attr	Reset Value	Description
5	RW	0x0	bus_error_intr_en 1'b0: DISABLE 1'b1: ENABLE
4	RW	0x0	line_flag1_intr_en 1'b0: DISABLE 1'b1: ENABLE
3	RW	0x0	line_flag0_intr_en 1'b0: DISABLE 1'b1: ENABLE
2	RW	0x0	addr_same_intr_en 1'b0: DISABLE 1'b1: ENABLE
1	RW	0x0	fs1_intr_en 1'b0: DISABLE 1'b1: ENABLE
0	RW	0x0	fs0_intr_en 1'b0: DISABLE 1'b1: ENABLE

VOP_LITE_INTR_CLEAR

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15	RW	0x0	mmu_irq_intr_clr 1'b0: DISABLE 1'b1: ENABLE
14:10	RO	0x0	reserved
9	RW	0x0	dma_frm_fsh_intr_clr 1'b0: DISABLE 1'b1: ENABLE
8	W1C	0x0	dsp_hold_valid_intr_clr 1'b0: DISABLE 1'b1: ENABLE
7	W1C	0x0	win1_empty_intr_clr 1'b0: DISABLE 1'b1: ENABLE
6	W1C	0x0	win0_empty_intr_clr 1'b0: DISABLE 1'b1: ENABLE
5	W1C	0x0	bus_error_intr_clr 1'b0: DISABLE 1'b1: ENABLE

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Bit	Attr	Reset Value	Description
4	W1C	0x0	line_flag1_intr_clr 1'b0: DISABLE 1'b1: ENABLE
3	W1C	0x0	line_flag0_intr_clr 1'b0: DISABLE 1'b1: ENABLE
2	W1C	0x0	addr_same_intr_clr 1'b0: DISABLE 1'b1: ENABLE
1	W1C	0x0	fs1_intr_clr 1'b0: DISABLE 1'b1: ENABLE
0	W1C	0x0	fs0_intr_clr 1'b0: DISABLE 1'b1: ENABLE

VOP_LITE_INTR_STATUS

Address: Operational Base + offset (0x003c)

Bit	Attr	Reset Value	Description
31	RW	0x0	mmu_intr_raw_status mmu interrupt raw status
30:26	RO	0x0	reserved
25	RO	0x0	dma_frm_fsh_intr_raw_sts dma finish interrupt raw status
24	RO	0x0	dsp_hold_valid_intr_raw_sts display hold interrupt raw status
23	RO	0x0	win1_empty_intr_raw_sts win1 empty interrupt raw status
22	RO	0x0	win0_empty_intr_raw_sts win0 empty interrupt raw status
21	RO	0x0	bus_error_intr_raw_sts bus error interrupt raw status
20	RO	0x0	line_flag1_intr_raw_sts line flag1 interrupt raw status
19	RO	0x0	line_flag0_intr_raw_sts line flag0 interrupt raw status
18	RW	0x0	addr_same_intr_raw_sts same address interrupt raw status
17	RO	0x0	fs1_intr_raw_sts new frame start interrupt raw status
16	RO	0x0	fs0_intr_raw_sts frame start interrupt raw status
15	RO	0x0	mmu_intr_status mmu interrupt status
14:10	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
9	RW	0x0	dma_frm_fsh_intr_sts dma finish interrupt status
8	RO	0x0	dsp_hold_valid_intr_sts display hold interrupt status
7	RO	0x0	win1_empty_intr_sts win1 empty interrupt status
6	RO	0x0	win0_empty_intr_sts win0 empty interrupt status
5	RO	0x0	bus_error_intr_sts bus error interrupt status
4	RO	0x0	line_flag1_intr_sts line flag1 interrupt status
3	RO	0x0	line_flag0_intr_sts line flag0 interrupt status
2	RW	0x0	addr_same_intr_sts same address interrupt status
1	RW	0x0	fs1_intr_sts new frame start interrupt status
0	RO	0x0	fs0_intr_sts frame start interrupt status

VOP_LITE_WIN1_CTRL0

Address: Operational Base + offset (0x0090)

Bit	Attr	Reset Value	Description
31:14	RO	0x0	reserved
13	RW	0x0	win1_alpha_swap 1'b0: ARGB 1'b1: RGBA
12	RW	0x0	win1_rb_swap 1'b0: RGB 1'b1: BGR
11:10	RO	0x0	reserved
9	RW	0x0	win1_no_outstanding 1'b0: enable 1'b1: disable
8	RW	0x0	win1_interlace_read 1'b0: disable 1'b1: enable
7	RO	0x0	reserved
6:4	RW	0x0	win1_data_fmt 3'b000 : ARGB888 3'b001 : RGB888 3'b010 : RGB565 others: reserved

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Bit	Attr	Reset Value	Description
3:1	RO	0x0	reserved
0	RW	0x0	win1_en 1'b0: Win1 layer disable 1'b1: Win1 layer enable

VOP_LITE_WIN1_CTRL1

Address: Operational Base + offset (0x0094)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:8	RW	0x5	sw_win1_rid win1 axi read id
7:4	RW	0x0	win1_axi_gather_num win1 axi gather_num gather number
3:2	RW	0x0	win1_dma_burst_length 2'b00: burst16 (burst 15 in rgb888 pack mode) 2'b01: burst8 (burst 12 in rgb888 pack mode) 2'b10: burst4 (burst 6 in rgb888 pack mode)
1	RO	0x0	reserved
0	RW	0x0	win1_axi_gather_en 1'b0: disable 1'b1: enable

VOP_LITE_WIN1_VIR

Address: Operational Base + offset (0x0098)

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12:0	RW	0x0000	win1_vir_stride Number of words of Win1 Virtual width ARGB888 : win1_vir_width RGB888 : (win1_vir_width*3/4) + (win1_vir_width%3) RGB565 : ceil(win1_vir_width/2)

VOP_LITE_WIN1_MST

Address: Operational Base + offset (0x00a0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	win1_mst

VOP_LITE_WIN1_DSP_INFO

Address: Operational Base + offset (0x00a4)

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Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved
26:16	RW	0x0ef	dsp_win1_height win1_dsp_height = (win1 dsp vertical size -1)
15:11	RO	0x0	reserved
10:0	RW	0x13f	dsp_win1_width win1_dsp_width = (win1 dsp horizontial size -1)

VOP_LITE_WIN1_DSP_ST

Address: Operational Base + offset (0x00a8)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	dsp_win1_yst win1 y-axis start point
15:12	RO	0x0	reserved
11:0	RW	0x00a	dsp_win1_xst win1 x-axis start point

VOP_LITE_WIN1_COLOR_KEY

Address: Operational Base + offset (0x00ac)

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24	RW	0x0	win1_key_en 1'b0: disable 1'b1: enable
23:0	RW	0x000000	win1_key_color win1 color key

VOP_LITE_WIN1_ALPHA_CTRL

Address: Operational Base + offset (0x00bc)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:4	RW	0x00	win1_alpha_value win1 global alpha value
3	RW	0x0	win1_alpha_sat_mode 1'b0 : alpha value no change 1'b1 : alpha = alpha + alpha[7]
2	RW	0x0	win1_alpha_pre_mul 1'b0 : Non-premultiplied alpha 1'b1 : Premultiplied alpha
1	RW	0x0	win1_alpha_mode 1'b0: user-defined alpha 1'b1: per-pixel alpha
0	RW	0x0	win1_alpha_en 1'b0: disable 1'b1: enable

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VOP_LITE_HWC_CTRL0

Address: Operational Base + offset (0x00e0)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x0	sw_hwc_rid hwc axi read id
3	RW	0x0	hwc_lut_en 1'b0: disable 1'b1: enable *This bit should be "0" when CPU updates the LUT, and should be "1" when hwc LUT mode enable
2	RW	0x0	hwc_load_en 1'b0: disable 1'b1: enable *Setting this bit would reload the Hwc data. It would be auto cleared after reload finish
1	RW	0x0	hwc_size 1'b0: 32x32 1'b1: 64x64
0	RW	0x0	hwc_en 1'b0: Hwc layer disable 1'b1: Hwc layer enable

VOP_LITE_HWC_MST

Address: Operational Base + offset (0x00e8)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	hwc_mst hwc memory start address

VOP_LITE_HWC_DSP_ST

Address: Operational Base + offset (0x00ec)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	dsp_hwc_yst hwc y-axis start point
15:12	RO	0x0	reserved
11:0	RW	0x000	dsp_hwc_xst hwc x-axis start point

VOP_LITE_HWC_ALPHA_CTRL

Address: Operational Base + offset (0x00f0)

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Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:4	RW	0x00	hwc_alpha_value hwc global alpha value
3	RW	0x0	hwc_alpha_sat_mode 1'b0 : alpha value no change 1'b1 : alpha = alpha + alpha[7]
2	RW	0x0	hwc_alpha_pre_mul 1'b0 : Non-premultiplied alpha 1'b1 : Premultiplied alpha
1	RW	0x0	hwc_alpha_mode 1'b0: user-defined alpha 1'b1: per-pixel alpha
0	RW	0x0	hwc_alpha_en 1'b0: disable 1'b1: enable

VOP_LITE_DSP_HTOTAL_HS_END

Address: Operational Base + offset (0x0100)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x14a	dsp_htotal dsp_htotal
15:12	RO	0x0	reserved
11:0	RW	0x00a	dsp_hs_end dsp_hs_end

VOP_LITE_DSP_HACT_ST_END

Address: Operational Base + offset (0x0104)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x00a	dsp_hact_st dsp_hact_st
15:12	RO	0x0	reserved
11:0	RW	0x000	dsp_hact_end dsp_hact_end

VOP_LITE_DSP_VTOTAL_VS_END

Address: Operational Base + offset (0x0108)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x0fa	dsp_vtotal dsp_vtotal
15:12	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
11:0	RW	0x00a	dsp_vs_end dsp_vs_end

VOP_LITE_DSP_VACT_ST_END

Address: Operational Base + offset (0x010c)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x00a	dsp_vact_st dsp_vact_st
15:12	RO	0x0	reserved
11:0	RW	0x0fa	dsp_vact_end dsp_vact_end

VOP_LITE_DSP_VS_ST_END_F1

Address: Operational Base + offset (0x0110)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	dsp_vs_st_f1 Panel display scanning vertical vsync start point of 2nd field (interlace display mode)
15:12	RO	0x0	reserved
11:0	RW	0x000	dsp_vs_end_f1 Panel display scanning vertical vsync end point of 2nd field(interlace display mode)

VOP_LITE_DSP_VACT_ST_END_F1

Address: Operational Base + offset (0x0114)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	dsp_vact_st_f1 Panel display scanning vertical active start point of 2nd field (interlace display mode)
15:12	RO	0x0	reserved
11:0	RW	0x000	dsp_vact_end_f1 Panel display scanning vertical active end point of 2nd field (interlace display mode)

VOP_LITE_BCSH_CTRL

Address: Operational Base + offset (0x0160)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
7	RW	0x0	sw_bcsh_r2y_en 1'b0:bypass 1'b1:enable
6	RW	0x0	sw_bcsh_y2r_en 1'b0:bypass 1'b1:enable
5:4	RW	0x0	sw_bcsh_y2r_csc_mode Color space conversion: 2'b00/11: mpeg 2'b01: hd 2'b10: jpeg
3:2	RW	0x0	video_mode 2'b00 : black 2'b01 : blue 2'b10 : color bar 2'b11 : normal video
1	RW	0x0	sw_bcsh_r2y_csc_mode Color space conversion: 1'b0: BT601 1'b1: BT709
0	RW	0x0	bcsh_en 1'b0 : bcsh bypass 1'b1 : bcsh enable

VOP_LITE_BCSH_COL_BAR

Address: Operational Base + offset (0x0164)

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:16	RW	0x00	color_bar_v v component of color bar
15:8	RW	0x00	color_bar_u u component of color bar
7:0	RW	0x00	color_bar_y y component of color bar

VOP_LITE_BCSH_BCS

Address: Operational Base + offset (0x0168)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:20	RW	0x000	sat_con Saturation*Contrast*256 : 0,1.992*1.992
19:17	RO	0x0	reserved
16:8	RW	0x000	contrast Contrast*256 : 0,1.992

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Bit	Attr	Reset Value	Description
7	RO	0x0	reserved
6:0	RW	0x00	brightness Brightness : -128,127

VOP_LITE_BCSH_H

Address: Operational Base + offset (0x016c)

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24:16	RW	0x000	cos_hue cos_hue
15:9	RO	0x0	reserved
8:0	RW	0x000	sin_hue sin_hue

VOP_LITE_FRC_LOWER01_0

Address: Operational Base + offset (0x0170)

Bit	Attr	Reset Value	Description
31:16	RW	0x1284	lower01_frm1 lower01_frm1
15:0	RW	0x4821	lower01_frm0 lower01_frm0

VOP_LITE_FRC_LOWER01_1

Address: Operational Base + offset (0x0174)

Bit	Attr	Reset Value	Description
31:16	RW	0x2148	lower01_frm3 lower01_frm3
15:0	RW	0x8412	lower01_frm2 lower01_frm2

VOP_LITE_FRC_LOWER10_0

Address: Operational Base + offset (0x0178)

Bit	Attr	Reset Value	Description
31:16	RW	0xa55a	lower10_frm1 lower10_frm1
15:0	RW	0x9696	lower10_frm0 lower10_frm0

VOP_LITE_FRC_LOWER10_1

Address: Operational Base + offset (0x017c)

Bit	Attr	Reset Value	Description
31:16	RW	0x5aa5	lower10_frm3 lower10_frm3
15:0	RW	0x6969	lower10_frm2 lower10_frm2

VOP_LITE_FRC_LOWER11_0

Address: Operational Base + offset (0x0180)

Bit	Attr	Reset Value	Description
31:16	RW	0xdeb7	lower11_frm1 lower11_frm1
15:0	RW	0x7bed	lower11_frm0 lower11_frm0

VOP_LITE_FRC_LOWER11_1

Address: Operational Base + offset (0x0184)

Bit	Attr	Reset Value	Description
31:16	RW	0xed7b	lower11_frm3 lower11_frm3
15:0	RW	0xb7de	lower11_frm2 lower11_frm2

VOP_LITE_MCU_RW_BYPASS_PORT

Address: Operational Base + offset (0x018c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mcu_write_data_bypass mcu write bypass data

VOP_LITE_DBG_REG_SCAN_LINE

Address: Operational Base + offset (0x0190)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RO	0x000	scan_line_num

VOP_LITE_BLANKING_VALUE

Address: Operational Base + offset (0x0194)

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24	RW	0x0	blanking_value_config_en 1'b0 : disable 1'b1 : enable
23:0	RW	0x000000	sw_blanking_value blank value

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VOP_LITE_FLAG_REG_FRM_VALID

Address: Operational Base + offset (0x0198)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	flag_reg_frm_valid valid by frame start

VOP_LITE_FLAG_REG

Address: Operational Base + offset (0x019c)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	flag_reg

VOP_LITE_HWC_LUT_ADDR

Address: Operational Base + offset (0x0600)

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:0	RW	0x000000	hwc_lut_addr Field0000 Description

VOP_LITE_GAMMA_LUT_ADDR

Address: Operational Base + offset (0x0a00)

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:0	RW	0x000000	gamma_lut_addr

VOP_LITE_MMU_DTE_ADDR

Address: Operational Base + offset (0x0f00)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MMU_DTE_ADDR MMU DTE address

VOP_LITE_MMU_STATUS

Address: Operational Base + offset (0x0f04)

Bit	Attr	Reset Value	Description
31:10	RO	0x0	reserved
9:5	RW	0x00	PAGE_FAULT_BUS_ID Index of master reponsible for last page fault
4	RW	0x0	PAGE_FAULT_IS_WRITE The direction of access for last page fault: 0 = Read 1 = Write

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Bit	Attr	Reset Value	Description
3	RW	0x0	MMU_IDLE The MMU is idle when accesses are being translated and there are no unfinished translated accesses
2	RW	0x0	STAIL_ACTIVE MMU stall mode currently enabled. The mode is enabled by command
1	RW	0x0	PAGE_FAULT_ACTIVE MMU page fault mode currently enabled . The mode is enabled by command
0	RW	0x0	PAGING_ENABLED Paging is enabled

VOP_LITE_MMU_COMMAND

Address: Operational Base + offset (0x0f08)

Bit	Attr	Reset Value	Description
31:3	RO	0x0	reserved
2:0	RW	0x0	MMU_CMD MMU_CMD. This can be: 3'b000: MMU_ENABLE_PAGING 3'b001: MMU_DISABLE_PAGING 3'b010: MMU_ENABLE_STALL 3'b011: MMU_DISABLE_STALL 3'b100: MMU_ZAP_CACHE 3'b101: MMU_PAGE_FAULT_DONE 3'b110: MMU_FORCE_RESET

VOP_LITE_MMU_PAGE_FAULT_ADDR

Address: Operational Base + offset (0x0f0c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	PAGE_FAULT_ADDR address of last page fault

VOP_LITE_MMU_ZAP_ONE_LINE

Address: Operational Base + offset (0x0f10)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	MMU_ZAP_ONE_LINE address to be invalidated from the page table cache

VOP_LITE_MMU_INT_RAWSTAT

Address: Operational Base + offset (0x0f14)

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x0	READ_BUS_ERROR read bus error
0	RW	0x0	PAGE_FAULT page fault

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VOP_LITE_MMU_INT_CLEAR

Address: Operational Base + offset (0x0f18)

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x0	READ_BUS_ERROR read bus error
0	RW	0x0	PAGE_FAULT page fault

VOP_LITE_MMU_INT_MASK

Address: Operational Base + offset (0x0f1c)

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x0	READ_BUS_ERROR read bus error
0	RW	0x0	PAGE_FAULT page fault

VOP_LITE_MMU_INT_STATUS

Address: Operational Base + offset (0x0f20)

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x0	READ_BUS_ERROR read bus error
0	RW	0x0	PAGE_FAULT page fault

VOP_LITE_MMU_AUTO_GATING

Address: Operational Base + offset (0x0f24)

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x0	sw_mmu_cfg_mode when it is 1'b0, the mmu reg config will valid after frame start
0	RW	0x0	mmu_auto_gating when it is 1'b1, the mmu will auto gating it self

VOP_LITE_MMU_CFG_DONE

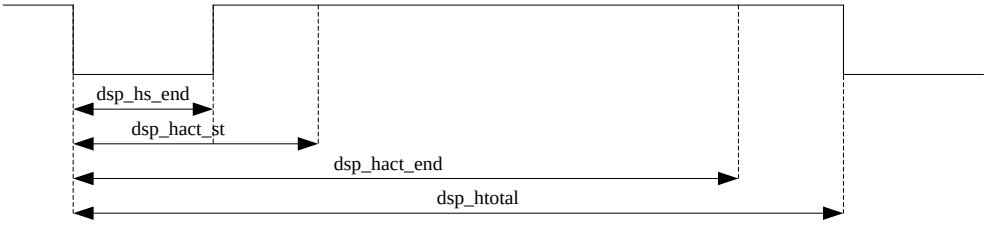
Address: Operational Base + offset (0x0f28)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved

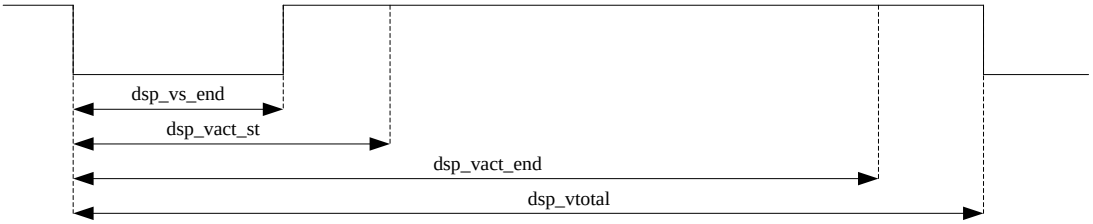
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Bit	Attr	Reset Value	Description
0	RW	0x0	reg_load_mmu_en In the first setting of the register, the new value was saved into the mirror register. When all the mmu register config finish, writing this register to enable the copyright of the mirror register to real register

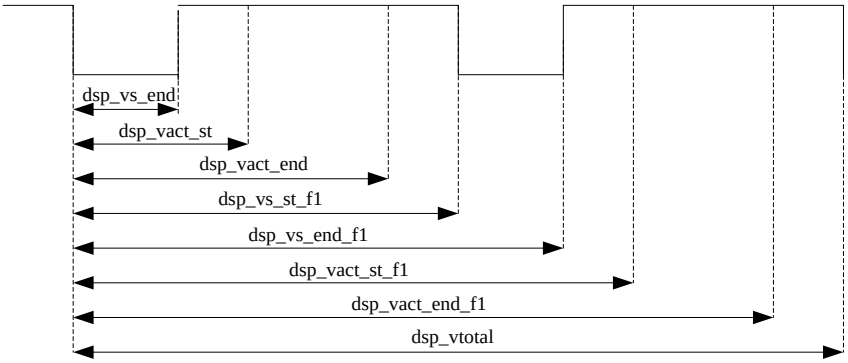
7.5 Timing Diagram



Horizontal timing



Vertical timing(Progressive mode)



Vertical timing(Interlace mode)

Fig. 7-12 VOP RGB interface timing setting

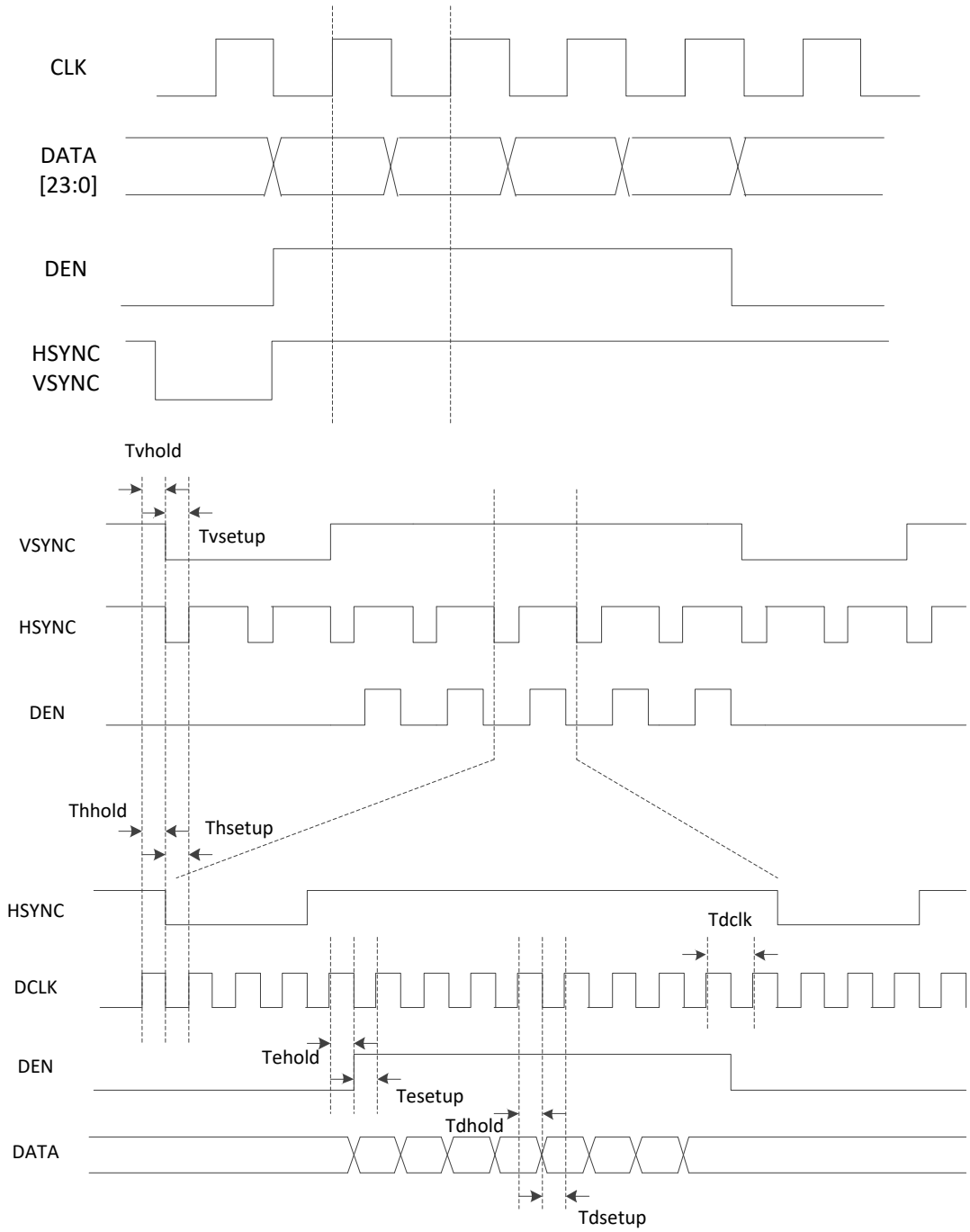


Fig. 7-13 VOP RGB Interface Timing(SDR)

7.6 Interface Description

7.6.1 VOP Outputs

VOP supports RGB, MIPI,output. the MIPI output interface is same as RGB interface . VOP is suitable for different display mode by different usage, which is shown as follows.

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Table 7-2 VOP Control Pins Definition

Display mode	RGB Parallel 24-bit	RGB Parallel 18-bit	RGB Parallel 16-bit
DCLK	DCLK	DCLK	DCLK
VSYNC	VSYNC	VSYNC	VSYNC
HSYNC	HSYNC	HSYNC	HSYNC
DEN	DEN	DEN	DEN
DATA	DATA[23:0]	DATA[17:0]	DATA[15:0]

7.7 Application Notes

7.7.1 DMA transfer mode

There are three DMA transfer modes for loading win0 or win1 frame data determined by following parameters(X=0,1):
dma_burst_length
winX_no_outstanding
winX_gather_en
winX_gather_thres

7.7.2 auto outstanding transfer mode(random transfer)

When winX_no_outstanding is 0, multi-bursts transfer command could be sent out to AXI master interface continuously if the internal memory has enough space to store new data. The continuous random burst number is in the range of 1 to 4, mainly depending on the empty level of internal memory, dma_burst_length, data format and active image width.

2. configured outstanding transfer mode(fixed transfer)

When winX_gather_en is 1, fixed-number of bursts transfer command should be sent out to AXI master interface continuously if the internal memory has enough space to store new data. The fixed-number is determined by winX_gather_thres. Since the internal memory size is limited, there is some restriction for the winX_gather_thres as follows.

Table 7-3 Gather configuration for all format

Gather Threshold	dma_burst_length =2'b00(burst16)	dma_burst_length =2'b01(burst8)	dma_burst_length =2'b10(burst4)
ARGB888 RGB888 RGB565	0,1,2,3	0,1,2,3	0,1,2,3
8BPP	0,1,2,3	0,1,2,3	0,1,2,3

7.7.3 GAMMA LUT

When dsp_lut_en is 0, the DSP LUT data should be refreshed by software. i.e, writing dsp lut data to the internal memory with the start address DSP_LUT_MST. The memory size is 256x24, i.e, lower 24bits valid, and the writing data number is determined by software.

7.7.4 DMA control（QoS/Hurry/Outstanding）

If you want to get higher priority for VOP to access external memory when the frame data is urgent, a QoS and hurry request can be generated and sent out basing on the configured values:
sw_noc_qos_en: SYS_CTRL1[0]
sw_noc_qos_value: SYS_CTRL1[2:1]
sw_noc_hurry_en: SYS_CTRL1[4]
sw_noc_hurry_value: SYS_CTRL1[6:5]
sw_noc_hurry_threshold: SYS_CTRL1[11:8]
sw_axi_max_outstand_en: SYS_CTRL1[12]
sw_axi_max_outstand_num: SYS_CTRL1[20:16]
QoS request for higher bus priority for win1
NOC hurry for higher bus priority for VIO when win0 needs higher priority.
Max Outstanding num is configurable.

7.7.5 Interrupt

VOP interrupt is comprised of 11 interrupt sources:

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- dsp hold interrupt
- frame start0 interrupt
- frame start1 interrupt
- address same interrupt
- line flag0 interrupt
- line flag1 interrupt
- bus error interrupt
- win0 empty interrupt
- win1 empty interrupt
- dma finish interrupt

Every interrupt has independent interrupt enable signal(VOP_INT_EN),interrupt clear signal(VOP_INT_CLR) and interrupt raw status signal (VOP_INT_STATUS).
There is only one interrupt combined with all this interrupt signals to cpu , and it high active.
Dma finish interrupt is used for changing DDR frequency. This interrupt will be asserted when dma finish getting all the Pixel DATA every frame. This interrupt is asserted at the end of the frame.
Address same interrupt will be asserted at this kind of scenario that all the memory start address configured in VOP reg are same compared with the former frame. This interrupt is asserted at the beginning of frame start.
The difference between frame start0 interrupt and frame start1 interrupt is that frame start0 interrupt will be asserted every frame, while the frame start1 interrupt will be masked when all the memory start address are same.

7.7.6 RGB display mode

RGB display mode is used for RGB panel display. It is a continuous frames display mode.

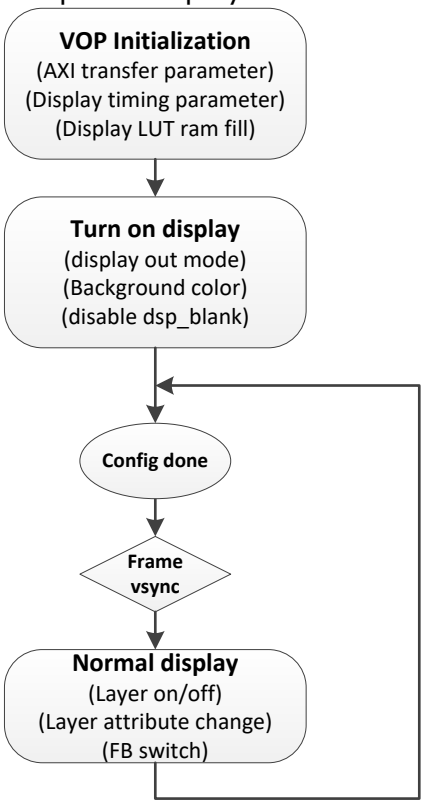


Fig. 7-54 VOP RGB Mode Programming Flow

1.VOP initialization

VOP initialization should be done before turning display on.
First, AXI bus parameter (VOP_SYS_CTRL1) should be set for DMA transfer.
Second, display panel/interface timing should be set for display output. The registers are: VOP_DSP_HTOTAL_HS_END/ VOP_DSP_HACT_ST_END/ VOP_DSP_VTOTAL_HS_END/ VOP_DSP_VACT_ST_END/ VOP_DSP_VS_ST_END_F1/ VOP_DSP_VACT_ST_END_F1

2.Background display

Before normal display, the background display could be turn on.

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First, set display output mode (VOP_DSP_CTRL0/1) according to display device.
Second, disable dsp_blank mode, which would not be enable until frame synchronization.
Finally, writing '1' to "VOP_REG_CFG_DONE" register then all the frame-sync registers will be enable at the beginning of next frame.

3.Normal display

In normal display, all the display layers' attribute could be different according display scenario. So there is a programming loop in this mode.
First, configure all the display layers' attribute registers for the change of image format, location, size, scaling factor, alpha and overlay and so on. Those register would not be enable until frame synchronization.
Finally, write 1 to "VOP_REG_CFG_DONE" register then all the frame-sync registers will be enable at the beginning of next frame.

7.7.7 Immediately control register

There are two type registers in VOP , one is effective immediately, the other is effective by frame sync. Effective immediately registers list as follows, other registers are all effective by frame sync.

Table 7-4 effective immediately register table

register address	description
0x0008	background
0x0018	All display and control signal registers
0xe0~0xf4	Frc configuration bits

7.7.8 Output Polarity Control

There are four channel outputs(RGB HDMI LVDS MIPI , some may not support because SOC do not have the related interface) ,every channel has its own xxx_dclk_en, xxx_dclk_pol, xxx_hsync_pol, xxx_vsync_pol, xxx_den_pol.
The xxx_dclk_en should be set to 1 when output select the xxx channel, and the other channel's xxx_dclk_en should be set to 0 to gate the output clk and data.
When using RGB panel, the dclk should be tied to "0" or "1" in some scenarios.
In this case, you should enable sw_io_pad_clk_sel, to tie dclk to "0". If enable rgb_dclk_pol at the same time, the dclk will tie to "1".

7.7.9 Some special control

- The blanking value of VSYNC could be configured through reg BLANKING_VALUE;
- The current scan line number could be read through reg_addr 0x190;
- There is a FLAG_REG which is readable and writable. This FLAG_REG does not for config function , our software staff may use it in the future. After writing a meaningful 32bit value to FLAG_REG, we can read it before frame valid through reading 0x1fc value, and can get the same value after frame valid reading 0x1f8 value;

7.7.10 RGB PATH

TTL typical configuration is as follows:

```
Word32(GRF_BASE + GRF_VO_CON1) = 0x00040004 ;
Word32(GRF_BASE + GRF_CPIO3A_IOMUX_SEL_L) = 0x11111111 ;
Word32(GRF_BASE + GRF_CPIO3A_IOMUX_SEL_H) = 0x11111111 ;
Word32(GRF_BASE + GRF_CPIO3B_IOMUX_SEL_L) = 0x11111111 ;
Word32(GRF_BASE + GRF_CPIO3B_IOMUX_SEL_H) = 0x11111111 ;
Word32(GRF_BASE + GRF_CPIO3C_IOMUX_SEL_L) = 0x11111111 ;
Word32(GRF_BASE + GRF_CPIO3C_IOMUX_SEL_H) = 0x11111111 ;
Word32(GRF_BASE + GRF_CPIO3D_IOMUX_SEL_L) = 0x11111111 ;
```

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Chapter 8 Raster Graphic Acceleration(RGA)

8.1 Overview

RGA is a separate 2D raster graphic acceleration unit. It accelerates 2D graphics operations, such as image scaling, rotation, BitBLT, alpha blending and fading.
RGA supports the following features:

- **Data format**
  - Input data:
    - Support ARGB/RGB888/RGB565/RGB4444/RGB5551/YUV420/YUV422
    - Support YUV422SP10bit/YUV420SP10bit(YUV-8bits out)
  - Output data:
    - ARGB/RGB888/RGB565/RGB4444/RGB5551/YUV420/YUV422
  - Pixel Format conversion, BT.601/BT.709
  - Dither operation
  - Max resolution: 8192x8192 source, 4096x4096 destination
- **Scaling**
  - Down-scaling: Average filter
  - Up-scaling: Bi-cubic filter(source>2048 would use Bi-linear)
  - Arbitrary non-integer scaling ratio，from 1/8 to 8
- **Rotation**
  - 0, 90, 180, 270 degree rotation
  - x-mirror, y-mirror& rotation operation
- **BitBLT**
  - Block transfer
  - Color palette/Color fill, support with alpha
  - Transparency mode (color keying/stencil test, specified value/value range)
  - Two source BitBLT:
  - A+B=B only BitBLT, A support rotate&scale when B fixed
  - A+B=C second source (B) has same attribute with (C) plus rotation function
- **Alpha Blending**
  - New comprehensive per-pixel alpha(color/alpha channel separately)
  - Fading
  - SRC1(R2Y)&&SRC0(YUV)—alpha->DST(YUV)
- **MMU**
  - 4k/64k page size
  - Four channel: SRC/SRC1/DST/CMD, individual base address and enable control bit
  - TLB pre-fetch

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8.2 Block Diagram

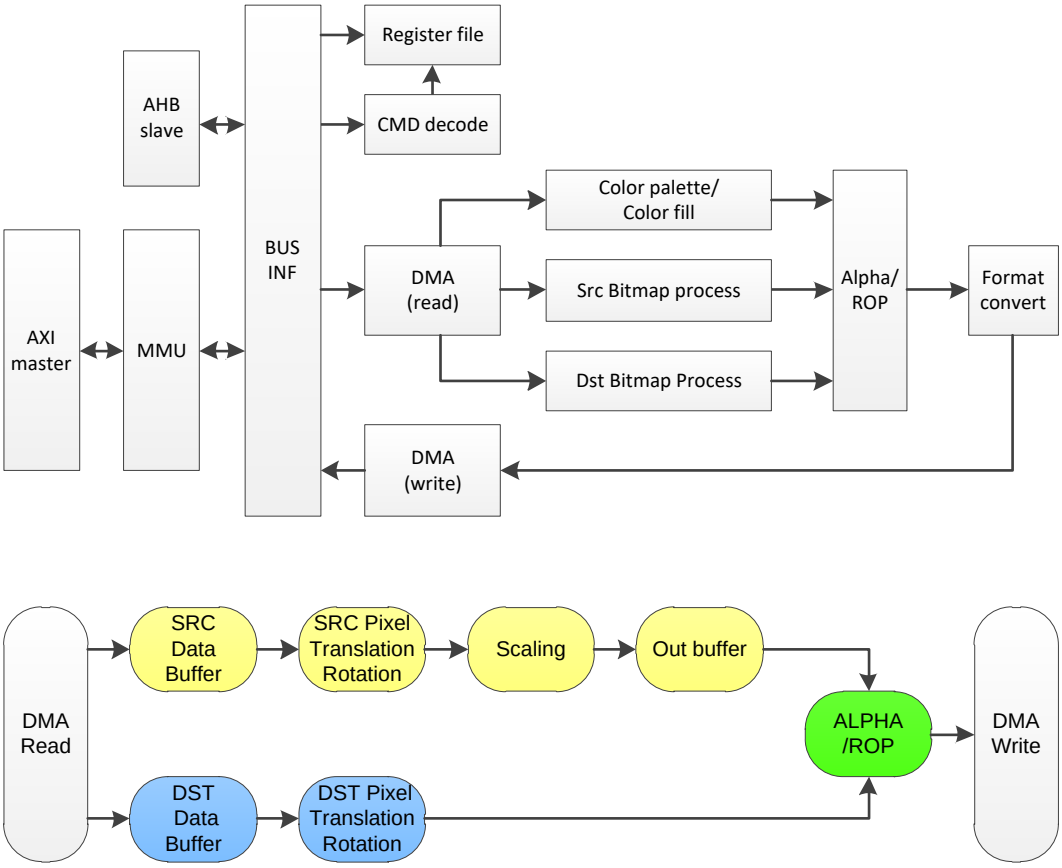


Fig. 8-1RGA Block Diagram

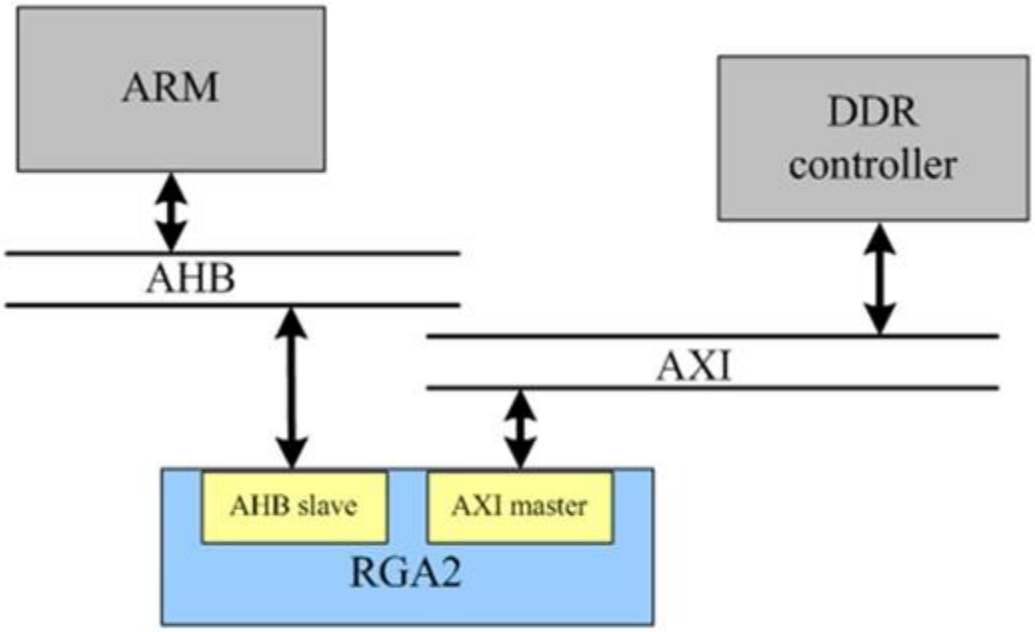


Fig. 8-2 RGA2 in SOC

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8.3 Function Description

8.3.1 Data Format

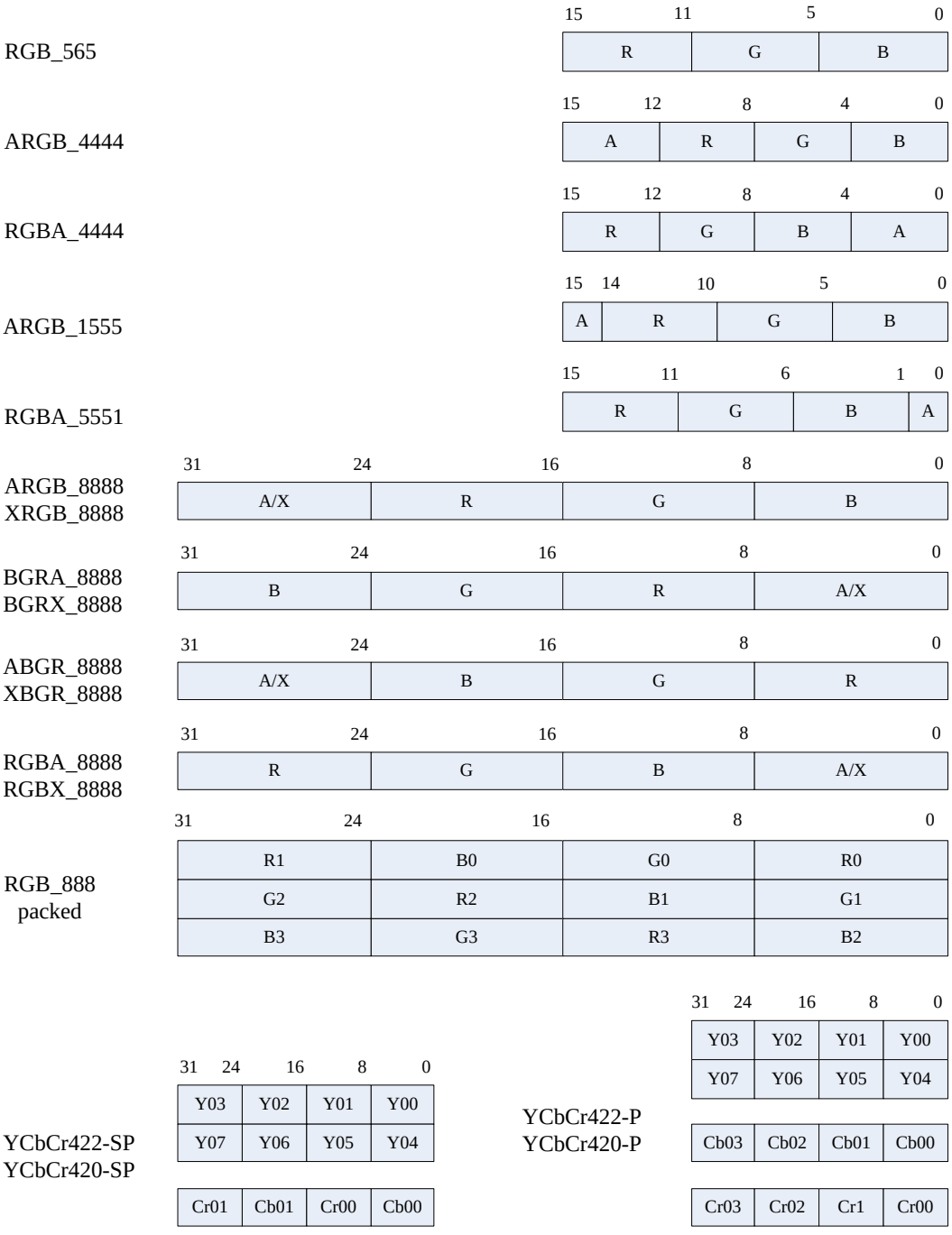


Fig. 8-3 RGA Input Data Format

All input datas (defined by SRC_IN_FMT/DST_IN_FMT) are converted to ABGR8888. The results are converted to the output data format (defined by DST_OUT_FMT).

8.3.2 Dithering

There could have dithering operation for source image when the source image format is not RGB565 and the destination format is RGB565.

The down-dithering is done using Dither Allegro.

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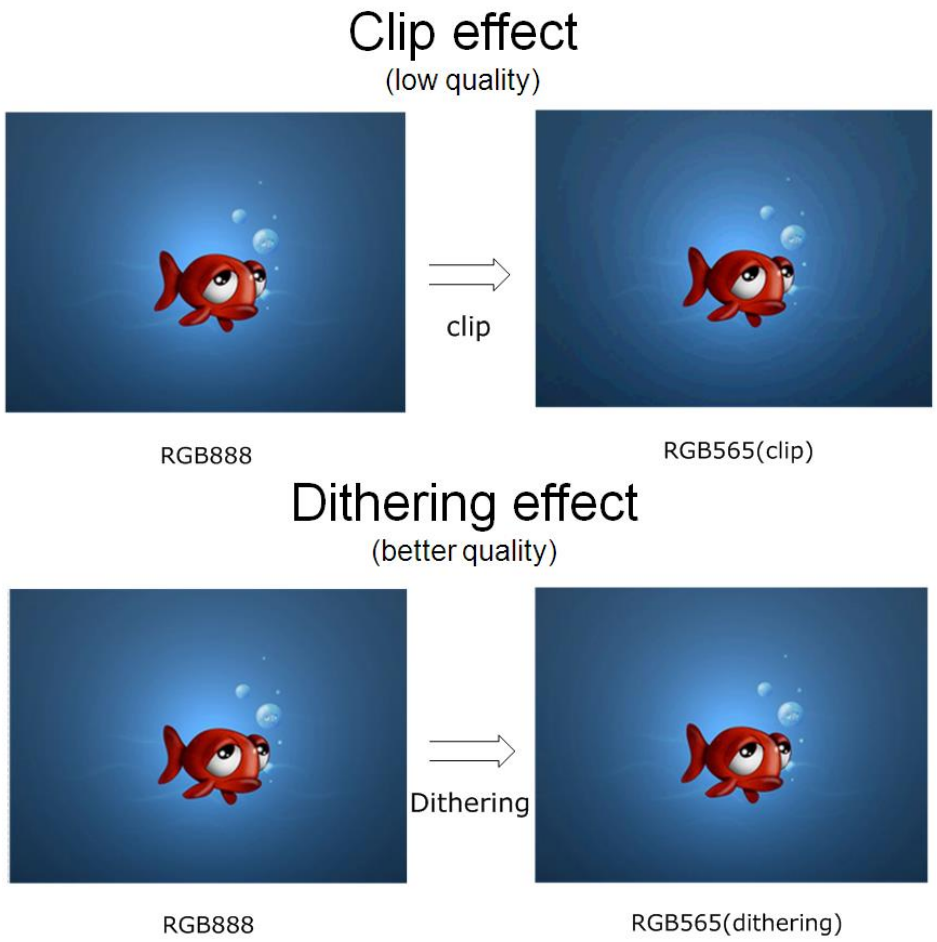
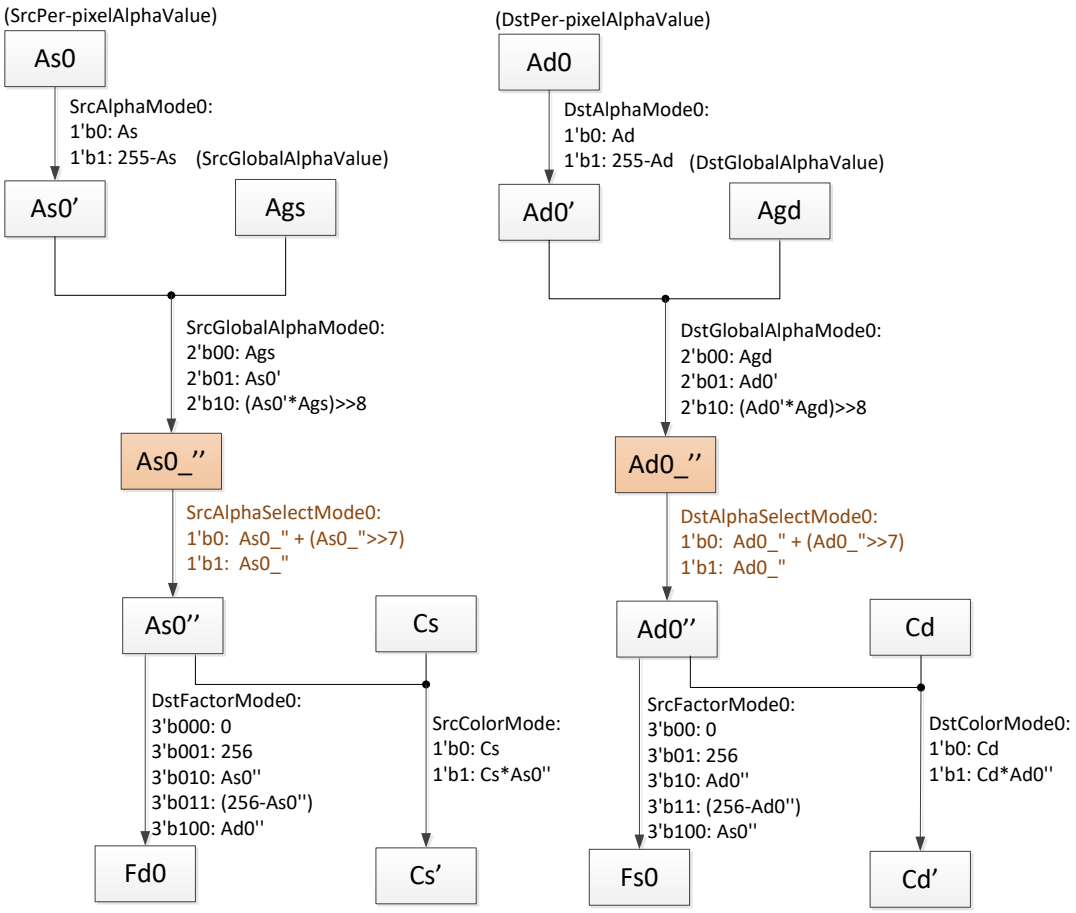


Fig. 8-4 RGA Dither effect

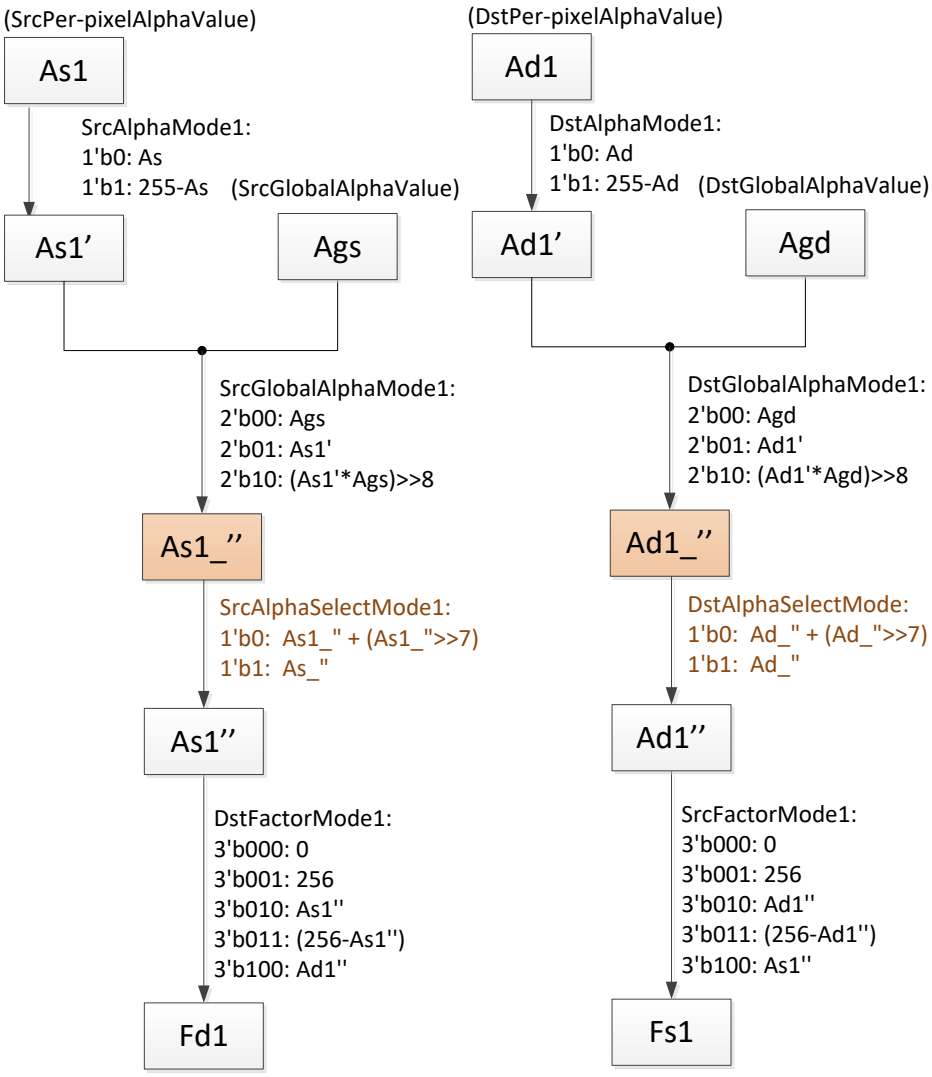
8.3.3 Alpha mode



$$Cd = Fs0 * Cs' + Fd0 * Cd' \quad (1)$$

(Cd – dst color, Fs0 – color src factor0, Cs' – src color', Fd0 – color dst factor0, Cd' – dst color')

Fig. 8-5layer0 alpha blending calculate flow



$$Ad = Fs1 * As1'' + Fd1 * Ad1'' \quad (2)$$

(Ad – dst alpha, Fs1 – alpha src factor1, As1'' – src alpha'', Fd1 – alpha dst factor1, Ad1' – dst alpha'')

Fig. 8-6 layer1 alpha blending calculate flow

8.3.4 Color fill

Two modes of color fill can be done by RGA: solid fill and gradient fill.

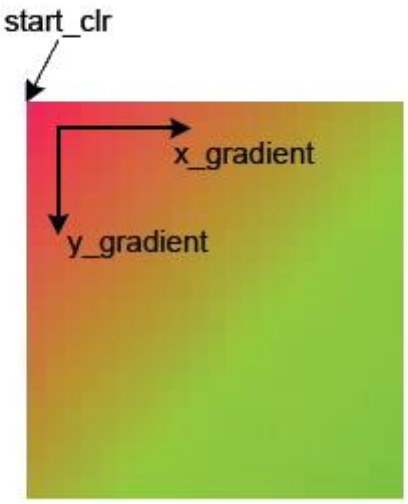


Fig. 8-7 RGA Gradient Fill

Gradient fill using following equations for ARGB calculation of every pixel in different

coordinary.

A_cur = (A_start + x*x_A_gradient) +y*y_A_gradient;
R_cur = (R_start + x*x_R_gradient) +y*y_R_gradient;
G_cur = (G_start + x*x_G_gradient) +y*y_G_gradient;
B_cur = (B_start + x*x_B_gradient) +y*y_B_gradient;

A_start, R_start, G_start, B_start is the ARGB value of start point. There are four pairs of values for horizontal and vertical gradient. Saturation operation could be enabled or disabled if the color overflows 255 or underflows 0.

8.3.5 Raster Operation (ROP)

Raster operation (ROP) is a Booleanoperation between operands, which involve AND, OR, XOR, and NOT operations. For ROP2, operands are P (select pan) and D (Destination bitmap). For ROP3, operands are P (pattern), S (source bitmap) and D (Destination bitmap). For ROP4, operands are P (pattern), S (source bitmap), D (Destination bitmap) and MASK.

Table 8-1 RGAROP Boolean operations

Operator	Meaning
a	Bitwise AND
n	Bitwise NOT (inverse)
o	Bitwise OR
x	Bitwise exclusive OR (XOR)

8.3.6 Scaling

The scaling operation is the imageresizing processingof source image. Scaling is done base on ARGB8888 format.

There are three scale modes: scale down (bilinear, Average); scale up(bilinear, Bi-cubic);

8.4 Register Description

8.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

8.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
RGA2_SYS_CTRL	0x0000	W	0x00000044	RGA system control register
RGA2_CMD_CTRL	0x0004	W	0x00000000	RGA command control register
RGA2_CMD_BASE	0x0008	W	0x12345678	RGA command codes base address register
RGA2_STATUS1	0x000c	W	0x00000000	RGA status register
RGA2_INT	0x0010	W	0x00000000	RGA interrupt register
RGA2_MMU_CTRL0	0x0014	W	0x00000000	Register0000 Description
RGA2_MMU_CMD_BASE	0x0018	W	0x00000000	Register0000 Description
RGA2_STATUS2	0x001c	W	0x00000000	RGA status register
RGA2_WORK_CNT	0x0020	W	0x00000000	
RGA2_VERSION_INFO	0x0028	W	0x00000000	RTL version and FPGA version information
RGA2_PERF_LATENCY_CTRL0	0x0040	W	0x00000024	Only exist when this IP has axi_performance monitor feature
RGA2_PERF_LATENCY_CTRL1	0x0044	W	0x00000021	Only exist when this IP has axi_performance monitor feature
RGA2_PERF_RD_MAX_LATENCY_NUM0	0x0048	W	0x00000000	Only exist when this IP has axi_performance monitor feature

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Name	Offset	Size	Reset Value	Description
RGA2_PERF_RD_LATENCY_SAMP_NUM	0x004c	W	0x00000000	Only exist when this IP has axi_performance monitor feature
RGA2_PERF_RD_LATENCY_ACC_SUM	0x0050	W	0x00000000	Only exist when this IP has axi_performance monitor feature
RGA2_PERF_RD_AXI_TOTAL_BYTE	0x0054	W	0x00000000	Only exist when this IP has axi_performance monitor feature
RGA2_PERF_WR_AXI_TOTAL_BYTE	0x0058	W	0x00000000	Only exist when this IP has axi_performance monitor feature
RGA2_PERF_WORKING_CNT	0x005c	W	0x00000000	Only exist when this IP has axi_performance monitor feature
RGA2_MODE_CTRL	0x0100	W	0x00000000	RGA mode control register
RGA2_SRC_INFO	0x0104	W	0x00000000	RGA source information register
RGA2_SRC_BASE0	0x0108	W	0x00000000	RGA source image Y/RGB base address register
RGA2_SRC_BASE1	0x010c	W	0x00000000	RGA source image Cb/Cbr base address register
RGA2_SRC_BASE2	0x0110	W	0x00000000	RGA source image Cr base address register
RGA2_SRC_BASE3	0x0114	W	0x00000000	RGA source image 1 base address register
RGA2_SRC_VIR_INFO	0x0118	W	0x00000000	RGA source image virtual stride / RGA source image tile number register
RGA2_SRC_ACT_INFO	0x011c	W	0x00000000	RGA source image active width/height register
RGA2_SRC_X_FACTOR	0x0120	W	0x00000000	RGA source image horizontal scaling factor
RGA2_SRC_Y_FACTOR	0x0124	W	0x00000000	RGA source image vertical scaling factor
RGA2_SRC_BG_COLOR	0x0128	W	0x00000000	RGA source image background color
RGA2_SRC_FG_COLOR	0x012c	W	0x00000000	RGA source image foreground color
RGA2_SRC_TR_COLOR0	0x0130	W	0x00000000	RGA source image transparency color min value
RGA2_CP_GR_A	0x0130	W	0x00000000	RGA color gradient fill step register (color fill mode)
RGA2_SRC_TR_COLOR1	0x0134	W	0x00000000	RGA source image transparency color max value
RGA2_CP_GR_B	0x0134	W	0x00000000	RGA color gradient fill step register (color fill mode)
RGA2_DST_INFO	0x0138	W	0x00000000	RGA destination format register

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Name	Offset	Size	Reset Value	Description
RGA2_DST_BASE0	0x013c	W	0x00000000	RGA destination image base address 0 register
RGA2_DST_BASE1	0x0140	W	0x00000000	RGA destination image base address 1 register
RGA2_DST_BASE2	0x0144	W	0x00000000	RGA destination image base address 2 register
RGA2_DST_VIR_INFO	0x0148	W	0x00000000	RGA destination image virtual width/height register
RGA2_DST_ACT_INFO	0x014c	W	0x00000000	RGA destination image active width/height register
RGA2_ALPHA_CTRL0	0x0150	W	0x00000000	Alpha control register 0
RGA2_ALPHA_CTRL1	0x0154	W	0x00000000	Register0000 Description
RGA2_FADING_CTRL	0x0158	W	0x00000000	Fading control register
RGA2_PAT_CON	0x015c	W	0x00000000	Pattern size/offset register
RGA2_ROP_CON0	0x0160	W	0x00000000	ROP code 0 control register
RGA2_CP_GR_G	0x0160	W	0x00000000	RGA color gradient fill step register (color fill mode)
RGA2_ROP_CON1	0x0164	W	0x00000000	ROP code 1 control register
RGA2_CP_GR_R	0x0164	W	0x00000000	RGA color gradient fill step register (color fill mode)
RGA2_MASK_BASE	0x0168	W	0x00000000	RGA mask base address register
RGA2_MMU_CTRL1	0x016c	W	0x00000000	RGA MMU control register 1
RGA2_MMU_SRC_BASE	0x0170	W	0x00000000	RGA source MMU TLB base address
RGA2_MMU_SRC1_BASE	0x0174	W	0x00000000	RGA source1 MMU TLB base address
RGA2_MMU_DST_BASE	0x0178	W	0x00000000	RGA destination MMU TLB base address
RGA2_MMU_ELS_BASE	0x017c	W	0x00000000	RGA ELSE MMU TLB base address

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

8.4.3 Detail Register Description

RGA2_SYS_CTRL

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7	RW	0x0	sw_rst_handsave_p it would save protect-rstn into initial status if long time dead in protect-rstn status. (auto clear into '0')
6	RW	0x1	sw_rst_protect_e protect-rstn mode enable. it would be ensure all axi write/read operation into completion status when sw_cclk_sreset_p or sw_aclk_sreset_p valid

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Bit	Attr	Reset Value	Description
5	RW	0x0	sw_auto_rst it would auto-resetn after one frame finish. 0: disable 1: enable
4	RW	0x0	sw_cclk_sreset_p RGA core clk domain Soft reset, write '1' to this would reset the RGA engine except config registers
3	WO	0x0	sw_aclk_sreset_p RGA aclk domain Soft reset, write '1' to this would reset the RGA engine except config registers
2	WO	0x1	sw_auto_ckg RGA auto clock gating enable bit 0：disable 1：enable
1	WO	0x0	sw_cmd_mode RGA command mode 0：slave mode 1：master mode
0	W1C	0x0	sw_cmd_op_st_p Only used in passive (slave) control mode

RGA2_CMD_CTRL

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12:3	RW	0x000	sw_cmd_incr_num RGA command increment number
2	WO	0x0	sw_cmd_stop RGA command stop mode Command execution would stop after the current graphic operation finish if set this bit to 1
1	WO	0x0	sw_cmd_incr_valid_p RGA command increment valid (Auto cleared) When setting this bit, 1. The total cmd number would increase by the RGA_INCR_CMD_NUM. 2. RGA would continue running if idle
0	RW	0x0	sw_cmd_line_st_p RGA command line fetch start (command line reset) (Auto cleared) When fetch start, the total cmd number would reset to RGA_INCR_CMD_NUM

RGA2_CMD_BASE

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Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:0	RW	0x12345678	sw_cmd_base RGA command codes base address

RGA2_STATUS1

Address: Operational Base + offset (0x000c)

Bit	Attr	Reset Value	Description
31:20	RO	0x000	sw_cmd_total_num RGA command total number
19:8	RO	0x000	sw_cmd_cur_num RGA command current number
7:1	RO	0x00	Reserved Reserved
0	RO	0x0	sw_rga_sta RGA engine status 0: idle 1: working

RGA2_INT

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:11	RO	0x0	reserved
10	RW	0x0	sw_intr_af_e All command finished interrupt enable
9	RW	0x0	sw_intr_mmu_e MMU interrupt enable
8	RW	0x0	sw_intr_err_e Error interrupt enable
7	WO	0x0	sw_intr_cf_clr Current command finished interrupt clear
6	WO	0x0	sw_intr_af_clr All command finished interrupt clear
5	WO	0x0	sw_intr_mmu_clr MMU interrupt clear
4	WO	0x0	sw_intr_err_clr Error interrupt clear
3	RO	0x0	sw_intr_cf Current command finished interrupt flag
2	RO	0x0	sw_intr_af All command finished interrupt flag
1	RO	0x0	sw_intr_mmu MMU interrupt
0	RO	0x0	sw_intr_err Error interrupt flag

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RGA2_MMU_CTRL0

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:11	RW	0x000000	Reserved Reserved
10:9	RW	0x0	sw_els_ch_priority sw_els_ch_priority
8:7	RW	0x0	sw_dst_ch_priority sw_dst_ch_priority
6:5	RW	0x0	sw_src1_ch_priority sw_src1_ch_priority
4:3	RW	0x0	sw_src_ch_priority sw_src_ch_priority
2	RW	0x0	sw_cmd_mmu_flush RGA CMD channel MMU TLB flush: Set 1 to this bit to flush MMU TLB, auto clear
1	RW	0x0	sw_cmd_mmu_en RGA CMD channel MMU enable 0: disable 1: enable
0	RW	0x0	sw_mmu_page_size RGA MMU Page table size 0: 4KB page 1: 64KB page

RGA2_MMU_CMD_BASE

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RW	0x0000000	sw_mmu_cmd_base RGA command MMU TLB base address (word)

RGA2_STATUS2

Address: Operational Base + offset (0x001c)

Bit	Attr	Reset Value	Description
31:13	RO	0x00000	Reserved
12:11	RO	0x0	rpp_mkram_rready rpp_mkram_rready
10:6	RO	0x00	dstrpp_outbuf_rready dstrpp_outbuf_rready
5:2	RO	0x0	srcrpp_outbuf_rready dstrpp_outbuf_rready

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Bit	Attr	Reset Value	Description
1	RO	0x0	bus_error
0	RO	0x0	rpp_error

RGA2_WORK_CNT

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:27	RW	0x00	Reserved
26:0	RO	0x0000000	sw_work_cnt RGA total working counter

RGA2_VERSION_INFO

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	major used for IP structure version infomation
23:20	RW	0x0	minor big feature change under same structure
19:0	RW	0x00000	svnbuild rtl current svn number

RGA2_PERF_LATENCY_CTRL0

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:8	RW	0x000	sw_rd_latency_thr
7:4	RW	0x2	sw_rd_latency_id
3	RW	0x0	sw_axi_cnt_type sw_axi_cnt_type
2	RW	0x1	sw_axi_perf_frm_type 1'b0: clear by software configuration 1'b1: clear by frame end
1	RW	0x0	sw_axi_perf_clr_e 1'b0: software clear disable 1'b1: software clear enalbe
0	RW	0x0	sw_axi_perf_work_e 1'b0: disable 1'b1: enable

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RGA2_PERF_LATENCY_CTRL1

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:8	RW	0x0	sw_aw_count_id sw_aw_count_id
7:4	RW	0x2	sw_ar_count_id sw_ar_count_id
3	RW	0x0	sw_aw_cnt_id_type sw_aw_cnt_id_type
2	RW	0x0	sw_ar_cnt_id_type sw_ar_cnt_id_type
1:0	RW	0x1	sw_addr_align_type sw_addr_align_type

RGA2_PERF_RD_MAX_LATENCY_NUM0

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RO	0x0000	rd_max_latency_num_ch0

RGA2_PERF_RD_LATENCY_SAMP_NUM

Address: Operational Base + offset (0x004c)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rd_latency_thr_num_ch0

RGA2_PERF_RD_LATENCY_ACC_SUM

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rd_latency_acc_sum

RGA2_PERF_RD_AXI_TOTAL_BYTE

Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	perf_rd_axi_total_byte perf_rd_axi_total_byte

RGA2_PERF_WR_AXI_TOTAL_BYTE

Address: Operational Base + offset (0x0058)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	perf_wr_axi_total_byte perf_wr_axi_total_byte

RGA2_PERF_WORKING_CNT

Address: Operational Base + offset (0x005c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	perf_working_cnt perf_working_cnt

RGA2_MODE_CTRL

Address: Operational Base + offset (0x0100)

Bit	Attr	Reset Value	Description
31:8	RW	0x000000	Reserved Reserved
7	RW	0x0	sw_intr_cf_e Current command finished interrupt enable
6	RW	0x0	sw_gradient_sat Gradient saturation calculation mode 0:clip 1:not-clip
5	RW	0x0	sw_alpha_zero_key ARGB888 alpha zero key mode 0x000000 would be changed to 0x000100(RGB888)/0x0020(RGB565)for ARGB888 to RGBX/RGB565 color key 0: disable 1: enable
4	RW	0x0	sw_cf_rop4_pat Color fill/ROP4 pattern 0: solid color 1: pattern color
3	RW	0x0	sw_bb_mode Bitblt mode 0: SRC + DST => DST 1: SRC + SRC1 => DST
2:0	RW	0x0	sw_render_mode RGA 2D render mode 000: Bitblt 001: Color palette 010: Rectangle fill 011: Update palette LUT/pattern ram

RGA2_SRC_INFO

Address: Operational Base + offset (0x0104)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved

Bit	Attr	Reset Value	Description
28	RW	0x0	sw_src_yuv10_round_e this bit valid when RGA support yuv 10bit picture input 0: yuv 10bit to 8bit round disable 1: yuv 10bit to 8bit round enable
27	RW	0x0	sw_src_yuv10_e this bit valid when RGA support yuv 10bit picture input 0: yuv 10bit disable 1: yuv 10bit enalbe
26	RW	0x0	sw_vsp_mode 0:by-cubic 1:bi-linear
25:24	RW	0x0	sw_bic_coe_sel SRC bicubic scaling coefficient select 00: CATROM 01: MITCHELL 10: HERMITE 11: B-SPLINE
23	RW	0x0	sw_src_dither_up SRC dither up enable 0:disable 1:enable
22:19	RW	0x0	sw_src_trans_e Source transparency enable bits [3]: A value stencil test enable bit [2]: B value stencil test enable bit [1]: G value stencil test enable bit [0]: R value stencil test enable bit
18	RW	0x0	sw_src_trans_mode Source transparency mode 0: normal stencil test (color key) 1: inverted stencil test
17:16	RW	0x0	sw_src_vscl_mode SRC vertical scaling mode 00：no scaling 01: down-scaling 10: up-scaling
15:14	RW	0x0	sw_src_hscl_mode SRC horizontal scaling mode 00：no scaling 01: down-scaling 10: up-scaling

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Bit	Attr	Reset Value	Description
13:12	RW	0x0	sw_src_mir_mode SRC mirror mode 00: no mirror 01: x mirror 10: y mirror 11: x mirror + y mirror
11:10	RW	0x0	sw_src_rot_mode SRC rotation mode 00: 0 degree 01: 90 degree 10: 180 degree 11: 270 degree
9:8	RW	0x0	sw_src_csc_mode Source bitmap YUV2RGB conversion mode 00: bypass 01: BT.601-range0 10: BT.601-range1 11: BT.709-range0
7	RW	0x0	sw_cp_endian Source Color palette endian swap 0: big endian 1: little endian
6	RW	0x0	sw_src_uvswap Source Cb-Cr swap 0: CrCb 1: CbCr
5	RW	0x0	sw_src_alpha_swap Source bitmap data alpha swap 0: ABGR 1: BGRA
4	RW	0x0	sw_src_rbswap Source bitmap data RB swap 0: BGR 1: RGB

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Bit	Attr	Reset Value	Description
3:0	RW	0x0	sw_src_fmt Source bitmap data format 0000: ABGR888 0001: XBGR888 0010: BGR packed 0100: RGB565 0101: ARGB1555 0110: ARGB4444 1000: YUV422SP 1001: YUV422P 1010: YUV420SP 1011: YUV420P 1100: 1BPP (color palette) 1101: 2BPP (color palette) 1110: 4BPP (color palette) 1111: 8BPP (color palette)

RGA2_SRC_BASE0

Address: Operational Base + offset (0x0108)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_src_base0 source image Y/RGB base address

RGA2_SRC_BASE1

Address: Operational Base + offset (0x010c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_src_base1 source image Cb base address (YUV422/420-P) source image Cb/Cr base address (YU,V422/420-SP)

RGA2_SRC_BASE2

Address: Operational Base + offset (0x0110)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	sw_src_base2 source image Cr base address (YUV422/420-P)

RGA2_SRC_BASE3

Address: Operational Base + offset (0x0114)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	sw_src_base3 source image 1 RGB base address (source bitblt mode1)

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RGA2_SRC_VIR_INFO

Address: Operational Base + offset (0x0118)

Bit	Attr	Reset Value	Description
31:26	RW	0x00	Reserved
25:16	RW	0x000	sw_mask_vir_stride mask image virtual stride (words)
15	RW	0x0	Reserved Reserved
14:0	RW	0x0000	sw_src_vir_stride src image virtual stride (words)

RGA2_SRC_ACT_INFO

Address: Operational Base + offset (0x011c)

Bit	Attr	Reset Value	Description
31:29	RW	0x0	Reserved2 Reserved
28:16	RW	0x0000	sw_src_act_height source image active height
15:13	RW	0x0	Reserved1 Reserved
12:0	RW	0x0000	sw_src_act_width source image active width

RGA2_SRC_X_FACTOR

Address: Operational Base + offset (0x0120)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_src_hsp_factor Source image horizontal up-scaling factor =(DST_ACT_WIDTH/SRC_ACT_WIDTH) * 65536
15:0	RW	0x0000	sw_src_hsd_factor Source image horizontal down-scaling factor =(SRC_ACT_WIDTH/DST_ACT_WIDTH) * 65536

RGA2_SRC_Y_FACTOR

Address: Operational Base + offset (0x0124)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_src_vsp_factor Source image vertical up-scaling factor (DST_ACT_HEIGHT/SRC_ACT_HEIGHT) * 65536
15:0	RW	0x0000	sw_src_vsd_factor Source image vertical down-scaling factor (SRC_ACT_HEIGHT/DST_ACT_HEIGHT) * 65536

RGA2_SRC_BG_COLOR

Address: Operational Base + offset (0x0128)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_src_bg_color Source image background color ("0" bit color for mono expansion.)

RGA2_SRC_FG_COLOR

Address: Operational Base + offset (0x012c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_src_fg_color Source image foreground color ("1" bit color for mono expansion.) Color fill color, Pan color

RGA2_SRC_TR_COLOR0

Address: Operational Base + offset (0x0130)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_src_trans_amin source image transparency color A min value
23:16	RW	0x00	sw_src_trans_bmin source image transparency color B min value
15:8	RW	0x00	sw_src_trans_gmin source image transparency color G min value
7:0	RW	0x00	sw_src_trans_rmin source image transparency color R min value

RGA2_CP_GR_A

Address: Operational Base + offset (0x0130)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_gradient_y_a Y gradient value of Alpha (signed 8.8)
15:0	RW	0x0000	sw_gradient_x_a X gradient value of Alpha (signed 8.8)

RGA2_SRC_TR_COLOR1

Address: Operational Base + offset (0x0134)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_src_trans_amax source image transparency color A max value
23:16	RW	0x00	sw_src_trans_bmax source image transparency color B max value
15:8	RW	0x00	sw_src_trans_gmax source image transparency color G max value
7:0	RW	0x00	sw_src_trans_rmax source image transparency color R max value

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RGA2_CP_GR_B

Address: Operational Base + offset (0x0134)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_gradient_y_b Y gradient value of Blue (signed 8.8)
15:0	RW	0x0000	sw_gradient_x_b X gradient value of Blue (signed 8.8)

RGA2_DST_INFO

Address: Operational Base + offset (0x0138)

Bit	Attr	Reset Value	Description
31:22	RO	0x0	reserved
21	RW	0x0	sw_src1_csc_clip src1 read BGR2YUV Clip mode(from 0~255 clip to 36~235) 1: clip enable; 0: unclip
20:19	RW	0x0	sw_src1_csc_mode sw_dst_csc_mode SRC1 read bitmap RGB2YUV conversion mode 00: Bypass 01: BT.601-range0 10: BT.601-range1 11: BT.709-range0
18	RW	0x0	sw_dst_csc_clip dst write BGR2YUV Clip mode(from 0~255 clip to 36~235) 1: clip enable; 0: unclip
17:16	RW	0x0	sw_dst_csc_mode sw_dst_csc_mode DST write bitmap RGB2YUV conversion mode 00: Bypass 01: BT.601-range0 10: BT.601-range1 11: BT.709-range0
15:14	RW	0x0	sw_dither_mode sw_dither_mode DST dither down bit mode 00: 888 to 666 01: 888 to 565 10: 888 to 555 11: 888 to 444
13	RW	0x0	sw_dither_down sw_dither_down DST dither down enable 0:disable 1:enable

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Bit	Attr	Reset Value	Description
12	RW	0x0	sw_src1_dither_up sw_src1_dither_up DST/SRC1 dither up enable 0:disable 1:enable
11	RW	0x0	sw_src1_alpha_swap sw_src1_alpha_swap Source 1 bitmap data alpha swap 0: ABGR 1: BGRA
10	RW	0x0	sw_src1_rbswap sw_src1_rbswap Source 1 bitmap data RB swap 0: BGR 1: RGB
9:7	RW	0x0	sw_src1_fmt sw_src1_fmt Source 1 bitmap data format 000: ABGR888 001: XBGR888 010: BGR packed 100: RGB565 101: ARGB1555 110: ARGB4444
6	RW	0x0	sw_dst_uvswap Destination Cb-Cr swap 0: CrCb 1: CbCr
5	RW	0x0	sw_dst_alpha_swap Destination bitmap data alpha swap 0: ABGR 1: BGRA
4	RW	0x0	sw_dst_rbswap Destination bitmap data RB swap 0: BGR 1: RGB

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Bit	Attr	Reset Value	Description
3:0	RW	0x0	sw_dst_fmt Destination bitmap data format 0000: ABGR888 0001: XBGR888 0010: BGR packed 0100: RGB565 0101: ARGB1555 0110: ARGB4444 1000: YUV422SP 1001: YUV422P 1010: YUV420SP 1011: YUV420P If RGA has yuyv output format feature: 1100: YVYU422(U, LSB) 1101: YVYU420(U, LSB) 1110: VYUY422(Y, LSB) 1111: VYUY420(Y, LSB)

RGA2_DST_BASE0

Address: Operational Base + offset (0x013c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_dst_base0 destination image Y/RGB base address

RGA2_DST_BASE1

Address: Operational Base + offset (0x0140)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_dst_base1 destination image Cb/CbCr base address

RGA2_DST_BASE2

Address: Operational Base + offset (0x0144)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_dst_base2 destination image Cr base address

RGA2_DST_VIR_INFO

Address: Operational Base + offset (0x0148)

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Bit	Attr	Reset Value	Description
31:28	RW	0x0	Reserved2 Reserved
27:16	RW	0x000	sw_src1_vir_stride source image 1 virtual stride (words)
15:12	RW	0x0	Reserved1 Reserved
11:0	RW	0x000	sw_dst_vir_stride destination image virtual stride(words)

RGA2_DST_ACT_INFO

Address: Operational Base + offset (0x014c)

Bit	Attr	Reset Value	Description
31:28	RW	0x0	Reserved2 Reserved
27:16	RW	0x000	sw_dst_act_height Destination image active height
15:12	RW	0x0	Reserved1 Reserved
11:0	RW	0x000	sw_dst_act_width Destination image active width

RGA2_ALPHA_CTRL0

Address: Operational Base + offset (0x0150)

Bit	Attr	Reset Value	Description
31:21	RW	0x000	Reserved Reserved
20	RW	0x0	sw_mask_endian sw_mask_endian ROP4 mask endian swap 0: big endian 1: little endian
19:12	RW	0x00	sw_dst_global_alpha global alpha value of DST(Agd)
11:4	RW	0x00	sw_src_global_alpha global alpha value of SRC(Ags) fading value in fading mod
3:2	RW	0x0	sw_rop_mode ROP mode select 00: ROP 2 01: ROP 3 10: ROP 4

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Bit	Attr	Reset Value	Description
1	RW	0x0	sw_alpha_rop_sel Alpha or ROP select 0: alpha 1: ROP
0	RW	0x0	sw_alpha_rop_e Alpha or ROP enable 0: disable 1: enable

RGA2_ALPHA_CTRL1

Address: Operational Base + offset (0x0154)

Bit	Attr	Reset Value	Description
31:30	RW	0x0	Reserved Reserved
29	RW	0x0	sw_src_alpha_m1 Src Transparent/opaque of alpha channel (As1') 0: As 1: 255-As
28	RW	0x0	sw_dst_alpha_m1 Dst Transparent/opaque of alpha channel (Ad1') 0: Ad 1: 255-Ad
27:26	RW	0x0	sw_src_blend_m1 Alpha src blend mode select of alpha channel (As1_'') 00: Ags 01: As1' 10: (As1'*Ags)>>8 11: reserved
25:24	RW	0x0	sw_dst_blend_m1 Alpha dst blend mode select of alpha channel(Ad1_'') 00: Agd 01: Ad1' 10: (Ad1'*Agd)>>8 11: reserved
23	RW	0x0	sw_src_alpha_cal_m1 Alpha src calculate mode of alpha channel(As1'') 0: As1''= As1_''+ (As1_''>>7) 1: As1''= As1 _''
22	RW	0x0	sw_dst_alpha_cal_m1 Alpha dst calculate mode of alpha channel(Ad1'') 0: Ad1''= Ad1_'' + (Ad1_''>>7) 1: Ad1''= Ad1_''

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Bit	Attr	Reset Value	Description
21:19	RW	0x0	w_src_factor_m1 Src factore mode of alpha channel(Fs1) 000: 0 001: 256 010: Ad1’’ 011: 256-Ad1’’ 100: As1’’
18:16	RW	0x0	sw_dst_factor_m1 Dst factore mode of alpha channel(Fd1) 000: 0 001: 256 010: As1’’ 011: 256-As1’’ 100: Ad1’’
15	RW	0x0	sw_src_alpha_m0 Src Transparent/opaque of color channel (As0’) 0: As 1: 255-As
14	RW	0x0	sw_dst_alpha_m0 Dst Transparent/opaque of color channel (Ad0’) 0: Ad 1: 255-Ad
13:12	RW	0x0	sw_src_blend_m0 Alpha src blend mode select of color channel (As0_’’) 00: Ags 01: As0’ 10: (As0’*Ags)>>8 11: reserved
11:10	RW	0x0	sw_dst_blend_m0 Alpha dst blend mode select of color channel(Ad0_’’) 00: Agd 01: Ad0’ 10: (Ad0’*Agd)>>8 11: reserved
9	RW	0x0	sw_src_alpha_cal_m0 Alpha src calculate mode of color channel(As0’’) 0: As0’’= As0_’’+ (As0_’’>>7) 1: As0’’= As0 _’’
8	RW	0x0	sw_dst_alpha_cal_m0 Alpha dst calculate mode of color channel(Ad0’’) 0: Ad0’’= Ad0_’’ + (Ad0_’’>>7) 1: Ad0’’= Ad0_’’

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Bit	Attr	Reset Value	Description
7:5	RW	0x0	sw_src_factor_m0 Src factore mode of color channel(Fs0) 000: 0 001: 256 010: Ad0'' 011: 256-Ad0'' 100: As0''
4:2	RW	0x0	sw_dst_factor_m0 Dst factore mode of color channel(Fd0) 000: 0 001: 256 010: As0'' 011: 256-As0'' 100: Ad0''
1	RW	0x0	sw_src_color_m0 SRC color select(Cs') 0: Cs 1: Cs * As0''
0	RW	0x0	sw_dst_color_m0 SRC color select(Cd') 0: Cd 1: Cd * Ad0''

RGA2_FADING_CTRL

Address: Operational Base + offset (0x0158)

Bit	Attr	Reset Value	Description
31:25	RW	0x00	Reserved Reserved
24	RW	0x0	sw_fading_en Fading enable
23:16	RW	0x00	sw_fading_offset_b Fading offset B value
15:8	RW	0x00	sw_fading_offset_g Fading offset G value (Pattern total number when pattern loading)
7:0	RW	0x00	sw_fading_offset_r Fading offset R value (Start point of pattern ram in pattern mode)

RGA2_PAT_CON

Address: Operational Base + offset (0x015c)

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Bit	Attr	Reset Value	Description
31:24	RW	0x00	sw_pat_offset_y Pattern y offset
23:16	RW	0x00	sw_pat_offset_x Pattern x offset
15:8	RW	0x00	sw_pat_height Pattern height
7:0	RW	0x00	sw_pat_width Pattern width

RGA2_ROP_CON0

Address: Operational Base + offset (0x0160)

Bit	Attr	Reset Value	Description
31:25	RW	0x00	Reserved Reserved
24:0	RW	0x0000000	sw_rop3_code0 Rop3 code 0 control bits

RGA2_CP_GR_G

Address: Operational Base + offset (0x0160)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_gradient_y_g Y gradient value of Green (signed 8.8)
15:0	RW	0x0000	sw_gradient_x_g X gradient value of Green (signed 8.8)

RGA2_ROP_CON1

Address: Operational Base + offset (0x0164)

Bit	Attr	Reset Value	Description
31:25	RW	0x00	Reserved Reserved
24:0	RW	0x0000000	sw_rop3_code1 Rop3 code 1 control bits

RGA2_CP_GR_R

Address: Operational Base + offset (0x0164)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	sw_gradient_y_r Y gradient value of Red(signed 8.8)
15:0	RW	0x0000	sw_gradient_x_r X gradient value of Red(signed 8.8)

RGA2_MASK_BASE

Address: Operational Base + offset (0x0168)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sw_mask_base mask base address in ROP4 mode LUT/ pattern load base address

RGA2_MMU_CTRL1

Address: Operational Base + offset (0x016c)

Bit	Attr	Reset Value	Description
31:14	RW	0x00000	Reserved Reserved
13	RW	0x0	sw_els_mmu_flush RGA ELSE channel MMU TLB flush: Set 1 to this bit to flush MMU TLB, auto clear
12	RW	0x0	sw_els_mmu_en RGA ELSE channel MMU enable 0: disable 1: enable
11	RW	0x0	sw_dst_mmu_prefetch_dir sw_dst_mmu_prefetch_dir 0:forward 1:backward
10	RW	0x0	sw_dst_mmu_prefetch_en sw_dst_mmu_prefetch_en 0:disable 1:enable
9	RW	0x0	sw_dst_mmu_flush sw_dst_mmu_flush RGA DST channel MMU TLB flush: Set 1 to this bit to flush MMU TLB, auto clear
8	RW	0x0	sw_dst_mmu_en sw_dst_mmu_en RGA DST channel MMU enable 0: disable 1: enable
7	RW	0x0	sw_src1_mmu_prefetch_dir sw_src1_mmu_prefetch_dir 0:forward 1:backward
6	RW	0x0	sw_src1_mmu_prefetch_en sw_src1_mmu_prefetch_en 0:disable 1:enable
5	RW	0x0	sw_src1_mmu_flush sw_src1_mmu_flush RGA SRC1 channel MMU TLB flush: Set 1 to this bit to flush MMU TLB, auto clear

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Bit	Attr	Reset Value	Description
4	RW	0x0	sw_src1_mmu_en sw_src1_mmu_en RGA SRC1 channel MMU enable 0: disable 1: enable
3	RW	0x0	sw_src_mmu_prefetch_dir sw_src_mmu_prefetch_dir 0:forward 1:backward
2	RW	0x0	sw_src_mmu_prefetch_en sw_src_mmu_prefetch_en 0:disable 1:enable
1	RW	0x0	sw_src_mmu_flush RGA SRC channel MMU TLB flush: Set 1 to this bit to flush MMU TLB, auto clear
0	RW	0x0	sw_src_mmu_en RGA SRC channel MMU enable 0: disable 1: enable

RGA2_MMU_SRC_BASE

Address: Operational Base + offset (0x0170)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RW	0x0000000	sw_mmu_src_base RGA source MMU TLB base address (128-bit)

RGA2_MMU_SRC1_BASE

Address: Operational Base + offset (0x0174)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RW	0x0000000	sw_mmu_src1_base RGA source1 MMU TLB base address (128-bit)

RGA2_MMU_DST_BASE

Address: Operational Base + offset (0x0178)

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RW	0x0000000	sw_mmu_dst_base RGA destination MMU TLB base address (128-bit)

RGA2_MMU_ELS_BASE

Address: Operational Base + offset (0x017c)

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Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:0	RW	0x0000000	sw_mmu_els_base RGA destination MMU TLB base address (128-bit)

8.5 Application Notes

8.5.1 Register Partition

There are two types of register in RGA. The first 8 registers (0x0 - 0x1C) are general registers for system configuration including command mode, command parameter, RGA status, general interrupts. The other registers (from 0x100) are command registers for command codes.

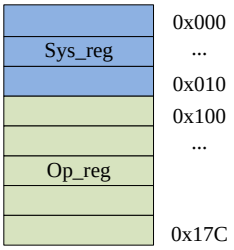


Fig. 8-8 RGAsoftware main register-region

8.5.2 Command Modes

RGA has two command modes: slave mode and master mode. In salve mode (RGA_SYS_CTRL[1] = 1'b0), 2D graphic command only could be run one by one. CPU set all the command registers in RGA and then start RGA running by setting RGA_SYS_CTRL[0] to '1'. In master mode (RGA_SYS_CTRL[1] = 1'b1), 2D graphic commands could be run sequentially. After setting command's number to RGA_CMD_CTRL[12:3], writing '1' to RGA_CMD_CTRL[0] will start the command fetch, then Internal command DMA fetch commands from external command line.
Command line is a collection of several command codes with continuous address. At the first start, the command start address (RGA_CMD_ADDR) and command number (RGA_CMD_CTRL[12:3]) should be set, then write '1' to cmd_line_st (RGA_CMD_CTRL[0]) to start the command line fetch. Incremental command is supported by setting cmd_incr_num (RGA_CMD_CTRL[12:3]) and cmd_incr_valid (RGA_CMD_CTRL[1]=1'b1)

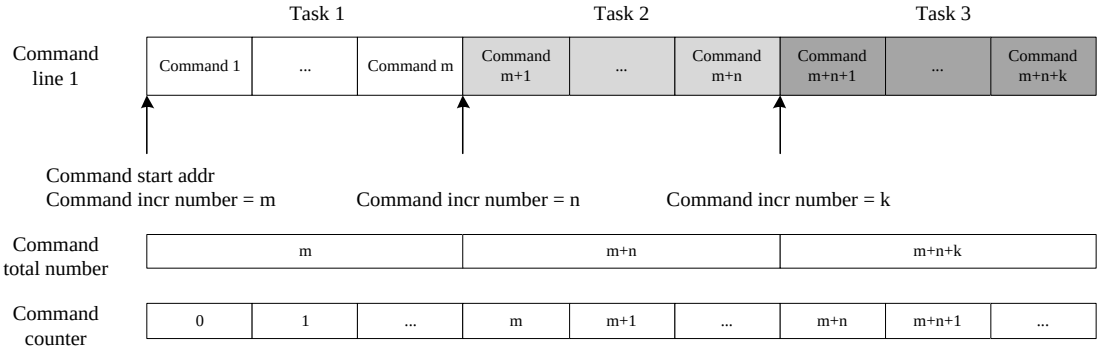


Fig. 8-9RGA command line and command counter

8.5.3 Command Sync

In slave command mode, command sync is controlled by CPU.
In master command mode, user can enable the current_cmd_int(sw_intr_cf), command by command to generate a interrupt at the end point of target command operation.

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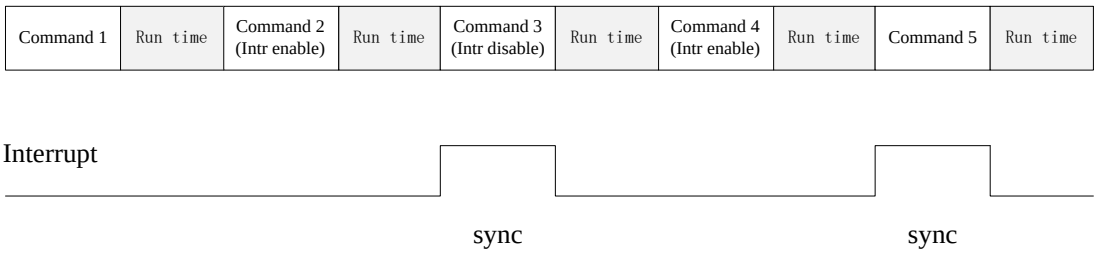


Fig. 8-10RGA command sync generation

8.5.4 ColorPaletteApplication Notes

1. Palette/LUT Load into special RAM in ELS_BUF_CTRL;
2. ColorPalette/Pattern interval operations no need to initialLUT/pattern ram if LUT/patterncontentno update;

8.5.5 Some special application constraint

1. The algorithm of vertical scale up: must select bicubic algorithm when source picture is smaller or equal to 2k and must select bilinear when bigger than 2k

2. The effects that the output's definition is near 2k or 4k maybe not very well when at the scenario that the vertical side is scale up and the horizontal is scale down within range of 2%(such as:2048x32→2008x64)

1

3. At the scenario A+B->C, the size among the A B C has some constraint :
   2 A's size must be equal to C. C's size must equal to B when A+C is no rotation. C's rotation (90degree)size must equal to B1 when A+C is rotation 90 degree .

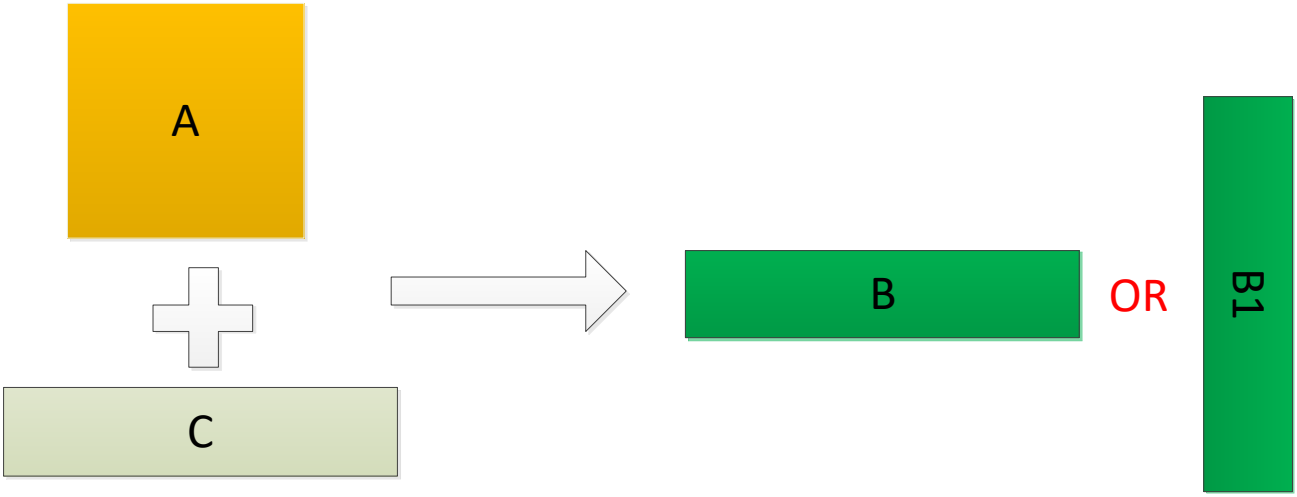


Fig. 8-11 the size constraint among A B C

4. YUV420/422-8bit virtual stride need 8byte align，xoff/yoff need 2byte algin；

5. YUV420/422-10bit virtual stride need 16byte align，not support xoff/yoff；

6. Vertical scale down or not && Horizontal Bi-cubic scale up src0 width<=2048；
   Vertical scale up && Horizontal Bi-cubic scale up src0 width<=1928；

7. Vertical scale down or not && Horizontal Bilinear scale up src0 width<=4096；
   Vertical scale up && Horizontal Bilinear scale up src0 width<=3856；

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Chapter 9 Crypto

9.1 Overview

Crypto is a hardware accelerator for encrypting or decrypting. It supports the most commonly used algorithm: DES/3DES, AES, SHA1, SHA256, MD5 and PKA.
The Crypto supports following features:

- Support Link List Item (LLI) DMA transfer
- Support SHA-1, SHA-256/224, SHA-512/384, MD5 with hardware padding
- Support HMAC of SHA-1, SHA-256, SHA-512, MD5 with hardware padding
- Support AES-128, AES-192, AES-256 encrypt & decrypt cipher
- Support DES & TDES cipher
- Support AES ECB/CBC/OFB/CFB/CTR/CTS/XTS/CCM/GCM/CBC-MAC/CMAC mode
- Support DES/TDES ECB/CBC/OFB/CFB mode
- Support up to 4096 bits PKA mathematical operations for RSA/ECC
- Support up to 8-channels configuration
- Support 256-bits OTP device root key hardwire calculation
- Support Up to 256 bits TRNG Output

9.2 Block Diagram

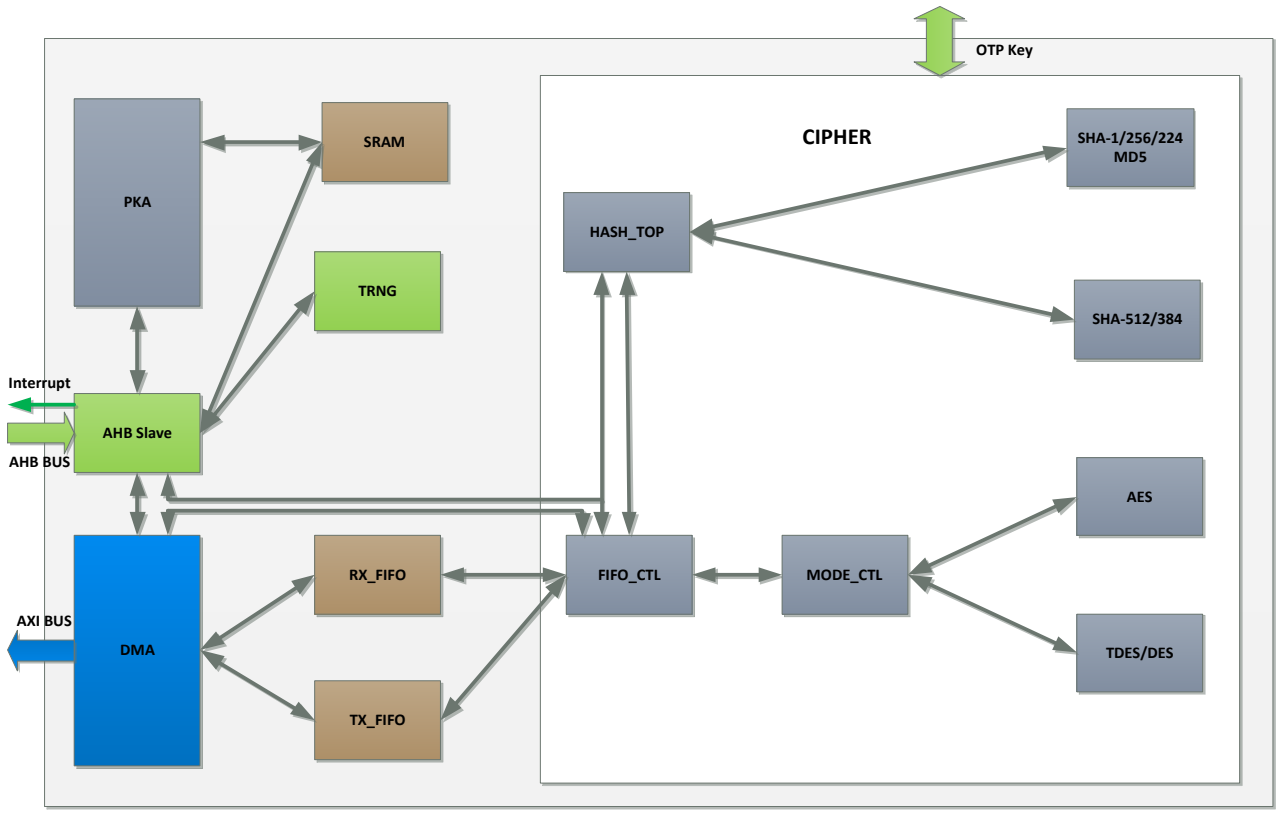


Fig. 9-1 Crypto Architecture

Crypto contains several modules : AHB_Slave, DMA, CIPHER, PKA, TRNG.

AHB_Slave

AHB_Slave is used to configure registers. This module is in HCLK domain.

DMA

DMA is used to transfer data from external memory to RX_FIFO, or from TX_FIFO to external memory. DMA uses 64-bits AXI3 protocol with max burst length to 16. LLI transfer is also supported for performance and convenience consideration. This module is in ACLK domain.

CIPHER

CIPHER contains AES, DES/TDES and HASH engines. And it also supports various mode

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operations. The source data is either from RX_FIFO , or from other engine output. The result data is sending either to TX_FIFO, or Registers in module AHB_Slave. This module is in CLK_CORE domain.

PKA

PKA is used to accelerate mathematical operations for big numbers. It supports - Modular arithmetic (addition, subtraction, multiplication and division), Regular arithmetic (addition, subtraction, multiplication and division), Modular inversion, Modular exponentiation, Logical operations (AND, OR, XOR, SHIFT). PKA has a SRAM which is used to store source , result and intermediate data for PKA operations. The software driver could use PKA operations to implement complicate calculation, such as RSA, ECC etc. It could support up to 4096 bits RSA modular exponentiation calculation. This module is in CLK_PKA domain.

TRNG

TRNG is used to collects random bits from the ring oscillator, up to 256 random bits per time. This module is in HCLK domain.

9.3 Register description

9.3.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

9.3.2 Registers Summary

Name	Offset	Size	Reset Value	Description
CRYPTO_CLK_CTL	0x0000	W	0x00000001	Clock Control Register
CRYPTO_RST_CTL	0x0004	W	0x00000000	Reset Control Register
CRYPTO_DMA_INT_EN	0x0008	W	0x00000000	DMA Interrupt Enable Register
CRYPTO_DMA_INT_ST	0x000c	W	0x00000000	DMA Interrupt Status Register
CRYPTO_DMA_CTL	0x0010	W	0x00000000	DMA Control Register
CRYPTO_DMA_LLI_ADDR	0x0014	W	0x00000000	DMA LIST Start Address Register
CRYPTO_DMA_ST	0x0018	W	0x00000000	DMA Status Register
CRYPTO_DMA_STATE	0x001c	W	0x00000000	DMA State Register
CRYPTO_DMA_LLI_RADDR	0x0020	W	0x00000000	DMA LLI Read Address Register
CRYPTO_DMA_SRC_RADDR	0x0024	W	0x00000000	DMA Source Data Read Address Register
CRYPTO_DMA_DST_WADDR	0x0028	W	0x00000000	DMA Destination Data Read Address Register
CRYPTO_DMA_ITEM_ID	0x002c	W	0x00000000	DMA Descriptor ID Register
CRYPTO_FIFO_CTL	0x0040	W	0x00000003	FIFO Control Register
CRYPTO_BC_CTL	0x0044	W	0x00000000	Block Cipher Control Register
CRYPTO_HASH_CTL	0x0048	W	0x00000004	Hash Control Register
CRYPTO_CIPHER_ST	0x004c	W	0x00000000	Cipher Status Register
CRYPTO_CIPHER_STATE	0x0050	W	0x00000400	Cipher Current State Register
CRYPTO_CHn_IV_0	0x0100	W	0x00000000	Channel n IV Register 0
CRYPTO_CHn_IV_1	0x0104	W	0x00000000	Channel n IV Register 1
CRYPTO_CHn_IV_2	0x0108	W	0x00000000	Channel n IV Register 2
CRYPTO_CHn_IV_3	0x010c	W	0x00000000	Channel n IV Register 3
CRYPTO_CHn_KEY_0	0x0180	W	0x00000000	Channel n KEY Register 0
CRYPTO_CHn_KEY_1	0x0184	W	0x00000000	Channel n KEY Register 1

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Name	Offset	Size	Reset Value	Description
CRYPTO_CHn_KEY_2	0x0188	W	0x00000000	Channel n KEY Register 2
CRYPTO_CHn_KEY_3	0x018c	W	0x00000000	Channel n KEY Register 3
CRYPTO_CHn_PKEY_0	0x0200	W	0x00000000	Channel n Private KEY Register 0
CRYPTO_CHn_PKEY_1	0x0204	W	0x00000000	Channel n Private KEY Register 1
CRYPTO_CHn_PKEY_2	0x0208	W	0x00000000	Channel n Private KEY Register 2
CRYPTO_CHn_PKEY_3	0x020c	W	0x00000000	Channel n Private KEY Register 3
CRYPTO_CHn_PC_LEN_0	0x0280	W	0x00000000	Channel n PC Length Register 0
CRYPTO_CHn_PC_LEN_1	0x0284	W	0x00000000	Channel n PC Length Register 1
CRYPTO_CHn_ADA_LEN_0	0x02c0	W	0x00000000	Channel n ADA Length Register 0
CRYPTO_CHn_ADA_LEN_1	0x02c4	W	0x00000000	Channel n ADA Length Register 1
CRYPTO_CHn_IV_LEN_0	0x0300	W	0x00000000	Channel n IV Length Register 0
CRYPTO_CHn_TAG_0	0x0320	W	0x00000000	Channel n Tag Register 0
CRYPTO_CHn_TAG_1	0x0324	W	0x00000000	Channel n Tag Register 1
CRYPTO_CHn_TAG_2	0x0328	W	0x00000000	Channel n Tag Register 2
CRYPTO_CHn_TAG_3	0x032c	W	0x00000000	Channel n Tag Register 3
CRYPTO_HASH_DOUT_0	0x03a0	W	0x00000000	HASH Data Output Register 0
CRYPTO_HASH_DOUT_1	0x03a4	W	0x00000000	HASH Data Output Register 1
CRYPTO_HASH_DOUT_2	0x03a8	W	0x00000000	HASH Data Output Register 2
CRYPTO_HASH_DOUT_3	0x03ac	W	0x00000000	HASH Data Output Register 3
CRYPTO_HASH_DOUT_4	0x03b0	W	0x00000000	HASH Data Output Register 4
CRYPTO_HASH_DOUT_5	0x03b4	W	0x00000000	HASH Data Output Register 5
CRYPTO_HASH_DOUT_6	0x03b8	W	0x00000000	HASH Data Output Register 6
CRYPTO_HASH_DOUT_7	0x03bc	W	0x00000000	HASH Data Output Register 7
CRYPTO_HASH_DOUT_8	0x03c0	W	0x00000000	HASH Data Output Register 8
CRYPTO_HASH_DOUT_9	0x03c4	W	0x00000000	HASH Data Output Register 9
CRYPTO_HASH_DOUT_10	0x03c8	W	0x00000000	HASH Data Output Register 10
CRYPTO_HASH_DOUT_11	0x03cc	W	0x00000000	HASH Data Output Register 11
CRYPTO_HASH_DOUT_12	0x03d0	W	0x00000000	HASH Data Output Register 12
CRYPTO_HASH_DOUT_13	0x03d4	W	0x00000000	HASH Data Output Register 13
CRYPTO_HASH_DOUT_14	0x03d8	W	0x00000000	HASH Data Output Register 14
CRYPTO_HASH_DOUT_15	0x03dc	W	0x00000000	HASH Data Output Register 15
CRYPTO_TAG_VALID	0x03e0	W	0x00000000	TAG Valid Register
CRYPTO_HASH_VALID	0x03e4	W	0x00000000	HASH Output Valid Register
CRYPTO_VERSION	0x03f0	W	0x00000000	CRYPTO Vertion Number Register
CRYPTO_RNG_CTL	0x0400	W	0x0000000c	RNG Control Register
CRYPTO_RNG_SAMPLE_CNT	0x0404	W	0x00000000	RNG Sample Counter Register
CRYPTO_RNG_DOUT_0	0x0410	W	0x00000000	RNG Data Output Register 0
CRYPTO_RNG_DOUT_1	0x0414	W	0x00000000	RNG Data Output Register 1
CRYPTO_RNG_DOUT_2	0x0418	W	0x00000000	RNG Data Output Register 2
CRYPTO_RNG_DOUT_3	0x041c	W	0x00000000	RNG Data Output Register 3
CRYPTO_RNG_DOUT_4	0x0420	W	0x00000000	RNG Data Output Register 4

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Name	Offset	Size	Reset Value	Description
CRYPTO_RNG_DOUT_5	0x0424	W	0x00000000	RNG Data Output Register 5
CRYPTO_RNG_DOUT_6	0x0428	W	0x00000000	RNG Data Output Register 6
CRYPTO_RNG_DOUT_7	0x042c	W	0x00000000	RNG Data Output Register 7
CRYPTO_RAM_CTL	0x0480	W	0x00000000	RAM Control Register
CRYPTO_RAM_ST	0x0484	W	0x00000001	RAM Status Register
CRYPTO_DEBUG_CTL	0x04a0	W	0x00000000	PKA Debug Control Register
CRYPTO_DEBUG_ST	0x04a4	W	0x00000001	PKA Debug Status Register
CRYPTO_DEBUG_MONITOR	0x04a8	W	0x0000feef	PKA Debug Monitor Bus Register
CRYPTO_PKA_MEM_MAP0	0x0800	W	0x00000000	PKA Memory Map 0 Register
CRYPTO_PKA_MEM_MAP1	0x0804	W	0x00000000	PKA Memory Map 1 Register
CRYPTO_PKA_MEM_MAP2	0x0808	W	0x00000000	PKA Memory Map 2 Register
CRYPTO_PKA_MEM_MAP3	0x080c	W	0x00000000	PKA Memory Map 3 Register
CRYPTO_PKA_MEM_MAP4	0x0810	W	0x00000000	PKA Memory Map 4 Register
CRYPTO_PKA_MEM_MAP5	0x0814	W	0x00000000	PKA Memory Map 5 Register
CRYPTO_PKA_MEM_MAP6	0x0818	W	0x00000000	PKA Memory Map 6 Register
CRYPTO_PKA_MEM_MAP7	0x081c	W	0x00000000	PKA Memory Map 7 Register
CRYPTO_PKA_MEM_MAP8	0x0820	W	0x00000000	PKA Memory Map 8 Register
CRYPTO_PKA_MEM_MAP9	0x0824	W	0x00000000	PKA Memory Map 9 Register
CRYPTO_PKA_MEM_MAP10	0x0828	W	0x00000000	PKA Memory Map 10 Register
CRYPTO_PKA_MEM_MAP11	0x082c	W	0x00000000	PKA Memory Map 11 Register
CRYPTO_PKA_MEM_MAP12	0x0830	W	0x00000000	PKA Memory Map 12 Register
CRYPTO_PKA_MEM_MAP13	0x0834	W	0x00000000	PKA Memory Map 13 Register
CRYPTO_PKA_MEM_MAP14	0x0838	W	0x00000000	PKA Memory Map 14 Register
CRYPTO_PKA_MEM_MAP15	0x083c	W	0x00000000	PKA Memory Map 15 Register
CRYPTO_PKA_MEM_MAP16	0x0840	W	0x00000000	PKA Memory Map 16 Register
CRYPTO_PKA_MEM_MAP17	0x0844	W	0x00000000	PKA Memory Map 17 Register
CRYPTO_PKA_MEM_MAP18	0x0848	W	0x00000000	PKA Memory Map 18 Register
CRYPTO_PKA_MEM_MAP19	0x084c	W	0x00000000	PKA Memory Map 19 Register
CRYPTO_PKA_MEM_MAP20	0x0850	W	0x00000000	PKA Memory Map 20 Register
CRYPTO_PKA_MEM_MAP21	0x0854	W	0x00000000	PKA Memory Map 21 Register

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Name	Offset	Size	Reset Value	Description
CRYPTO_PKA_MEM_MAP22	0x0858	W	0x00000000	PKA Memory Map 22 Register
CRYPTO_PKA_MEM_MAP23	0x085c	W	0x00000000	PKA Memory Map 23 Register
CRYPTO_PKA_MEM_MAP24	0x0860	W	0x00000000	PKA Memory Map 24 Register
CRYPTO_PKA_MEM_MAP25	0x0864	W	0x00000000	PKA Memory Map 25 Register
CRYPTO_PKA_MEM_MAP26	0x0868	W	0x00000000	PKA Memory Map 26 Register
CRYPTO_PKA_MEM_MAP27	0x086c	W	0x00000000	PKA Memory Map 27 Register
CRYPTO_PKA_MEM_MAP28	0x0870	W	0x00000000	PKA Memory Map 28 Register
CRYPTO_PKA_MEM_MAP29	0x0874	W	0x00000000	PKA Memory Map 29 Register
CRYPTO_PKA_MEM_MAP30	0x0878	W	0x00000000	PKA Memory Map 30 Register
CRYPTO_PKA_MEM_MAP31	0x087c	W	0x00000000	PKA Memory Map 31 Register
CRYPTO_PKA_OPCODE	0x0880	W	0x00000000	PKA Operation Code Register
CRYPTO_N_NP_TO_T1_ADDR	0x0884	W	0x000ff820	N_NP_TO_T1_ADDR Register
CRYPTO_PKA_STATUS	0x0888	W	0x00000001	PKA Status Register
CRYPTO_PKA_SW_RESET	0x088c	W	0x00000000	software reset of PKA
CRYPTO_PKA_L0	0x0890	W	0x00000000	PKA Length 0 Register
CRYPTO_PKA_L1	0x0894	W	0x00000000	PKA Length 1 Register
CRYPTO_PKA_L2	0x0898	W	0x00000000	PKA Length 2 Register
CRYPTO_PKA_L3	0x089c	W	0x00000000	PKA Length 3 Register
CRYPTO_PKA_L4	0x08a0	W	0x00000000	PKA Length 4 Register
CRYPTO_PKA_L5	0x08a4	W	0x00000000	PKA Length 5 Register
CRYPTO_PKA_L6	0x08a8	W	0x00000000	PKA Length 6 Register
CRYPTO_PKA_L7	0x08ac	W	0x00000000	PKA Length 7 Register
CRYPTO_PKA_PIPE_RDY	0x08b0	W	0x00000001	PKA pipe is ready for new opcode
CRYPTO_PKA_DONE	0x08b4	W	0x00000001	PKA Done Register
CRYPTO_PKA_MON_SELECT	0x08b8	W	0x00000000	PKA Monitor Select Register
CRYPTO_PKA_DEBUG_REG_EN	0x08bc	W	0x00000000	PKA Debug Enable Register
CRYPTO_DEBUG_CNT_ADDR	0x08c0	W	0x00000000	Debug Counter Address Register
CRYPTO_DEBUG_EXT_ADDR	0x08c4	W	0x00000000	Debug Extra Address Register

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Name	Offset	Size	Reset Value	Description
CRYPTO_PKA_DEBUG_HALT	0x08c8	W	0x00000000	PKA Debug Halt State Register
CRYPTO_PKA_MON_READ	0x08d0	W	0x0000feef	PKA Monitor Read Register
CRYPTO_PKA_INT_ENA	0x08d4	W	0x00000000	PKA Interrupt Enable Register
CRYPTO_PKA_INT_ST	0x08d8	W	0x00000000	PKA Interrupt Status Register
CRYPTO_SRAM_ADDR	0x1000	W	0x00000000	SRAM Base Address

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

9.3.3 Detail Register Description

CRYPTO_CLK_CTL

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:17	RO	0x0	reserved
16	WO	0x0	write_enable When bit n=1, the corresponding bit n-16 can be written by software; When bit n=0, the corresponding bit n-16 can't be written by software.
15:1	RO	0x0	reserved
0	RW	0x1	auto_clkgate_en 1: enable. CRYPTO will gate unused Block Cipher and HASH module automatically to save power. 0: disable. Symmetric Cipher and HASH Module clock will be always available.

CRYPTO_RST_CTL

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:16	RW	0x0	write_enable When bit n=1, the corresponding bit n-16 can be written by software; When bit n=0, the corresponding bit n-16 can't be written by software.
15:3	RO	0x0	reserved
2	RW	0x0	sw_pka_reset Software set this bit to start a reset to PKA module. After the reset is done, CRYPTO will clear this bit.
1	RW	0x0	sw_rng_reset Software set this bit to start a reset to TRNG module. After the reset is done, CRYPTO will clear this bit.
0	R/WSC	0x0	sw_cc_reset Software set this bit to start a reset to Symmetric Cipher and HASH module. After the reset is done, CRYPTO will clear this bit.

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CRYPTO_DMA_INT_EN

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:7	RO	0x0	reserved
6	RW	0x0	zero_len_int_en 1: enable ; 0: disable;
5	RW	0x0	list_err_int_en 1: enable ; 0: disable;
4	RW	0x0	src_err_int_en 1: enable ; 0: disable.
3	RW	0x0	dst_err_int_en 1: enable ; 0: disable;
2	RW	0x0	src_item_done_int_en 1: enable ; 0: disable.
1	RW	0x0	dst_item_done_int_en 1: enable ; 0: disable.
0	RW	0x0	list_done_int_en 1: enable ; 0: disable.

CRYPTO_DMA_INT_ST

Address: Operational Base + offset (0x000c)

Bit	Attr	Reset Value	Description
31:7	RO	0x0	reserved
6	W1C	0x0	zero_len Indicate that DMA has met an 0 byte source transfer length in list descriptors. After the bit is read, the application should write 1 to clear this bit for next time use.
5	W1C	0x0	list_err Indicate that DMA has met an error response when transfer list descriptors. The state machine will exit current transfer and then return to IDLE state. After the bit is read, the application should write 1 to clear this bit for next time use.
4	W1C	0x0	src_err Indicate that DMA has met an error response when transfer source data. The state machine will exit current transfer and then return to IDLE state. After the bit is read, the application should write 1 to clear this bit for next time use.

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Bit	Attr	Reset Value	Description
3	W1C	0x0	dst_err Indicate that DMA has met an error response when transfer destination data. The state machine will exit current transfer and then return to IDLE state. After the bit is read, the application should write 1 to clear this bit for next time use.
2	W1C	0x0	src_item_done Indicate that DMA has completed a read transfers which the current list descriptor pointed to . After the bit is read, the application should write 1 to clear this bit for next time use.
1	W1C	0x0	dst_item_done Indicate that DMA has completed a write transfers which the current list descriptor pointed to . After the bit is read, the application should write 1 to clear this bit for next time use.
0	W1C	0x0	list_done Indicate that DMA has completed all the transfers which the list descriptors pointed to . After the bit is read, the application should write 1 to clear this bit for next time use.

CRYPTO_DMA_CTL

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:18	RO	0x0	reserved
17:16	WO	0x0	write_enable When bit n=1, the corresponding bit n-16 can be written by software; When bit n=0, the corresponding bit n-16 can't be written by software.
15:2	RO	0x0	reserved
1	R/WSC	0x0	dma_restart If DMA data for next stage is not ready, application could pause DMA by descriptor commands. DMA will stop prefetching next descriptor . The application could restart DMA by asserting this bit when DMA data for next state is ready. Crypto will continue with previous transfer, and clear the bit automatically.
0	R/WSC	0x0	dma_start DMA asserts the bit to start DMA transfer, then Crypto will clear the bit automatically .

CRYPTO_DMA_LLI_ADDR

Address: Operational Base + offset (0x0014)

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Bit	Attr	Reset Value	Description
31:3	RW	0x00000000	dma_lli_addr When DMA_CTL.start asserted, Crypto will read the address to get the 1'st descriptor. It should be 8-bytes align. We suggest dma_lli_addr 64-byte align for best performance consideration.
2:0	RO	0x0	reserved

CRYPTO_DMA_ST

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	dma_busy 1: dma busy ; 0: dma idle ;

CRYPTO_DMA_STATE

Address: Operational Base + offset (0x001c)

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5:4	RO	0x0	dma_lli_state For debug use only. 00: IDLE STATE; 01: FETCH STATE ; 10: WORK STATE ;
3:2	RO	0x0	dma_src_state For debug use only. 00: IDLE STATE; 01: LOAD STATE ; 10: WORK STATE ;
1:0	RO	0x0	dma_dst_state For debug use only. 00: IDLE STATE; 01: LOAD STATE ; 10: WORK STATE ;

CRYPTO_DMA_LLI_RADDR

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dma_lli_raddr For debug use only. It indicates the current dma lli read address.

CRYPTO_DMA_SRC_RADDR

Address: Operational Base + offset (0x0024)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dma_src_raddr For debug use only. It indicates the current dma source read address.

CRYPTO_DMA_DST_WADDR

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	dma_dst_waddr For debug use only. It indicates the current dma destination write address.

CRYPTO_DMA_ITEM_ID

Address: Operational Base + offset (0x002c)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RO	0x00	dma_item_id For debug use only. It indicates the current descriptor ID.

CRYPTO_FIFO_CTL

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:18	RO	0x0	reserved
17:16	WO	0x0	write_enable When bit n=1, the corresponding bit n-16 can be written by software; When bit n=0, the corresponding bit n-16 can't be written by software.
15:2	RO	0x0	reserved
1	RW	0x1	dout_byteswap 1: little endian ; 0: big endian .
0	RW	0x1	din_byteswap 1: little endian ; 0: big endian .

CRYPTO_BC_CTL

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:16	WO	0x000	write_enable When bit n=1, the corresponding bit n-16 can be written by software; When bit n=0, the corresponding bit n-16 can't be written by software.
15:10	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
9:8	RW	0x0	bc_cipher_sel 00: AES ; 01: Reserved; 10: DES ; 11: TDES .
7:4	RW	0x0	mode FOR AES, 0: ECB ; 1: CBC ; 2: CTS ; 3: CTR ; 4: CFB ; 5: OFB ; 6: XTS ; 7: CCM; 8: GCM; 9: CMAC ; A: CBC-MAC. Others: Reserved. For TDES/DES , 0: ECB ; 1: CBC ; 4: CFB ; 5: OFB ; Others: Reserved.
3:2	RW	0x0	key_size For AES , 00: 128 bit ; 01: 192 bit ; 10: 256 bit ; 11: reserved. For TDES/DES, it is reserved.
1	RW	0x0	decrypt 1: decrypt ; 0: encrypt .
0	RW	0x0	bc_enable 1: enable ; 0: disable .

CRYPTO_HASH_CTL

Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved

Bit	Attr	Reset Value	Description
23:16	WO	0x00	write_enable When bit n=1, the corresponding bit n-16 can be written by software; When bit n=0, the corresponding bit n-16 can't be written by software.
15:8	RO	0x0	reserved
7:4	RW	0x0	hash_cipher_sel 0: SHA-1 ; 1: MD-5 ; 2: SHA-256 ; 3: SHA-224 ; 8: SHA-512 ; 9: SHA-384 ; A: SHA-512/224 ; B: SHA-512/256 ; Others: Reserved.
3	RW	0x0	hmac_enable Crypto supports HMAC-SHA1, HMAC-SHA256, HMAC_SHA512. 1: enable ; 0: disable.
2	RW	0x1	hw_pad_enable 1: enable ; 0: disable .
1	RW	0x0	hash_src_sel 0: from RX-FIFO ; 1: from TX-FIFO .
0	RW	0x0	hash_enable 1: enable ; 0: disable.

CRYPTO_CIPHER_ST

Address: Operational Base + offset (0x004c)

Bit	Attr	Reset Value	Description
31:3	RO	0x0	reserved
2	RO	0x0	otp_key_valid Indicate if otp_key is valid. 1: valid ; 0: invalid .
1	RO	0x0	hash_busy 1: busy ; 0: idle ;
0	RO	0x0	block_cipher_busy 1: busy ; 0: idle ;

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CRYPTO_CIPHER_STATE

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:15	RO	0x0	reserved
14:10	RW	0x01	hash_state For debug use only. 00001: IDLE State ; 00010: IPAD State ; 00100: TEXT State; 01000: OPAD State; 10000: OPAD EXT State .
9:8	RW	0x0	gcm_state For debug use only. 00: IDLE State; 01: PRE State; 10: NA State; 11: PC State.
7:6	RW	0x0	ccm_state For debug use only. 00: IDLE State; 01: PRE State; 10: NA State; 11: PC State.
5:4	RW	0x0	parallel_state For debug use only. 00: IDLE State; 01: PRE State; 10: BULK State. 11: Reserved
3:2	RW	0x0	mac_state For debug use only. 00: IDLE State; 01: PRE State; 10: BULK State. 11: Reserved
1:0	RO	0x0	serial_state For debug use only. 00: IDLE State; 01: PRE State; 10: BULK State. 11: Reserved

CRYPTO_CHn_IV_0

Address: Operational Base + offset (0x0100)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	chn_iv_0 Channel n range from 0 to 7. CHn_IV_0 address = 0x0100 + 0x10 * n . For CTR Mode, IV stands for counter. For XTS Mode, IV stands for tweak.

CRYPTO_CHn_IV_1

Address: Operational Base + offset (0x0104)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	chn_iv_1 Channel n range from 0 to 7. CHn_IV_1 address = 0x0104 + 0x10 * n . For CTR Mode, IV stands for counter. For XTS Mode, IV stands for tweak.

CRYPTO_CHn_IV_2

Address: Operational Base + offset (0x0108)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	chn_iv_2 Channel n range from 0 to 7. CHn_IV_2 address = 0x0108 + 0x10 * n . For CTR Mode, IV stands for counter. For XTS Mode, IV stands for tweak.

CRYPTO_CHn_IV_3

Address: Operational Base + offset (0x010c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	chn_iv_3 Channel n range from 0 to 7. CHn_IV_3 address = 0x010c + 0x10 * n . For CTR Mode, IV stands for counter. For XTS Mode, IV stands for tweak.

CRYPTO_CHn_KEY_0

Address: Operational Base + offset (0x0180)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	chn_key_0 Channel n range from 0 to 7. CHn_KEY_0 address = 0x0180 + 0x10 * n .

CRYPTO_CHn_KEY_1

Address: Operational Base + offset (0x0184)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	chn_key_1 Channel n range from 0 to 7. CHn_KEY_1 address = 0x0184 + 0x10 * n .

CRYPTO_CHn_KEY_2

Address: Operational Base + offset (0x0188)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	chn_key_2 Channel n range from 0 to 7. CHn_KEY_2 address = 0x0188 + 0x10 * n .

CRYPTO_CHn_KEY_3

Address: Operational Base + offset (0x018c)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	chn_key_3 Channel n range from 0 to 7. CHn_KEY_3 address = 0x018c + 0x10 * n .

CRYPTO_CHn_PKEY_0

Address: Operational Base + offset (0x0200)

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	chn_pkey_0 Channel n range from 0 to 7. CHn_PKEY_0 address = 0x0200 + 0x10 * n .

CRYPTO_CHn_PKEY_1

Address: Operational Base + offset (0x0204)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	chn_pkey_1 Channel n range from 0 to 7. CHn_PKEY_1 address = 0x0204 + 0x10 * n .

CRYPTO_CHn_PKEY_2

Address: Operational Base + offset (0x0208)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	chn_pkey_2 Channel n range from 0 to 7. CHn_PKEY_2 address = 0x208 + 0x10 * n .

CRYPTO_CHn_PKEY_3

Address: Operational Base + offset (0x020c)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	chn_key_3 Channel n range from 0 to 7. CHn_PKEY_3 address = 0x020c + 0x10 * n .

CRYPTO_CHn_PC_LEN_0

Address: Operational Base + offset (0x0280)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	chn_pc_len_0 Channel n range from 0 to 7. CHn_PC_LEN_0 address = 0x0280 + 0x8 * n . Length in byte unit.

CRYPTO_CHn_PC_LEN_1

Address: Operational Base + offset (0x0284)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:0	RW	0x00000000	chn_pc_len_1 Channel n range from 0 to 7. CHn_PC_LEN_1 address = 0x0284 + 0x8 * n . Length in byte unit.

CRYPTO_CHn_ADA_LEN_0

Address: Operational Base + offset (0x02c0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	chn_ada_len_0 Channel n range from 0 to 7. CHn_ADA_LEN_0 address = 0x02c0 + 0x8 * n . Length in byte unit.

CRYPTO_CHn_ADA_LEN_1

Address: Operational Base + offset (0x02c4)

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:0	RW	0x00000000	chn_ada_len_1 Channel n range from 0 to 7. CHn_ADA_LEN_1 address = 0x02c4 + 0x8 * n . Length in byte unit.

CRYPTO_CHn_IV_LEN_0

Address: Operational Base + offset (0x0300)

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Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4:0	RW	0x00	chn_iv_len Channel n range from 0 to 7. CHn_IV_LEN_0 address = 0x0300 + 0x4 * n . Length in byte unit. Up to 16 byte IV for GCM

CRYPTO_CHn_TAG_0

Address: Operational Base + offset (0x0320)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	chn_tag_0 Channel n range from 0 to 7. CHn_TAG_0 address = 0x0320 + 0x10 * n . When the corresponding TAG_VALID is high, TAG value is valid.

CRYPTO_CHn_TAG_1

Address: Operational Base + offset (0x0324)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	chn_tag_1 Channel n range from 0 to 7. CHn_TAG_1 address = 0x0324 + 0x10 * n . When the corresponding TAG_VALID is high, TAG value is valid.

CRYPTO_CHn_TAG_2

Address: Operational Base + offset (0x0328)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	chn_tag_2 Channel n range from 0 to 7. CHn_TAG_2 address = 0x0328 + 0x10 * n . When the corresponding TAG_VALID is high, TAG value is valid.

CRYPTO_CHn_TAG_3

Address: Operational Base + offset (0x032c)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	chn_tag_3 Channel n range from 0 to 7. CHn_TAG_3 address = 0x032c + 0x10 * n . When the corresponding TAG_VALID is high, TAG value is valid.

CRYPTO_HASH_DOUT_0

Address: Operational Base + offset (0x03a0)

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	hash_dout_0 0'th output word for all hash function, in big endian.

CRYPTO_HASH_DOUT_1

Address: Operational Base + offset (0x03a4)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	hash_dout_1 1'th output word for all hash function, in big endian.

CRYPTO_HASH_DOUT_2

Address: Operational Base + offset (0x03a8)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	hash_dout_2 2'th output word for all hash function, in big endian.

CRYPTO_HASH_DOUT_3

Address: Operational Base + offset (0x03ac)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	hash_dout_3 3'th output word for all hash function, in big endian.This is MD5 last output word. HASH_DOUT_4 ~ HASH_DOUT_15 is invalid data for MD5.

CRYPTO_HASH_DOUT_4

Address: Operational Base + offset (0x03b0)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	hash_dout_4 4'th output word for all hash function, in big endian.This is SHA-1 last output word. HASH_DOUT_5 ~ HASH_DOUT_15 is invalid data for SHA-1.

CRYPTO_HASH_DOUT_5

Address: Operational Base + offset (0x03b4)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	hash_dout_5 5'th output word for all hash function, in big endian.

CRYPTO_HASH_DOUT_6

Address: Operational Base + offset (0x03b8)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	hash_dout_6 6'th output word for all hash function, in big endian.

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CRYPTO_HASH_DOUT_7

Address: Operational Base + offset (0x03bc)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	hash_dout_7 7'th output word for all hash function, in big endian.This is SHA-256/224 last output word. HASH_DOUT_8 ~ HASH_DOUT_15 is invalid data for SHA-256/224.

CRYPTO_HASH_DOUT_8

Address: Operational Base + offset (0x03c0)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	hash_dout_8 8'th output word for all hash function, in big endian.

CRYPTO_HASH_DOUT_9

Address: Operational Base + offset (0x03c4)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	hash_dout_9 9'th output word for all hash function, in big endian.

CRYPTO_HASH_DOUT_10

Address: Operational Base + offset (0x03c8)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	hash_dout_10 10'th output word for all hash function, in big endian.

CRYPTO_HASH_DOUT_11

Address: Operational Base + offset (0x03cc)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	hash_dout_11 11'th output word for all hash function, in big endian.

CRYPTO_HASH_DOUT_12

Address: Operational Base + offset (0x03d0)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	hash_dout_12 12'th output word for all hash function, in big endian.

CRYPTO_HASH_DOUT_13

Address: Operational Base + offset (0x03d4)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	hash_dout_13 13'th output word for all hash function, in big endian.

CRYPTO_HASH_DOUT_14

Address: Operational Base + offset (0x03d8)

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	hash_dout_14 14'th output word for all hash function, in big endian.

CRYPTO_HASH_DOUT_15

Address: Operational Base + offset (0x03dc)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	hash_dout_15 15'th output word for all hash function, in big endian.This is SHA-512, SHA-384, SHA-512/224, SHA-512/256 last output word.

CRYPTO_TAG_VALID

Address: Operational Base + offset (0x03e0)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7	W1C	0x0	ch7_tag_valid When channel 7 tag calculation is finished, CRYPTO will set this bit. After the bit is read by application, it should be cleared by writing 1 to this bit. 1: channel 7 tag is valid ; 0: channel 7 tag is invalid ;
6	W1C	0x0	ch6_tag_valid When channel 6 tag calculation is finished, CRYPTO will set this bit. After the bit is read by application, it should be cleared by writing 1 to this bit. 1: channel 6 tag is valid ; 0: channel 6 tag is invalid ;
5	W1C	0x0	ch5_tag_valid When channel 5 tag calculation is finished, CRYPTO will set this bit. After the bit is read by application, it should be cleared by writing 1 to this bit. 1: channel 5 tag is valid ; 0: channel 5 tag is invalid ;
4	W1C	0x0	ch4_tag_valid When channel 4 tag calculation is finished, CRYPTO will set this bit. After the bit is read by application, it should be cleared by writing 1 to this bit. 1: channel 4 tag is valid ; 0: channel 4 tag is invalid ;
3	W1C	0x0	ch3_tag_valid When channel 3 tag calculation is finished, CRYPTO will set this bit. After the bit is read by application, it should be cleared by writing 1 to this bit. 1: channel 3 tag is valid ; 0: channel 3 tag is invalid ;

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Bit	Attr	Reset Value	Description
2	W1C	0x0	ch2_tag_valid When channel 2 tag calculation is finished, CRYPTO will set this bit. After the bit is read by application, it should be cleared by writing 1 to this bit. 1: channel 2 tag is valid ; 0: channel 2 tag is invalid ;
1	W1C	0x0	ch1_tag_valid When channel 1 tag calculation is finished, CRYPTO will set this bit. After the bit is read by application, it should be cleared by writing 1 to this bit. 1: channel 1 tag is valid ; 0: channel 1 tag is invalid ;
0	W1C	0x0	ch0_tag_valid When channel 0 tag calculation is finished, CRYPTO will set this bit. After the bit is read by application, it should be cleared by writing 1 to this bit. 1: channel 0 tag is valid ; 0: channel 0 tag is invalid ;

CRYPTO_HASH_VALID

Address: Operational Base + offset (0x03e4)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	W1C	0x0	hash_valid When HASH calculation is finished, CRYPTO will set this bit. After the bit is read by application, it should be cleared by writing 1 to this bit. 1: HASH_DOUT is valid ; 0: HASH_DOUT is invalid ;

CRYPTO_VERSION

Address: Operational Base + offset (0x03f0)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	version_num Version number: V1.0.0.0.

CRYPTO_RNG_CTL

Address: Operational Base + offset (0x0400)

Bit	Attr	Reset Value	Description
31:22	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
21:16	WO	0x00	write_enable When bit n=1, the corresponding bit n-16 can be written by software; When bit n=0, the corresponding bit n-16 can't be written by software.
15:6	RO	0x0	reserved
5:4	RW	0x0	rng_len 00: 64 bit; 01: 128 bit; 10: 192 bit; 11: 256 bit;
3:2	RW	0x3	ring_sel There are 4 osc rings choice to decide the rng output data. 00: fatest osc ring ; 01: slower than osc ring 0 ; 10: slower than osc ring 1 ; 11: slowest osc ring ;
1	RW	0x0	rng_enable 1: enable ; 0: disable.
0	R/WSC	0x0	rng_start The application triggers this bit to start collect rng output data. After rng is started, CRYPTO will clear the bit automatically. 1: start ; 0: do nothing .

CRYPTO_RNG_SAMPLE_CNT

Address: Operational Base + offset (0x0404)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0000	rng_sample_cnt RNG collects osc ring output bit every rng_sample_cnt time. The value of rng_sample_cnt affects RNG output data rate, the value more bigger, the rate more slower.

CRYPTO_RNG_DOUT_0

Address: Operational Base + offset (0x0410)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rng_dout_0 The 32'th osc ring bit is captured in RNG_DOUT_0.bit31.

CRYPTO_RNG_DOUT_1

Address: Operational Base + offset (0x0414)

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rng_dout_1 The 64'th osc ring bit is captured in RNG_DOUT_1.bit31. If RNG_CTL.rng_len = 0x00, the last valid bit of RNG is stored in RNG_DOUT_1.bit31, and RNG_DOUT_2 ~ RNG_DOUT_7 are invalid.

CRYPTO_RNG_DOUT_2

Address: Operational Base + offset (0x0418)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rng_dout_2 The 96'th osc ring bit is captured in RNG_DOUT_2.bit31.

CRYPTO_RNG_DOUT_3

Address: Operational Base + offset (0x041c)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rng_dout_3 The 128'th osc ring bit is captured in RNG_DOUT_3.bit31. If RNG_CTL.rng_len = 0x01, the last valid bit of RNG is stored in RNG_DOUT_3.bit31, and RNG_DOUT_4 ~ RNG_DOUT_7 are invalid.

CRYPTO_RNG_DOUT_4

Address: Operational Base + offset (0x0420)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rng_dout_4 The 160'th osc ring bit is captured in RNG_DOUT_4.bit31.

CRYPTO_RNG_DOUT_5

Address: Operational Base + offset (0x0424)

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	rng_dout_5 The 192'th osc ring bit is captured in RNG_DOUT_5.bit31. If RNG_CTL.rng_len = 0x02, the last valid bit of RNG is stored in RNG_DOUT_5.bit31, and RNG_DOUT_6~ RNG_DOUT_7 are invalid.

CRYPTO_RNG_DOUT_6

Address: Operational Base + offset (0x0428)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rng_dout_6 The 224'th osc ring bit is captured in RNG_DOUT_6.bit31.

CRYPTO_RNG_DOUT_7

Address: Operational Base + offset (0x042c)

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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rng_dout_7 The 256'th osc ring bit is captured in RNG_DOUT_7.bit31. If RNG_CTL.rng_len = 0x03, the last valid bit of RNG is stored in RNG_DOUT_7.bit31.

CRYPTO_RAM_CTL

Address: Operational Base + offset (0x0480)

Bit	Attr	Reset Value	Description
31:17	RO	0x0	reserved
16	WO	0x0	write_enable When bit n=1, the corresponding bit n-16 can be written by software; When bit n=0, the corresponding bit n-16 can't be written by software.
15:1	RO	0x0	reserved
0	RW	0x0	ram_pka_rdy Indicate whether ram is controlled by PKA engine. 0: ram is controlled by CPU. 1: ram is controlled by CRYPTO PKA engine.

CRYPTO_RAM_ST

Address: Operational Base + offset (0x0484)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RO	0x1	clk_ram_rdy Indicate whether clk_ram is stable, and ready for use. 0: not stable ; 1: stable.

CRYPTO_DEBUG_CTL

Address: Operational Base + offset (0x04a0)

Bit	Attr	Reset Value	Description
31:17	RO	0x0	reserved
16	WO	0x0	write_enable When bit n=1, the corresponding bit n-16 can be written by software; When bit n=0, the corresponding bit n-16 can't be written by software.
15:1	RO	0x0	reserved
0	RW	0x0	pka_debug_mode 1: PKA is in debug mode ; 0: PKA is in normal mode.

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CRYPTO_DEBUG_ST

Address: Operational Base + offset (0x04a4)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RO	0x1	pka_debug_clk_en For debug use only.

CRYPTO_DEBUG_MONITOR

Address: Operational Base + offset (0x04a8)

Bit	Attr	Reset Value	Description
31:0	RW	0x0000feef	pka_monitor_bus For debug use only.

CRYPTO_PKA_MEM_MAP0

Address: Operational Base + offset (0x0800)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:2	RW	0x000	memory_map0 memory map 0 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

CRYPTO_PKA_MEM_MAP1

Address: Operational Base + offset (0x0804)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:2	RW	0x000	memory_map1 memory map 1 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

CRYPTO_PKA_MEM_MAP2

Address: Operational Base + offset (0x0808)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:2	RW	0x000	memory_map2 memory map 2 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

CRYPTO_PKA_MEM_MAP3

Address: Operational Base + offset (0x080c)

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Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:2	RW	0x000	memory_map3 memory map 3 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

CRYPTO_PKA_MEM_MAP4

Address: Operational Base + offset (0x0810)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:2	RW	0x000	memory_map4 memory map 4 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

CRYPTO_PKA_MEM_MAP5

Address: Operational Base + offset (0x0814)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:2	RW	0x000	memory_map5 memory map 5 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

CRYPTO_PKA_MEM_MAP6

Address: Operational Base + offset (0x0818)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:2	RW	0x000	memory_map6 memory map 6 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

CRYPTO_PKA_MEM_MAP7

Address: Operational Base + offset (0x081c)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:2	RW	0x000	memory_map7 memory map 7 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

CRYPTO_PKA_MEM_MAP8

Address: Operational Base + offset (0x0820)

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Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:2	RW	0x000	memory_map8 memory map 8 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

CRYPTO_PKA_MEM_MAP9

Address: Operational Base + offset (0x0824)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:2	RW	0x000	memory_map9 memory map 9 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

CRYPTO_PKA_MEM_MAP10

Address: Operational Base + offset (0x0828)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:2	RW	0x000	memory_map10 memory map 10 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

CRYPTO_PKA_MEM_MAP11

Address: Operational Base + offset (0x082c)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:2	RW	0x000	memory_map11 memory map 11 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

CRYPTO_PKA_MEM_MAP12

Address: Operational Base + offset (0x0830)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:2	RW	0x000	memory_map12 memory map 12 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

CRYPTO_PKA_MEM_MAP13

Address: Operational Base + offset (0x0834)

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Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:2	RW	0x000	memory_map13 memory map 13 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

CRYPTO_PKA_MEM_MAP14

Address: Operational Base + offset (0x0838)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:2	RW	0x000	memory_map14 memory map 14 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

CRYPTO_PKA_MEM_MAP15

Address: Operational Base + offset (0x083c)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:2	RW	0x000	memory_map15 memory map 15 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

CRYPTO_PKA_MEM_MAP16

Address: Operational Base + offset (0x0840)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:2	RW	0x000	memory_map16 memory map 16 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

CRYPTO_PKA_MEM_MAP17

Address: Operational Base + offset (0x0844)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:2	RW	0x000	memory_map17 memory map 17 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

CRYPTO_PKA_MEM_MAP18

Address: Operational Base + offset (0x0848)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:2	RW	0x000	memory_map18 memory map 18 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

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CRYPTO_PKA_MEM_MAP19

Address: Operational Base + offset (0x084c)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:2	RW	0x000	memory_map19 memory map 19 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

CRYPTO_PKA_MEM_MAP20

Address: Operational Base + offset (0x0850)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:2	RW	0x000	memory_map20 memory map 20 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

CRYPTO_PKA_MEM_MAP21

Address: Operational Base + offset (0x0854)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:2	RW	0x000	memory_map21 memory map 21 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

CRYPTO_PKA_MEM_MAP22

Address: Operational Base + offset (0x0858)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:2	RW	0x000	memory_map22 memory map 22 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

CRYPTO_PKA_MEM_MAP23

Address: Operational Base + offset (0x085c)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:2	RW	0x000	memory_map23 memory map 23 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

CRYPTO_PKA_MEM_MAP24

Address: Operational Base + offset (0x0860)

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Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:2	RW	0x000	memory_map24 memory map 24 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

CRYPTO_PKA_MEM_MAP25

Address: Operational Base + offset (0x0864)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:2	RW	0x000	memory_map25 memory map 25 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

CRYPTO_PKA_MEM_MAP26

Address: Operational Base + offset (0x0868)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:2	RW	0x000	memory_map26 memory map 26 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

CRYPTO_PKA_MEM_MAP27

Address: Operational Base + offset (0x086c)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:2	RW	0x000	memory_map27 memory map 27 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

CRYPTO_PKA_MEM_MAP28

Address: Operational Base + offset (0x0870)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:2	RW	0x000	memory_map28 memory map 28 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

CRYPTO_PKA_MEM_MAP29

Address: Operational Base + offset (0x0874)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:2	RW	0x000	memory_map29 memory map 29 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

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CRYPTO_PKA_MEM_MAP30

Address: Operational Base + offset (0x0878)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:2	RW	0x000	memory_map30 memory map 30 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

CRYPTO_PKA_MEM_MAP31

Address: Operational Base + offset (0x087c)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:2	RW	0x000	memory_map31 memory map 30 [11:2], bit[1:0] is stuck to 0.
1:0	RO	0x0	reserved

CRYPTO_PKA_OPCODE

Address: Operational Base + offset (0x0880)

Bit	Attr	Reset Value	Description
31:27	WO	0x00	opcode Defines the PKA operation 0x04 Add,Inc 0x05 Sub,Dec,Neg 0x06 ModAdd,ModInc 0x07 ModSub,ModDec,ModNeg 0x08 AND,TST0,CLR0 0x09 OR,COPY,SET0 0xa XOR,FLIP0,INVERT,COMPARE 0xc SHR0 0xd SHR1 0xe SHL0 0xf SHL1 0x10 MulLow 0x11 ModMul 0x12 ModMulN 0x13 ModExp 0x14 Division 0x15 Div 0x16 ModDiv 0x00 Terminate

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Bit	Attr	Reset Value	Description
26:24	WO	0x0	len The virtual length address 0-7. Virtual address 0 point to PKA_L0. Virtual address 1 point to PKA_L1. ... Virtual address 7 point to PKA_L7.
23:18	WO	0x00	reg_a Operand A virtual address 0-15. Virtual address 0 point to PKA_MEM_MAP0. Virtual address 1 point to PKA_MEM_MAP1. ... Virtual address 15 point to PKA_MEM_MAP15.
17:12	WO	0x00	reg_b Operand B virtual address 0-15. Virtual address 0 point to PKA_MEM_MAP0. Virtual address 1 point to PKA_MEM_MAP1. ... Virtual address 15 point to PKA_MEM_MAP15.
11:6	WO	0x00	reg_r Result register virtual address 0-15. Virtual address 0 point to PKA_MEM_MAP0. Virtual address 1 point to PKA_MEM_MAP1. ... Virtual address 15 point to PKA_MEM_MAP15.
5:0	WO	0x00	tag Tag.

CRYPTO_N_NP_TO_T1_ADDR

Address: Operational Base + offset (0x0884)

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:15	RW	0x1f	reg_t1 Virtual address of temporary register number 1. Virtual address 0 point to PKA_MEM_MAP0. Virtual address 1 point to PKA_MEM_MAP1. ... Virtual address 15 point to PKA_MEM_MAP15.
14:10	RW	0x1e	reg_t0 Virtual address of temporary register number 0. Virtual address 0 point to PKA_MEM_MAP0. Virtual address 1 point to PKA_MEM_MAP1. ... Virtual address 15 point to PKA_MEM_MAP15.

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Bit	Attr	Reset Value	Description
9:5	RW	0x01	reg_np Virtual address of register np. Virtual address 0 point to PKA_MEM_MAP0. Virtual address 1 point to PKA_MEM_MAP1. ... Virtual address 15 point to PKA_MEM_MAP15.
4:0	RW	0x00	reg_n Virtual address of register n. Virtual address 0 point to PKA_MEM_MAP0. Virtual address 1 point to PKA_MEM_MAP1. ... Virtual address 15 point to PKA_MEM_MAP15.

CRYPTO_PKA_STATUS

Address: Operational Base + offset (0x0888)

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:14	RO	0x00	tag Tag of the Last Operation.
13:9	RO	0x00	opcode the last OPCODE.
8	RO	0x0	pka_cpu_busy PKA is busy memory control is by PKA.
7	RO	0x0	modinv_of_zero modular inverse of zero flag.
6	RO	0x0	alu_sign_out sign of the last operation(MSB).
5	RO	0x0	alu_carry Carry of the last ALU operation.
4	RO	0x0	div_by_zero Division by 0.
3	RO	0x0	alu_mod_ovflw Modular overflow flag.
2	RO	0x0	alu_out_zero ALU out is 0.
1	RO	0x0	pka_busy PKA is busy.
0	RO	0x1	pipe_is_busy PKA ready signal 0 : pipe full 1 : PKA ready for new command.

CRYPTO_PKA_SW_RESET

Address: Operational Base + offset (0x088c)

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Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	WO	0x0	pka_sw_reset PKA software reset the reset mechanism will take about four PKA clocks until the reset line is de-asserted.

CRYPTO_PKA_L0

Address: Operational Base + offset (0x0890)

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12:0	RW	0x0000	pka_l0 PKA length 0, in bit unit.

CRYPTO_PKA_L1

Address: Operational Base + offset (0x0894)

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12:0	RW	0x0000	pka_l1 PKA length 1, in bit unit.

CRYPTO_PKA_L2

Address: Operational Base + offset (0x0898)

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12:0	RW	0x0000	pka_l2 PKA length 2, in bit unit.

CRYPTO_PKA_L3

Address: Operational Base + offset (0x089c)

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12:0	RW	0x0000	pka_l3 PKA length 3, in bit unit.

CRYPTO_PKA_L4

Address: Operational Base + offset (0x08a0)

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12:0	RW	0x0000	pka_l4 PKA length 4, in bit unit.

CRYPTO_PKA_L5

Address: Operational Base + offset (0x08a4)

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Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12:0	RW	0x0000	pka_l5 PKA length 5, in bit unit.

CRYPTO_PKA_L6

Address: Operational Base + offset (0x08a8)

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12:0	RW	0x0000	pka_l6 PKA length 6, in bit unit.

CRYPTO_PKA_L7

Address: Operational Base + offset (0x08ac)

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12:0	RW	0x0000	pka_l7 PKA length 7, in bit unit.

CRYPTO_PKA_PIPE_RDY

Address: Operational Base + offset (0x08b0)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RO	0x1	pka_pipe_rdy PKA pipe is ready for new opcode

CRYPTO_PKA_DONE

Address: Operational Base + offset (0x08b4)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RO	0x1	pka_done PKA operation is completed and pipe is empty.

CRYPTO_PKA_MON_SELECT

Address: Operational Base + offset (0x08b8)

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3:0	RW	0x0	pka_mon_select PKA monitor select which PKA fsm monitor is being output.

CRYPTO_PKA_DEBUG_REG_EN

Address: Operational Base + offset (0x08bc)

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Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	pka_debug_reg_en Enable all the debug mechanism when set.

CRYPTO_DEBUG_CNT_ADDR

Address: Operational Base + offset (0x08c0)

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:0	R/WSC	0x00000	debug_cnt_addr The clock counter initial values. clock is disabled when counter expires. Triggered when pka_debug_en is set.

CRYPTO_DEBUG_EXT_ADDR

Address: Operational Base + offset (0x08c4)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	WO	0x0	debug_ext_addr Disable the debug Mechanism

CRYPTO_PKA_DEBUG_HALT

Address: Operational Base + offset (0x08c8)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RO	0x0	pka_debug_halt In debug mode: PKA is in halt state.

CRYPTO_PKA_MON_READ

Address: Operational Base + offset (0x08d0)

Bit	Attr	Reset Value	Description
31:0	RO	0x0000feef	pka_mon_read This is the PKA monitor bus register output.

CRYPTO_PKA_INT_ENA

Address: Operational Base + offset (0x08d4)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	pka_int_ena 1: enable pka interrupt. 0: disable pka interrupt

CRYPTO_PKA_INT_ST

Address: Operational Base + offset (0x08d8)

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Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	W1C	0x0	pka_int_st Indicate that PKA operation completes . After the bit is read, the application should write 1 to clear this bit for next time use.

CRYPTO_SRAM_ADDR

Address: Operational Base + offset (0x1000)

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	sram_addr Sram address starts from 0x1000 to 0x1fff. When RAM_CTL.ram_pka_rdy == 0, application could access sram. Otherwise, application can't .

9.4 Application Note

9.4.1 Clock & Reset

There are 4 clock domains in Crypto. The clock and reset signals are described in the following table .

Table 9-1 Crypto Clock & Reset Description

Signal	Attr	Description
hclk	clock	AHB clock
aclk	clock	AXI master clock
clk_core	clock	Cipher work clock
clk_pka	clock	PKA work clock
hresetn	reset	Asynchronously assert, synchronously de-assert to hclk, low active
aresetn	reset	Asynchronously assert, synchronously de-assert to aclk, low active
resetn_core	reset	Asynchronously assert, synchronously de-assert to clk_core, low active
resetn_pka	reset	Asynchronously assert, synchronously de-assert to clk_pka, low active

Each function need different clocks. The applications could gate the un-used clock to save power. Please see the following table for detail information.

Table 9-2 Crypto Clock & Reset Description

Operation	HCLK	ACLK	CLK_CORE	CLK_PKA
AES	ON	ON	ON	OFF
DES/TDES	ON	ON	ON	OFF
HASH/HMAC	ON	ON	ON	OFF
PKA	ON	OFF	OFF	ON
TRNG	ON	OFF	OFF	OFF

Even when CLK_CORE is on, Crypto is doing some cipher job. And Crypto could still be able to automatically gate most parts of un-used blocks to save more power, if CRYPTO_CLK_CTL.auto_clkgate_en is set to '1' . The default value for this bit is also '1' . Application could do a soft reset to a certain clock domain. Please refer to "Chapter CRU" for more details.

9.4.2 Performance

Cipher performance is shown in the following table.

Table 9-3 Crypto Performance Description

Algorithm	block size (Byte)	clk_core frequency (Mhz)	cycle	serial max throughput (MBps)	parallel max throughput (MBps)
DES	8	200	18	88	352
TDES	8	200	55	29	116
AES-128	16	200	12	266	1066
AES-192	16	200	14	228	914
AES-256	16	200	16	200	800
SHA-1	64	200	81	158	NA
MD5	64	200	65	196	NA
SHA-256/224	64	200	65	196	NA
SHA-512/384/ 512_224/ 512_256	128	200	81	316	NA

There are 2 column throughput rates in the table, 1 is serial mode, the other is parallel mode. In parallel mode, there are 4 engines working at the same time . So the speed is 4 times than serial mode. Parallel mode includes ECB/CTR/XTS both encryption and decryption mode, CFB/CBC/CTS only decryption mode. Other modes are serial. HASH doesn't have parallel mode.
For PKA, the cycles for each calculation are not certain. It depends on the parameters. Take RSA-2048 for example, it takes about 28M cycles to finish a calculation. PKA can run 300 Mhz. It means it can run over 10 times per second.

9.4.3 DMA

DMA supports Link List Item (LLI) DMA transaction.

- Each item contains 8 bytes, and start address should be 8 bytes align ;
- We suggest that DATA start address is 8 bytes align ;
- Total DATA length is byte align.
- Support segmenting HASH/HMAC DATA into multi sections. We suggest that each section DATA length is a multiple of 64 bytes, except this section is the last section.

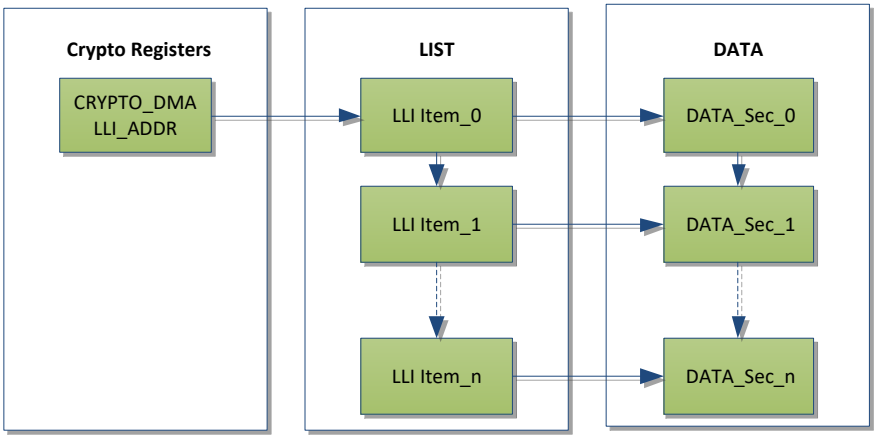


Fig. 9-2 LLI DMA Usage

As shown in the Figure above, Register CRYPTO_DMA_LLI_ADDR points to 1'st LLI item in external memory. Each LLI item contains DATA address, length, control information and next LLI item pointer, except the last LLI item. The last item doesn't have the next LLI Item pointer. After the last LLI item is finished , DMA will go to idle state.
LLI item definition is shown in the following table.

Table 9-4 LLI Item Description

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offset	Def	Description
0x00	SRC_ADDRESS[31:0]	source data start address
0x04	SRC_LENGTH[31:0]	source data length，in byte unit
0x08	DST_ADDRESS[31:0]	destination data start address
0x0c	DST_LENGTH[31:0]	destination data length，in byte unit
0x10	USER_DEFINE[31:0]	used in cipher block
0x14	reserve	reserve
0x18	DMA_CTRL[31:0]	used in DMA block
0x1c	next address[31:0]	next LLI item address. When DMA_CTRL.LAST = "1"，NEXT_ADDRESS is invalid.

DMA_CTRL: the definition is shown in the following table.

Table 9-5 LLI Item dma_ctl Description

Bit	Def	Definition
[31:24]	ITEM_ID[7:0]	used to identify LLI items.
[23:16]	reserve	
[15:11]	reserve	
10	source_item_done enable	When source data fetch is completed, CRYPTO_DMA_INT_ST.source_item_done will assert if this bit is set.
9	reserved	reserved
8	list_done enable	When all LLI items transfer is completed, CRYPTO_DMA_INT_ST.list_done will assert if this bit is set.
[7:2]	reserved	reserved
1	PAUSE	indicate DMA will hold on after executes current item. DMA won't go on unless CRYPTO_DMA_CTL.restart is configured
0	LAST	indicate current item is the last one. After executes current item, DMA will return to IDLE state.

Table 9-6 LLI Item user_define Description

Bit	Signal	Description
31:9	Reserved	Reserved
8	otpkey_sel	otpkey select. 1: select otpkey; 0: select register key
7	Privacy_sel	pkey select. 1: select pkey ; 0: select key ;
6:4	Chnl_num	channel number, from 0 to 7 .
3	String_attr	indicate current item's attribution. 0: ADA ; 1: PC(plaintext or ciphertext)
2	String_last	indicate current item is the string last item
1	String_start	indicate current item is the string first item
0	Cipher_start	indicate current item is the cipher first item

9.4.4 Multi-Channel Map

There are 8-channel configurations for AES or DES/TDES operation. For different key-size, the map is different. Please find the register map in the following table.

Table 9-7 LLI Item user_define Description

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Cipher sel	otpkey sel	privacy sel	chnl num	key	iv(tag/…)
AES-128/ DES	0	0	0	CH0_KEY0-3/ CH0_KEY0-1	CH0_IV0-3/ CH0_IV0-1
AES-128/ DES	0	0	n	CHn_KEY0-3/ CHn_KEY0-1	CHn_IV0-3/ CHn_IV0-1
AES-128/ DES	0	0	7	CH7_KEY0-3/ CH7_KEY0-1	CH7_IV0-3/ CH7_IV0-1
AES-128/ DES	0	1	0	CH0_PKEY0-3/ CH0_PKEY0-1	CH0_IV0-3/ CH0_IV0-1
AES-128/ DES	0	1	n	CHn_PKEY0-3/ CHn_PKEY0-1	CHn_IV0-3/ CHn_IV0-1
AES-128/ DES	0	1	7	CH7_PKEY0-3/ CH7_PKEY0-1	CH7_IV0-3/ CH7_IV0-1
AES-128/ DES	1	NA	0	OTP_KEY[255:128]	CH0_IV0-3/ CH0_IV0-1
AES-128/ DES	1	NA	n	OTP_KEY[127:0]	CHn_IV0-3/ CHn_IV0-1
AES-128/ DES	1	NA	7	OTP_KEY[127:0]	CH7_IV0-3/ CH7_IV0-1
AES-192/ TDES	0	0	0	CH0_KEY0-3, CH1_KEY0-1	CH0_IV0-3/ CH0_IV0-1
AES-192/ TDES	0	0	1	CH2_KEY0-3, CH3_KEY0-1	CH1_IV0-3/ CH1_IV0-1
AES-192/ TDES	0	0	2	CH4_KEY0-3, CH5_KEY0-1	CH2_IV0-3/ CH2_IV0-1
AES-192/ TDES	0	0	3	CH6_KEY0-3, CH7_KEY0-1	CH3_IV0-3/ CH3_IV0-1
AES-192/ TDES	0	1	0	CH0_PKEY0-3, CH1_PKEY0-1	CH0_IV0-3/ CH0_IV0-1
AES-192/ TDES	0	1	1	CH2_PKEY0-3, CH3_PKEY0-1	CH1_IV0-3/ CH1_IV0-1
AES-192/ TDES	0	1	2	CH4_PKEY0-3, CH5_PKEY0-1	CH2_IV0-3/ CH2_IV0-1
AES-192/ TDES	0	1	3	CH6_PKEY0-3, CH7_PKEY0-1	CH3_IV0-3/ CH3_IV0-1
AES-192/ TDES	0	NA	4-7	not supported	not supported
AES-192/ TDES	1	NA	0	OTP[255:64]	CH0_IV0-3/ CH0_IV0-1
AES-192/ TDES	1	NA	1-7	not supported	not supported
AES-256	0	0	0	CH0_KEY0-3, CH1_KEY0-3	CH0_IV0-3/ CH0_IV0-1
AES-256	0	0	1	CH2_KEY0-3, CH3_KEY0-3	CH1_IV0-3/ CH1_IV0-1

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Cipher sel	otpkey sel	privacy sel	chnl num	key	iv(tag/…)
AES-256	0	0	2	CH4_KEY0-3, CH5_KEY0-3	CH2_IV0-3/ CH2_IV0-1
AES-256	0	0	3	CH6_KEY0-3, CH7_KEY0-3	CH3_IV0-3/ CH3_IV0-1
AES-256	0	1	0	CH0_PKEY0-3, CH1_PKEY0-3	CH0_IV0-3/ CH0_IV0-1
AES-256	0	1	1	CH2_PKEY0-3, CH3_PKEY0-3	CH1_IV0-3/ CH1_IV0-1
AES-256	0	1	2	CH4_PKEY0-3, CH5_PKEY0-3	CH2_IV0-3/ CH2_IV0-1
AES-256	0	1	3	CH6_PKEY0-3, CH7_PKEY0-3	CH3_IV0-3/ CH3_IV0-1
AES-256	0	NA	4-7	not supported	not supported
AES-256	1	NA	0	OTP[255:0]	CH0_IV0-3/ CH0_IV0-1
AES-256	1	NA	1-7	not supported	not supported

In AES-XTS mode, there are 2 keys, and only AES-128 and AES-256 mode are. Please refer to the following table for detail information.

Table 9-8 LLI Item user_define Description

Cipher sel	otpkey sel	privacy sel	chnl num	key1	key2	tweak
AES-128	0	0	0	CH0_KEY0-3	CH4_KEY0-3	CH0_IV0-3
AES-128	0	0	1	CH1_KEY0-3	CH5_KEY0-3	CH1_IV0-3
AES-128	0	0	2	CH2_KEY0-3	CH6_KEY0-3	CH2_IV0-3
AES-128	0	0	3	CH3_KEY0-3	CH7_KEY0-3	CH3_IV0-3
AES-128	0	1	0	CH0_PKEY0-3	CH4_PKEY0-3	CH0_IV0-3
AES-128	0	1	1	CH1_PKEY0-3	CH5_PKEY0-3	CH1_IV0-3
AES-128	0	1	2	CH2_PKEY0-3	CH6_PKEY0-3	CH2_IV0-3
AES-128	0	1	3	CH3_PKEY0-3	CH7_PKEY0-3	CH3_IV0-3
AES-128	0	NA	4-7	not supported	not supported	not supported
AES-128	1	NA	NA	not supported	not supported	not supported
AES-256	0	0	0	CH0_KEY0-3, CH1_KEY0-3	CH4_KEY0-CH5_KEY3	CH0_IV0-3
AES-256	0	0	1	CH2_KEY0-3, CH3_KEY0-3	CH6_KEY0-CH7_KEY3	CH1_IV0-3
AES-256	0	1	0	CH0_PKEY0-3, CH1_PKEY0-3	CH4_PKEY0-CH5_PKEY3	CH0_IV0-3
AES-256	0	1	1	CH2_PKEY0-3, CH3_PKEY0-3	CH6_PKEY0-CH7_PKEY3	CH1_IV0-3
AES-256	0	NA	2-7	not supported	not supported	not supported

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Cipher sel	otpkey sel	privacy sel	chnl num	key1	key2	tweak
AES-256	1	NA	NA	not supported	not supported	not supported

Note: The difference between CHn_KEY and CHn_PKEY is that: CHn_KEY could be read/write, CHn_PKEY could be write , but can't be read . The read value for CHn_PKEY is all '0'.

9.4.5 HASH Data Path

HASH and AES could run in parallel way. There are 2 paths lead to AES-HASH function. One is AES-HASH-RX mode, the other is AES-HASH-TX mode.

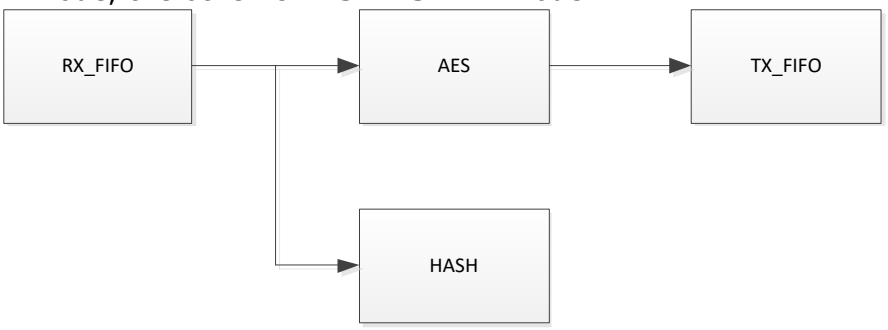


Fig. 9-3 AES-HASH-RX mode

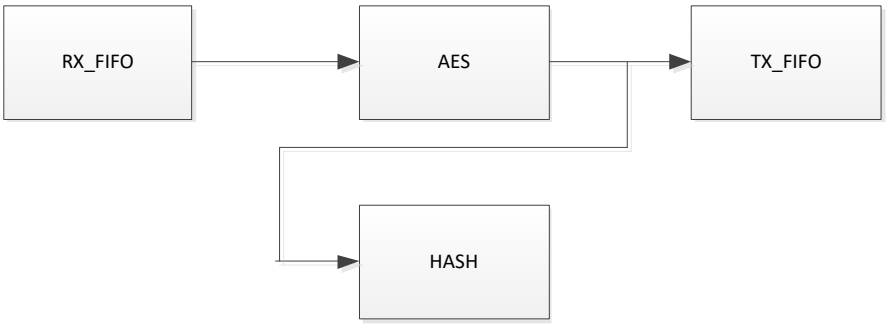


Fig. 9-4 AES-HASH-TX mode

As shown in the figures above, we could facilitate operations in some cases. For example, secure boot, we need both AES and HASH operations for the same blocks of data. The data HASH gets from RX_FIFO or TX_FIFO is byteswaped if the byteswap function is configured.

9.4.6 Program Steps

The application could succeed various crypto operations if they program properly.

- Program the LLI address to DMA_LLI_ADDR;
- Program KEY , IV, or other parameter if needed ;
- Program BC_CTL or HASH_CTL for control information;
- Prepare LLI Item;
- Enable interrupt, or do nothing.

All these operations could be in any order.

- Program DMA_CTL.start to start the operation;

This step should be the last configuration step. After this register is configured, other registers should not be changed.

- Wait interrupt asserted, or just poll the DMA_INT_ST bits .
- Program DMA_INT_ST to clear interrupt status, and get the result.

The application could also use LLI.pause when the next LLI item is not ready. After the new item is prepared, the application could program DMA_CTL.restart to continue previous operation.

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Chapter 10 USB2.0 Host

10.1 Overview

USB2.0 host controller supports fully USB2.0 functions with one EHCI host controller and one OHCI host controller, and each host controller has one USB port. OHCI host controller only supports full-speed and low-speed mode and is used for full-speed devices and low-speed devices. EHCI only supports high-speed mode and is used for high-speed devices. OHCI host controller and EHCI host controller shares the same USB port, EHCI host controller will auto select the owner (OHCI or EHCI) of this USB port depending on the speed mode of attached devices, when selecting OHCI as owner, OHCI host controller will serve for the attached device; when selecting EHCI as owner, EHCI host controller will serve for the attached device.

USB2.0 Host Controller supports the following features:

- Compatible Specifications
  - Universal Serial Bus Specification, Revision 2.0
  - Enhanced Host Controller Interface Specification (EHCI), Revision 1.0
  - Open Host Controller Interface Specification (OHCI), Revision 1.0a
- Support High-speed (480Mbps), Full-speed (12Mbps) and Low-speed (1.5Mbps)

10.2 Block Diagram

USB2.0 Host Controller comprises with:

- EHCI Host Controller: Perform High-speed transactions
- OHCI Host Controller: Perform full/low-speed transactions
- Port Routing Control: Select EHCI Host Controller or OHCI Host Controller

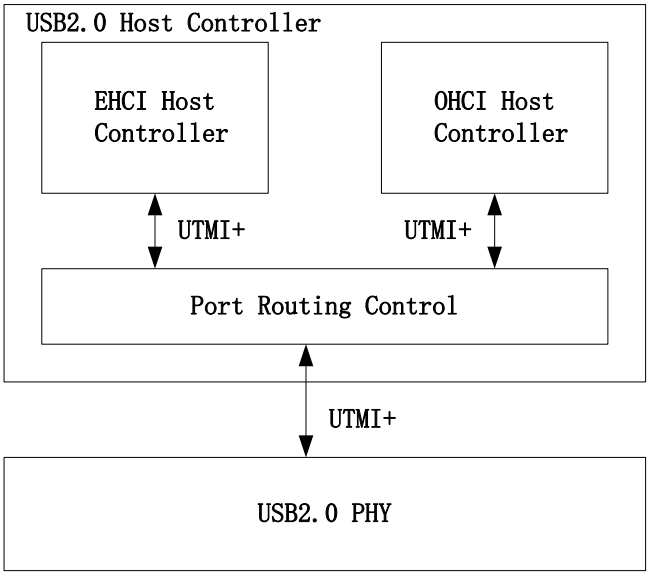


Fig. 10-1USB2.0 Host Controller Block Diagram

10.3 Function Description

10.3.1 EHCI Host Controller

It performs descriptors and data read or write from or to system memory and packs or un-pack USB transactions from or to UTMI+ interface defined in EHCI specification for high-speed data transmission.

10.3.2 OHCI Host Controller

It performs descriptors and data read/write from/to system memory and packs or un-pack USB transactions from or to UTMI+ interface defined in OHCI specification for full-speed or low-speed data transmission.

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10.3.3 Port Routing Control

As part of logic in the EHCI host controller, it is used to auto-select EHCI or OHCI host controller to serve the attached device depending on the speed of the attached device.

10.4 Register Description

10.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

Table 10-1USB2.0 Host Controller Address Mapping

Base Address[16]	Device	Address Length	Offset Address Range
1'b0	EHCI	64K BYTE	0x00000 ~ 0x0ffff
1'b1	OHCI	64K BYTE	0x10000 ~ 0x1ffff

EHCI and OHCI register definitions, please refer to Enhanced Host Controller Interface Specification (EHCI), Revision 1.0 and Open Host Controller Interface Specification (OHCI), Revision 1.0a.

10.5 Interface Description

Table 10-2 USB2.0 PHY Interface Description

Module Pin	Direction	Pad Name	Descriptions
USB0ID	I	IO_USB0_ID	USB2.0 PHY OTG Port ID, left unused for TypeC
USB0PN	I/O	IO_USB0_PN	USB2.0 PHY OTG Port PN
USB0PP	I/O	IO_USB0_PP	USB2.0 PHY OTG Port PP
VBUS	I	IO_USB0_VBUS	USB2.0 PHY OTG Port VBUS
USB1PN	I/O	IO_USB1_PN	USB2.0 PHY Host Port PN
USB1PP	I/O	IO_USB1_PP	USB2.0 PHY Host Port PP
USBRBIAS	I/O	IO_USB0_RBIAS	USB2.0 PHY Shared RBIAS

10.6 Application Notes

10.6.1 Special Setting

10.6.2 Program flow

Please refer to Enhanced Host Controller Interface Specification (EHCI), Revision 1.0 and Open Host Controller Interface Specification (OHCI), Revision 1.0a.

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Chapter 11 USB OTG2.0

11.1 Overview

USB OTG 2.0 is a Dual-Role Device controller, which supports both device and host functions and is fully compliant with OTG Supplement to USB2.0 specification and support high-speed (480Mbps), full-speed (12Mbps), low-speed (1.5Mbps) transfer.
USB OTG 2.0 is optimized for portable electronic devices, point-to-point applications (no hub, direct connection to device) and multi-point applications to devices.

11.1.1 Features

- Compliant with the OTG Supplement to the USB2.0 Specification
- Operates in High-Speed, Full-Speed and Low-Speed mode (host mode only)
- Support 9 channels in host mode
- 9 Device mode endpoints in addition to control endpoint 0, 4 in, 3 out and 2 IN/OUT
- Built-in one 1024x35 bits FIFO
- Internal DMA with scatter/gather function
- Supports packet-based, dynamic FIFO memory allocation for endpoints for flexible, efficient use of RAM
- Support dynamic FIFO sizing

11.2 Block Diagram

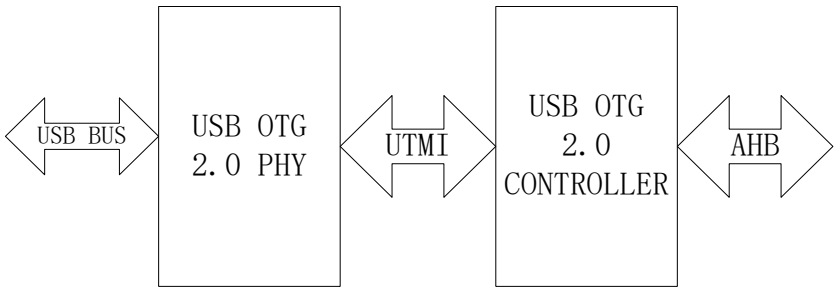


Fig. 11-1 USB OTG 2.0 Architecture

The Fig shows the architecture of USB OTG 2.0. It is broken up into two separate units: USB OTG 2.0 controller and USB OTG 2.0 PHY. The two units are interconnected with UTMI interface.

11.3 USB OTG 2.0 Controller

The USB OTG 2.0 Controller can active as USB2.0 host controller or USB2.0 device controller basing on ID status of Micron-AB receptacle.
As USB2.0 host controller, it uses one transmit FIFO for all non-periodic out transactions and one transmit FIFO for all periodic out transactions as transmit buffers to hold the data to be transmitted over USB, and use one receive FIFO for all periodic and non-periodic transactions to hold the received data from the USB until it is transferred to the system memory by DMA.
As USB2.0 device controller, it also use a single receive FIFO to receive the data for all the out endpoints from USB, and individual transmit FIFOs for each IN endpoint.

11.4 USB OTG 2.0 PHY

The USB OTG 2.0 PHY handles the low level USB protocol and signaling from controller and differential pairs. It includes functions such as data serialization and de-serialization, bit stuffing and clock recovery and synchronization. Its feature contains:

- provide dual UTMI ports
- OTG0 Support UART Bypass Function
- Fully compliant with USB specifications Rev 2.0
- Supports 480Mbps (HS), 12Mbps (FS) & 1.5Mbps(LS) serial data transmission

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- Supports low latency hub mode with 40 bit time around trip delay
- 8 bit or 16 bit UTMI interface compliant with UTMI+ specification level 3 Rev 1.
- Loop back BIST mode supported
- Built-in I/O and ESD structure
- On-die self-calibrated HS/FS/LS termination
- 24MHz crystal oscillator with integrated phase-locked loop (PLL) oscillator
- Dual 3.3V / 1.2V supply

11.5 UART BYPASS FUNCITON

UART bypass mode is used for software team debugging by transmitting UART signals over USB differential pairs. When in UART bypass mode, UART2 can transmit UART protocol signals over USB differential pairs and USB is not functional; Otherwise, UART2 use normal UART interface and USB is functional.

11.6 Register Description

11.6.1 Register Summary

Name	Offset	Size	Reset Value	Description
USBOTG_GOTGCTL	0x0000	W	0x00000000	Control and Status Register
USBOTG_GOTGINT	0x0004	W	0x00000000	Interrupt Register
USBOTG_GAHBCFG	0x0008	W	0x00000000	AHB Configuration Register
USBOTG_GUSBCFG	0x000c	W	0x00001400	USB Configuration Register
USBOTG_GRSTCTL	0x0010	W	0x80000000	Reset Register
USBOTG_GINTSTS	0x0014	W	0x00000000	Interrupt Register
USBOTG_GINTMSK	0x0018	W	0x00000000	Interrupt Mask Register
USBOTG_GRXSTSR	0x001c	W	0x00000000	Receive Status Debug Read Register
USBOTG_GRXSTSP	0x0020	W	0x00000000	Receive Status Read and Pop Register
USBOTG_GRXFSIZ	0x0024	W	0x00000000	Receive FIFO Size Register
USBOTG_GNPTXFSIZ	0x0028	W	0x00000000	Non-Periodic Transmit FIFO Size Register
USBOTG_GNPTXSTS	0x002c	W	0x00000000	Non-Periodic Transmit FIFO/Queue Status Register
USBOTG_GI2CCTL	0x0030	W	0x11000000	I2C Address Register
USBOTG_GPVNDCTL	0x0034	W	0x00000000	PHY Vendor Control Register
USBOTG_GGPIO	0x0038	W	0x00000000	General Purpost Input/Output Register
USBOTG_GUID	0x003c	W	0x00000000	User ID Register
USBOTG_GSNPSID	0x0040	W	0x00004f54	Core ID Register
USBOTG_GHWCFG1	0x0044	W	0x00000000	User HW Config1 Register
USBOTG_GHWCFG2	0x0048	W	0x00000000	User HW Config2 Register
USBOTG_GHWCFG3	0x004c	W	0x00000000	User HW Config3 Register
USBOTG_GHWCFG4	0x0050	W	0x00000000	User HW Config4 Register
USBOTG_GLPMCFG	0x0054	W	0x00000000	Core LPM Configuration Register
USBOTG_GPWRDN	0x0058	W	0x00000000	Global Power Down Register

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Name	Offset	Size	Reset Value	Description
USBOTG_GDFIFOCFG	0x005c	W	0x00000000	Global DFIFO Software Config Register
USBOTG_GADPCTL	0x0060	W	0x00000000	ADP Timer,Control and Status Register
USBOTG_HPTXFSIZ	0x0100	W	0x00000000	Host Periodic Transmit FIFO Size Register
USBOTG_DIEPTXFn	0x0104	W	0x00000000	Device Periodic Transmit FIFO-n Size Register
USBOTG_HCFG	0x0400	W	0x00000000	Host Configuration Register
USBOTG_HFIR	0x0404	W	0x00000000	Host Frame Interval Register
USBOTG_HFNUM	0x0408	W	0x0000ffff	Host Frame Number/Frame Time Remaining Register
USBOTG_HPTXSTS	0x0410	W	0x00000000	Host Periodic Transmit FIFO/Queue Status Register
USBOTG_HAINT	0x0414	W	0x00000000	Host All Channels Interrupt Register
USBOTG_HAINTMSK	0x0418	W	0x00000000	Host All Channels Interrupt Mask Register
USBOTG_HPRT	0x0440	W	0x00000000	Host Port Control and Status Register
USBOTG_HCCHARn	0x0500	W	0x00000000	Host Channel-n Characteristics Register
USBOTG_HCSPLTn	0x0504	W	0x00000000	Host Channel-n Split Control Register
USBOTG_HCINTn	0x0508	W	0x00000000	Host Channel-n Interrupt Register
USBOTG_HCINTMSKn	0x050c	W	0x00000000	Host Channel-n Interrupt Mask Register
USBOTG_HCTSIZn	0x0510	W	0x00000000	Host Channel-n Transfer Size Register
USBOTG_HCDMAn	0x0514	W	0x00000000	Host Channel-n DMA Address Register
USBOTG_HCDMABn	0x051c	W	0x00000000	Host Channel-n DMA Buffer Address Register
USBOTG_DCFG	0x0800	W	0x08200000	Device Configuration Register
USBOTG_DCTL	0x0804	W	0x00002000	Device Control Register
USBOTG_DSTS	0x0808	W	0x00000000	Device Status Register
USBOTG_DIEPMSK	0x0810	W	0x00000000	Device IN Endpoint common interrupt mask register
USBOTG_DOEPMSK	0x0814	W	0x00000000	Device OUT Endpoint common interrupt mask register
USBOTG_DAINT	0x0818	W	0x00000000	Device All Endpoints interrupt register

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Name	Offset	Size	Reset Value	Description
USBOTG_DAINTMSK	0x081c	W	0x00000000	Device All Endpoint interrupt mask register
USBOTG_DTKNQR1	0x0820	W	0x00000000	Device IN token sequence learning queue read register1
USBOTG_DTKNQR2	0x0824	W	0x00000000	Device IN token sequence learning queue read register2
USBOTG_DVBUSDIS	0x0828	W	0x00000b8f	Device VBUS discharge time register
USBOTG_DVBUSPULSE	0x082c	W	0x00000000	Device VBUS Pulsing Timer Register
USBOTG_DTHRCTL	0x0830	W	0x08100020	Device Threshold Control Register
USBOTG_DIEPEMPMSK	0x0834	W	0x00000000	Device IN endpoint FIFO empty interrupt mask register
USBOTG_DEACHINT	0x0838	W	0x00000000	Device each endpoint interrupt register
USBOTG_DEACHINTMSK	0x083c	W	0x00000000	Device each endpoint interrupt register mask
USBOTG_DIEPEACHMSKn	0x0840	W	0x00000000	Device each IN endpoint -n interrupt Register
USBOTG_DOEPEACHMSKn	0x0880	W	0x00000000	Device each out endpoint-n interrupt register
USBOTG_DIEPCTL0	0x0900	W	0x00008000	Device control IN endpoint 0 control register
USBOTG_DIEPINTn	0x0908	W	0x00000000	Device Endpoint-n Interrupt Register
USBOTG_DIEPTSIZn	0x0910	W	0x00000000	Device endpoint n transfer size register
USBOTG_DIEPDMAn	0x0914	W	0x00000000	Device endpoint-n DMA address register
USBOTG_DTXFSTSn	0x0918	W	0x00000000	Device IN endpoint transmit FIFO status register
USBOTG_DIEPDMABn	0x091c	W	0x00000000	Device endpoint-n DMA buffer address register
USBOTG_DIEPCTLn	0x0920	W	0x00000000	Device endpoint-n control register
USBOTG_DOEPCTL0	0x0b00	W	0x00000000	Device control OUT endpoint 0 control register
USBOTG_DOEPINTn	0x0b08	W	0x00000000	Device endpoint-n control register
USBOTG_DOEPTSIZn	0x0b10	W	0x00000000	Device endpoint n transfer size register
USBOTG_DOEPDMAn	0x0b14	W	0x00000000	Device Endpoint-n DMA Address Register
USBOTG_DOEPDMABn	0x0b1c	W	0x00000000	Device endpoint-n DMA buffer address register

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Name	Offset	Size	Reset Value	Description
USBOTG_DOEPCTLn	0x0b20	W	0x00000000	Device endpoint-n control register
USBOTG_PCGCR	0x0b24	W	0x200b8000	Power and clock gating control register
USBOTG_EPBUF0	0x1000	W	0x00000000	Device endpoint 0 / host out channel 0 address
USBOTG_EPBUF1	0x2000	W	0x00000000	Device endpoint 1 / host out channel 1 address
USBOTG_EPBUF2	0x3000	W	0x00000000	Device endpoint 2 / host out channel 2 address
USBOTG_EPBUF3	0x4000	W	0x00000000	Device endpoint 3 / host out channel 3 address
USBOTG_EPBUF4	0x5000	W	0x00000000	Device endpoint 4 / host out channel 4 address
USBOTG_EPBUF5	0x6000	W	0x00000000	Device endpoint 5 / host out channel 5 address
USBOTG_EPBUF6	0x7000	W	0x00000000	Device endpoint 6 / host out channel 6 address
USBOTG_EPBUF7	0x8000	W	0x00000000	Device endpoint 7 / host out channel 7 address

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

11.6.2 Detail Register Description

USBOTG_GOTGCTL

Address: Operational Base + offset (0x0000)
Control and Status Register

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27	RW	0x0	ChirpEn Chirp on enable This bit when programmed to 1'b1 results in the core asserting chirp_on before sending an actual Chirp "K" signal on USB. This bit is present only if OTG_BC_SUPPORT = 1. If OTG_BC_SUPPORT != 1, this bit is a reserved bit.
26:22	RO	0x00	MultValidBc Multi Valued ID pin Battery Charger ACA inputs in the following order: Bit 26 - rid_float. Bit 25 - rid_gnd Bit 24 - rid_a Bit 23 - rid_b Bit 22 - rid_c These bits are present only if OTG_BC_SUPPORT = 1. Otherwise, these bits are reserved and will read 5'h0.
21	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
20	RW	0x0	OTGVer OTG version Indicates the OTG revision. 0: OTG Version 1.3. In this version the core supports Data line pulsing and VBus pulsing for SRP. 1: OTG Version 2.0. In this version the core supports only Data line pulsing for SRP.
19	RO	0x0	BSesVld B-session valid Indicates the Device mode transceiver status. 0: B-session is not valid. 1: B-session is valid. In OTG mode, you can use this bit to determine if the device is connected or disconnected. Note: If you do not enabled OTG features (such as SRP and HNP), the read reset value will be 1.The vbus assigns the values internally for non-SRP or non-HNP configurations.
18	RO	0x0	ASesVld A-session valid Indicates the Host mode transceiver status. 0: A-session is not valid 1: A-session is valid Note: If you do not enabled OTG features (such as SRP and HNP), the read reset value will be 1.The vbus assigns the values internally for non-SRP or non-HNP configurations.
17	RO	0x0	DbnTime Long/short debounce time Indicates the debounce time of a detected connection. 0: Long debounce time, used for physical connections (100 ms + 2.5 us) 1: Short debounce time, used for soft connections (2.5 us)
16	RO	0x0	ConIDSts Connector ID Status Indicates the connector ID status on a connect event. 0: The core is in A-Device mode 1: The core is in B-Device mode
15:12	RO	0x0	reserved
11	RW	0x0	DevHNPEn Device HNP Enable The application sets this bit when it successfully receives a SetFeature. SetHNPEnable command from the connected USB host. 0: HNP is not enabled in the application 1: HNP is enabled in the application

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Bit	Attr	Reset Value	Description
10	RW	0x0	HstSetHNPEn Host set HNP enable The application sets this bit when it has successfully enabled HNP (using the SetFeature.SetHNPEnable command) on the connected device. 0: Host Set HNP is not enabled 1: Host Set HNP is enabled
9	RW	0x0	HNPReq HNP request The application sets this bit to initiate an HNP request to the connected USB host. The application can clear this bit by writing a 0 when the Host Negotiation Success Status Change bit in the OTG Interrupt register (GOTGINT.HstNegSucStsChng) is set. The core clears this bit when the HstNegSucStsChng bit is cleared. 0: No HNP request 1: HNP request
8	RO	0x0	HstNegScs Host Negotiation Success The core sets this bit when host negotiation is successful. The core clears this bit when the HNP Request (HNPReq) bit in this register is set. 0: Host negotiation failure 1: Host negotiation success
7:2	RO	0x0	reserved
1	RW	0x0	SesReq Session Request The application sets this bit to initiate a session request on the USB. The application can clear this bit by writing a 0 when the Host Negotiation Success Status Change bit in the OTG Interrupt register (GOTGINT.HstNegSucStsChng) is set. The core clears this bit when the HstNegSucStsChng bit is cleared. If you use the USB 1.1 Full-Speed Serial Transceiver interface to initiate the session request, the application must wait until the VBUS discharges to 0.2 V, after the B-Session Valid bit in this register (GOTGCTL.BSesVld) is cleared. This discharge time varies between different PHYs and can be obtained from the PHY vendor. 0: No session request 1: Session request
0	RO	0x0	SesReqScs Session Request Success The core sets this bit when a session request initiation is successful. 0: Session request failure 1: Session request success

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USBOTG_GOTGINT
Address: Operational Base + offset (0x0004)
Interrupt Register

Bit	Attr	Reset Value	Description
31:21	RO	0x0	reserved
20	W1C	0x0	MultiValueChg Multi-Valued input changed This bit when set indicates that there is a change in the value of at least one ACA pin value. This bit is present only if OTG_BC_SUPPORT = 1, otherwise it is reserved.
19	W1C	0x0	DbnceDone Debounce Done The core sets this bit when the debounce is completed after the device connected. The application can start driving USB reset after seeing this interrupt. This bit is only valid when the HNP Capable or SRP Capable bit is set in the Core USB Configuration register (GUSBCFG.HNPCap or GUSBCFG.SRPCap, respectively).
18	W1C	0x0	ADevTOUTChg A-Device Timeout Change The core sets this bit to indicate that the A-device has timed out while waiting for the B-device to connect.
17	W1C	0x0	HstNegDet Host Negotiation Detected The core sets this bit when it detects a host negotiation request on the USB
16:10	RO	0x0	reserved
9	W1C	0x0	HstNegSucStsChng Host Negotiation Success Status Change The core sets this bit on the success or failure of a USB host negotiation request. The application must read the Host Negotiation Success bit of the OTG Control and Status register (GOTGCTL.HstNegScs) to check for success or failure
8	W1C	0x0	SesReqSucStsChng Session Request Success Status Change The core sets this bit on the success or failure of a session request.The application must read the Session Request Success bit in the OTG Control and Status register (GOTGCTL.SesReqScs) to check for success or failure.
7:3	RO	0x0	reserved
2	W1C	0x0	SesEndDet Session End Detected The core sets this bit when the utmisrp_bvalid signal is deasserted
1:0	RO	0x0	reserved

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USBOTG_GAHBCFG
Address: Operational Base + offset (0x0008)
AHB Configuration Register

Bit	Attr	Reset Value	Description
31:23	RO	0x0	reserved
22	RW	0x0	NotiAllDmaWrit Notify All Dma Write Transactions This bit is programmed to enable the System DMA Done functionality for all the DMA write Transactions corresponding to the Channel/Endpoint. This bit is valid only when GAHBCFG.RemMemSupp is set to 1. GAHBCFG.NotiAllDmaWrit = 1. HSOTG core asserts int_dma_req for all the DMA write transactions on the AHB interface along with int_dma_done, chep_last_transact and chep_number signal informations. The core waits for sys_dma_done signal for all the DMA write transactions in order to complete the transfer of a particular Channel/Endpoint. GAHBCFG.NotiAllDmaWrit = 0. HSOTG core asserts int_dma_req signal only for the last transaction of DMA write transfer corresponding to a particular Channel/Endpoint. Similarly, the core waits for sys_dma_done signal only for that transaction of DMA write to complete the transfer of a particular Channel/Endpoint.
21	RW	0x0	RemMemSupp Remote Memory Support This bit is programmed to enable the functionality to wait for the system DMA Done Signal for the DMA Write Transfers. GAHBCFG.RemMemSupp=1. The int_dma_req output signal is asserted when HSOTG DMA starts write transfer to the external memory. When the core is done with the Transfers it asserts int_dma_done signal to flag the completion of DMA writes from HSOTG. The core then waits for sys_dma_done signal from the system to proceed further and complete the Data Transfer corresponding to a particular Channel/Endpoint. GAHBCFG.RemMemSupp=0. The int_dma_req and int_dma_done signals are not asserted and the core proceeds with the assertion of the XferComp interrupt as soon as the DMA write transfer is done at the HSOTG Core Boundary and it does not wait for the sys_dma_done signal to complete the DATA transfers.
20:9	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
8	RW	0x0	PTxFEmpLvl Periodic TxFIFO Empty Level Indicates when the Periodic TxFIFO Empty Interrupt bit in the Core Interrupt register (GINTSTS.PTxFEmp) is triggered. This bit is used only in Slave mode. 0: GINTSTS.PTxFEmp interrupt indicates that the Periodic TxFIFO is half empty 1: GINTSTS.PTxFEmp interrupt indicates that the Periodic TxFIFO is completely empty
7	RW	0x0	NPTxFEmpLvl Non-Periodic TxFIFO Empty Level This bit is used only in Slave mode. In host mode and with Shared FIFO with device mode, this bit indicates when the Non-Periodic TxFIFO Empty Interrupt bit in the Core Interrupt register GINTSTS.NPTxFEmp) is triggered. With dedicated FIFO in device mode, this bit indicates when IN endpoint Transmit FIFO empty interrupt (DIEPINTn.TxFEmp) is triggered. Host mode and with Shared FIFO with device mode: 1'b0: GINTSTS.NPTxFEmp interrupt indicates that the Non-Periodic TxFIFO is half empty 1'b1: GINTSTS.NPTxFEmp interrupt indicates that the Non-Periodic TxFIFO is completely empty Dedicated FIFO in device mode: 1'b0: DIEPINTn.TxFEmp interrupt indicates that the IN Endpoint TxFIFO is half empty 1'b1: DIEPINTn.TxFEmp interrupt indicates that the IN Endpoint TxFIFO is completely empty
6	RO	0x0	reserved
5	RW	0x0	DMAEn DMA Enable 0: Core operates in Slave mode 1: Core operates in a DMA mode This bit is always 0 when Slave-Only mode has been selected.

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Bit	Attr	Reset Value	Description
4:1	RW	0x0	HBstLen Burst Length/Type This field is used in both External and Internal DMA modes. In External DMA mode, these bits appear on dma_burst[3:0] ports, External DMA Mode defines the DMA burst length in terms of 32-bit words: 4'b0000: 1 word 4'b0001: 4 words 4'b0010: 8 words 4'b0011: 16 words 4'b0100: 32 words 4'b0101: 64 words 4'b0110: 128 words 4'b0111: 256 words Others: Reserved Internal DMA Mode AHB Master burst type: 4'b0000: Single 4'b0001: INCR 4'b0011: INCR4 4'b0101: INCR8 4'b0111: INCR16 Others: Reserved
0	RW	0x0	GlblIntrMsk Global Interrupt Mask The application uses this bit to mask or unmask the interrupt line assertion by itself. Irrespective of this bit's setting, the interrupt status registers are updated by the core. 1'b0: Mask the interrupt assertion to the application. 1'b1: Unmask the interrupt assertion to the application.

USBOTG_GUSBCFG

Address: Operational Base + offset (0x000c)

USB Configuration Register

Bit	Attr	Reset Value	Description
31	RW	0x0	CorruptTxpacket Corrupt Tx packet This bit is for debug purposes only. Never set this bit to 1.

Bit	Attr	Reset Value	Description
30	RW	0x0	ForceDevMode Force Device Mode Writing a 1 to this bit forces the core to device mode irrespective of utmiotg_iddig input pin. 1'b0: Normal Mode 1'b1: Force Device Mode After setting the force bit, the application must wait at least 25 ms before the change to take effect. When the simulation is in scale down mode, waiting for 500 us is sufficient. This bit is valid only when OTG_MODE = 0, 1 or 2. In all other cases, this bit reads 0.
29	RW	0x0	ForceHstMode Force Host Mode Writing a 1 to this bit forces the core to host mode irrespective of utmiotg_iddig input pin. 1'b0: Normal Mode 1'b1: Force Host Mode After setting the force bit, the application must wait at least 25 ms before the change to take effect. When the simulation is in scale down mode, waiting for 500 us is sufficient. This bit is valid only when OTG_MODE =0, 1 or 2. In allother cases, this bit reads 0.
28	RW	0x0	TxEndDelay Tx End Delay Writing a 1 to this bit enables the TxEndDelay timers in the core. 1'b0: Normal mode 1'b1: Introduce Tx end delay timers
27	RW	0x0	IC_USBTrafCtl IC_USB TrafficPullRemove Control When this bit is set, pullup/pulldown resistors are detached from the USB during traffic signaling.This bit is valid only when configuration parameter OTG_ENABLE_IC_USB = 1 and register field GUSBCFG.IC_USBCap is set to 1.
26	RW	0x0	IC_USBCap IC_USB-Capable The application uses this bit to control the IC_USB capabilities. 1'b0: IC_USB PHY Interface is not selected. 1'b1: IC_USB PHY Interface is selected. This bit is writable only if OTG_ENABLE_IC_USB=1 and OTG_FSPHY_INTERFACE!=0.The reset value depends on the configuration parameter OTG_SELECT_IC_USB when OTG_ENABLE_IC_USB = 1. In all other cases, this bit is set to 1'b0 and the bit is read only.

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Bit	Attr	Reset Value	Description
25	RW	0x0	ULPIIfDis ULPI Interface Protect Disable Controls circuitry built into the PHY for protecting the ULPI interface when the link tri-states STP and data. Any pull-ups or pull-downs employed by this feature can be disabled. Please refer to the ULPI Specification for more detail. 1'b0: Enables the interface protect circuit 1'b1: Disables the interface protect circuit
24	RW	0x0	IndPassThrough Indicator Pass Through Controls whether the Complement Output is qualified with the Internal Vbus Valid comparator before being used in the Vbus State in the RX CMD. Please refer to the ULPI Specification for more detail. 1'b0: Complement Output signal is qualified with the Internal VbusValid comparator. 1'b1: Complement Output signal is not qualified with the Internal VbusValid comparator.
23	RW	0x0	IndComple Indicator Complement Controls the PHY to invert the ExternalVbusIndicator input signal,generating the Complement Output. Please refer to the ULPI Specification for more detail 1'b0: PHY does not invert ExternalVbusIndicator signal 1'b1: PHY does invert ExternalVbusIndicator signal
22	RW	0x0	TermSelDLPulse TermSel DLine Pulsing Selection This bit selects utmi_termselect to drive data line pulse during SRP. 1'b0: Data line pulsing using utmi_txvalid (default). 1'b1: Data line pulsing using utmi_termsel.
21	RW	0x0	ULPIExtVbusIndicator ULPI External VBUS Indicator This bit indicates to the ULPI PHY to use an external VBUS over-current indicator. 1'b0: PHY uses internal VBUS valid comparator. 1'b1: PHY uses external VBUS valid comparator. (Valid only when RTL parameter OTG_HSPHY_INTERFACE = 2 or 3)

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Bit	Attr	Reset Value	Description
20	RW	0x0	ULPIExtVbusDrv ULPI External VBUS Drive This bit selects between internal or external supply to drive 5V on VBUS,in ULPI PHY. 1'b0: PHY drives VBUS using internal charge pump (default). 1'b1: PHY drives VBUS using external supply. (Valid only when RTL parameter OTG_HSPHY_INTERFACE = 2 or 3)
19	RW	0x0	ULPIClkSusM ULPI Clock SuspendM This bit sets the ClockSuspendM bit in the Interface Control register on the ULPI PHY. This bit applies only in serial or carkit modes. 1'b0: PHY powers down internal clock during suspend. 1'b1: PHY does not power down internal clock. (Valid only when RTL parameter OTG_HSPHY_INTERFACE = 2 or 3)
18	RW	0x0	ULPIAutoRes ULPI Auto Resume This bit sets the AutoResume bit in the Interface Control register on the ULPI PHY. 1'b0: PHY does not use AutoResume feature. 1'b1: PHY uses AutoResume feature. (Valid only when RTL parameter OTG_HSPHY_INTERFACE = 2 or 3)
17	RW	0x0	ULPIFsLs ULPI FS/LS Select The application uses this bit to select the FS/LS serial interface for the ULPI PHY. This bit is valid only when the FS serial transceiver is selected on the ULPI PHY. 1'b0: ULPI interface 1'b1: ULPI FS/LS serial interface (Valid only when RTL parameters OTG_HSPHY_INTERFACE = 2 or 3 and OTG_FSPHY_INTERFACE = 1, 2, or 3)
16	RW	0x0	OtgI2CSel UTMIFS or I2C Interface Select The application uses this bit to select the I2C interface. 1'b0: UTMI USB 1.1 Full-Speed interface for OTG signals 1'b1: I2C interface for OTG signals This bit is writable only if I2C and UTMIFS were specified for Enable I2C Interface (parameter OTG_I2C_INTERFACE = 2). Otherwise, reads return 0.

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Bit	Attr	Reset Value	Description
15	RW	0x0	PhyLPwrClkSel PHY Low-Power Clock Select Selects either 480-MHz or 48-MHz (low-power) PHY mode. In FS and LS modes, the PHY can usually operate on a 48-MHz clock to save power. 1'b0: 480-MHz Internal PLL clock 1'b1: 48-MHz External Clock In 480 MHz mode, the UTMI interface operates at either 60 or 30-MHz, depending upon whether 8- or 16-bit data width is selected. In 48-MHz mode, the UTMI interface operates at 48 MHz in FS and LS modes. This bit drives the utmi_fsls_low_power core output signal, and is valid only for UTMI+ PHYs.
14	RO	0x0	reserved
13:10	RW	0x5	USBTrdTim USB Turnaround Time Sets the turnaround time in PHY clocks. Specifies the response time for a MAC request to the Packet FIFO Controller (PFC) to fetch data from the DFIF(SPRAM). This must be programmed to 4'h5: When the MAC interface is 16-bit UTMI+. 4'h9: When the MAC interface is 8-bit UTMI+. Note: The values above are calculated for the minimum AHB frequency of 30MHz. USB turnaround time is critical for certification where long cables and 5-Hubs are used, so if you need the AHB to run at less than 30 MHz, and if USB turnaround time is not critical, these bits can be programmed to a larger value.
9	RW	0x0	HNPCap HNP-Capable The application uses this bit to control the DWC_otg core's HNP capabilities. 0: HNP capability is not enabled. 1: HNP capability is enabled. This bit is writable only if an HNP mode was specified for Mode of Operation (parameter OTG_MODE). Otherwise, reads return 0.
8	RW	0x0	SRPCap SRP-Capable The application uses this bit to control the DWC_otg core SRP capabilities. If the core operates as a non-SRP-capable B-device, it cannot request the connected A-device (host) to activate VBUS and start a session. 0: SRP capability is not enabled. 1: SRP capability is enabled. This bit is writable only if an SRP mode was specified for Mode of Operation in coreConsultant (parameter OTG_MODE). Otherwise, reads return 0.

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Bit	Attr	Reset Value	Description
7	RW	0x0	DDRSel ULPI DDR Select The application uses this bit to select a Single Data Rate (SDR) or Double Data Rate (DDR) or ULPI interface. 0: Single Data Rate ULPI Interface, with 8-bit-wide data bus 1: Double Data Rate ULPI Interface, with 4-bit-wide data bus
6	RW	0x0	PHYSel USB 2.0 High-Speed PHY or USB 1.1 Full-Speed Serial Transcei The application uses this bit to select either a high-speed UTMI+ or ULPI PHY, or a full-speed transceiver. 0: USB 2.0 high-speed UTMI+ or ULPI PHY 1: USB 1.1 full-speed serial transceiver If a USB 1.1 Full-Speed Serial Transceiver interface was not selected (parameter OTG_FSPHY_INTERFACE = 0), this bit is always 0, with Write Only access. If a high-speed PHY interface was not selected (parameter OTG_HSPHY_INTERFACE = 0), this bit is always 1, with Write Only access. If both interface types were selected in coreConsultant (parameters have non-zero values), the application uses this bit to select which interface is active, and access is Read and Write.
5	RW	0x0	FSIntf Full-Speed Serial Interface Select The application uses this bit to select either a unidirectional or bidirectional USB 1.1 full-speed serial transceiver interface. 0: 6-pin unidirectional full-speed serial interface 1: 3-pin bidirectional full-speed serial interface If a USB 1.1 Full-Speed Serial Transceiver interface was not selected (parameter OTG_FSPHY_INTERFACE = 0), this bit is always 0, with Write Only access. If a USB 1.1 FS interface was selected (parameter OTG_FSPHY_INTERFACE! = 0), then the application can set this bit to select between the 3- and 6-pin interfaces, and access is Read and Write.
4	RW	0x0	ULPI_UTMI_Sel ULPI or UTMI+ Select The application uses this bit to select either a UTMI+ interface or ULPI Interface. 0: UTMI+ Interface 1: ULPI Interface This bit is writable only if UTMI+ and ULPI was specified for High-Speed PHY Interface(s) in coreConsultant configuration (parameter OTG_HSPHY_INTERFACE = 3). Otherwise, reads return either 0 or 1, depending on the interface selected using the OTG_HSPHY_INTERFACE parameter.

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Bit	Attr	Reset Value	Description
3	RW	0x0	PHYIf PHY Interface The application uses this bit to configure the core to support a UTMI+ PHY with an 8- or 16-bit interface. When a ULPI PHY is chosen, this must be set to 8-bit mode. 0: 8 bits 1: 16 bits This bit is writable only if UTMI+ and ULPI were selected (parameter OTG_HSPHY_DWIDTH = 3). Otherwise, this bit returns the value for the power-on interface selected during configuration.
2:0	RW	0x0	TOutCal HS/FS Timeout Calibration The number of PHY clocks that the application programs in this field is added to the high-speed/full-speed inter-packet timeout duration in the core to account for any additional delays introduced by the PHY. This can be required, because the delay introduced by the PHY in generating the line state condition can vary from one PHY to another. The USB standard timeout value for high-speed operation is 736 to 816 (inclusive) bit times. The USB standard timeout value for full-speedoperation is 16 to 18 (inclusive) bit times. The application must program this field based on the speed of enumeration. The number of bit times added per PHY clock are: High-speed operation: One 30-MHz PHY clock = 16 bit times One 60-MHz PHY clock = 8 bit times Full-speed operation: One 30-MHz PHY clock = 0.4 bit times One 60-MHz PHY clock = 0.2 bit times One 48-MHz PHY clock = 0.25 bit times

USBOTG_GRSTCTL
Address: Operational Base + offset (0x0010)
Reset Register

Bit	Attr	Reset Value	Description
31	RO	0x1	AHBIdle AHB Master Idle Indicates that the AHB Master State Machine is in the IDLE condition.
30	RO	0x0	DMAReq DMA Request Signal Indicates that the DMA request is in progress. Used for debug.
29:11	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
10:6	RW	0x00	TxFNum TxFIFO Number This is the FIFO number that must be flushed using the TxFIFO Flush bit. This field must not be changed until the core clears the TxFIFO Flush bit. 5'h0: Non-periodic TxFIFO flush in Host mode; Non-periodic TxFIFO flush in device mode when in shared FIFO operation. Tx FIFO 0 flush in device mode when in dedicated FIFO mode. 5'h1: Periodic TxFIFO flush in Host mode: Periodic TxFIFO 1 flush in Device mode when in shared FIFO operation; TXFIFO 1 flush in device mode when in dedicated FIFO mode. 5'h2: Periodic TxFIFO 2 flush in Device mode when in shared FIFO operation: TXFIFO 2 flush in device mode when in dedicated FIFO mode. ... 5'hF: Periodic TxFIFO 15 flush in Device mode when in shared FIFO operation: TXFIFO 15 flush in device mode when in dedicated FIFO mode. 5'h10: Flush all the transmit FIFOs in device or host mode.
5	R/W SC	0x0	TxFFlsh TxFIFO Flush This bit selectively flushes a single or all transmit FIFOs, but cannot do so if the core is in the midst of a transaction. The application must write this bit only after checking that the core is neither writing to the TxFIFO nor reading from the TxFIFO. Verify using these registers: Read NAK Effective Interrupt ensures the core is not reading from the FIFO. Write GRSTCTL.AHBIdle ensures the core is not writing anything to the FIFO. Flushing is normally recommended when FIFOs are re-configured or when switching between Shared FIFO and Dedicated Transmit FIFO operation. FIFO flushing is also recommended during device endpoint disable. The application must wait until the core clears this bit before performing any operations. This bit takes eight clocks to clear, using the slower clock of phy_clk or hclk.
4	R/W SC	0x0	RxFFlsh RxFIFO Flush The application can flush the entire RxFIFO using this bit, but must first ensure that the core is not in the middle of a transaction. The application must only write to this bit after checking that the core is neither reading from the RxFIFO nor writing to the RxFIFO. The application must wait until the bit is cleared before performing any other operations. This bit requires 8 clocks (slowest of PHY or AHB clock) to clear.

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Bit	Attr	Reset Value	Description
3	R/WSC	0x0	INTknQFlsh IN Token Sequence Learning Queue Flush This bit is valid only if OTG_EN_DED_TX_FIFO = 0. The application writes this bit to flush the IN Token Sequence Learning Queue.
2	W1C	0x0	FrmCntrRst Host Frame Counter Reset The application writes this bit to reset the (micro)frame number counter inside the core. When the (micro)frame counter is reset, the subsequent SOF sent out by the core has a (micro)frame number of 0.
1	R/WSC	0x0	Reset A write to this bit issues a soft reset to the DWC_otg_power_dn module of the core.

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Bit	Attr	Reset Value	Description
0	R/W SC	0x0	CSftRst Core Soft Reset Resets the hclk and phy_clock domains as follows: Clears the interrupts and all the CSR registers except the following register bits: CGCCTL.RstPdwnModule PCGCCTL.GateHclk PCGCCTL.PwrClmp PCGCCTL.StopPPhyLPwrClkSelclk GUSBCFG.PhyLPwrClkSel GUSBCFG.DDRSel GUSBCFG.PHYSel GUSBCFG.FSIntf GUSBCFG.ULPI_UTMI_Sel GUSBCFG.PHYIf HCFG.FSLSPclkSel DCFG.DevSpd GGPIO GPWRDN GADPCTL All module state machines (except the AHB Slave Unit) are reset to the IDLE state, and all the transmit FIFOs and the receive FIFO are flushed. Any transactions on the AHB Master are terminated as soon as possible, after gracefully completing the last data phase of an AHB transfer. Any transactions on the USB are terminated immediately. When Hibernation or ADP feature is enabled, the PMU module is not reset by the Core Soft Reset. The application can write to this bit any time it wants to reset the core. This is a self-clearing bit and the core clears this bit after all the necessary logic is reset in the core, which can take several clocks, depending on the current state of the core. Once this bit is cleared software must wait at least 3 PHY clocks before doing any access to the PHY domain (synchronization delay). Software must also must check that bit 31 of this register is 1 (AHB Master is IDLE) before starting any operation. Typically software reset is used during software development and also when you dynamically change the PHY selection bits in the USB configuration registers listed above. When you change the PHY, the corresponding clock for the PHY is selected and used in the PHY domain. Once a new clock is selected, the PHY domain has to be reset for proper operation.

USBOTG_GINTSTS
Address: Operational Base + offset (0x0014)
Interrupt Register

Bit	Attr	Reset Value	Description
31	W1C	0x0	WkUpInt Resume/Remote Wakeup Detected Interrupt Wakeup Interrupt during Suspend(L2) or LPM(L1) state. During Suspend(L2): Device Mode:This interrupt is asserted only when Host Initiated Resume is detected on USB. Host Mode:This interrupt is asserted only when Device Initiated Remote Wakeup is detected on USB. During LPM(L1): Device Mode:This interrupt is asserted for either Host Initiated Resume or Device Initiated Remote Wakeup on USB. Host Mode:This interrupt is asserted for either Host Initiated Resume or Device Initiated Remote Wakeup on USB.
30	W1C	0x0	SessReqInt Session Request/New Session Detected Interrupt In Host mode, this interrupt is asserted when a session request is detected from the device. In Host mode, this interrupt is asserted when a session request is detected from the device. In Device mode, this interrupt is asserted when the utmisrp_bvalid signal goes high.
29	W1C	0x0	DisconnInt Disconnect Detected Interrupt This interrupt is asserted when a device disconnect is detected.
28	W1C	0x0	ConIDStsChng Connector ID Status Change This interrupt is asserted when there is a change in connector ID status.
27	W1C	0x0	LPM_Int LPM Transaction Received Interrupt Device Mode: This interrupt is asserted when the device receives an LPM transaction and responds with a non-ERRORed response. Host Mode: This interrupt is asserted when the device responds to an LPM transaction with a non-ERRORed response or when the host core has completed LPM transactions for the programmed number of times (GLPMCFG.RetryCnt). This field is valid only if the Core LPM Configuration register's LPMCapable (LPMCap) field is set to 1.
26	RO	0x0	PTxFEmp Periodic TxFIFO Empty This interrupt is asserted when the Periodic Transmit FIFO is either half or completely empty and there is space for at least one entry to be written in the Periodic Request Queue. The half or completely empty status is determined by the Periodic TxFIFO Empty Level bit in the Core AHB Configuration register (GAHBCFG.PTxFEmpLvl).

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Bit	Attr	Reset Value	Description
25	RO	0x0	HChInt Host Channels Interrupt The core sets this bit to indicate that an interrupt is pending on one of the channels of the core (in Host mode). The application must read the Host All Channels Interrupt (HAINT) register to determine the exact number of the channel on which the interrupt occurred, and then read the corresponding Host Channel-n Interrupt (HCINTn) register to determine the exact cause of the interrupt. The application must clear the appropriate status bit in the HCINTn register to clear this bit.
24	RO	0x0	PrtInt Host Port Interrupt The core sets this bit to indicate a change in port status of one of the DWC_otg core ports in Host mode. The application must read the Host Port Control and Status (HPRT) register to determine the exact event that caused this interrupt. The application must clear the appropriate status bit in the Host Port Control and Status register to clear this bit.
23	RW	0x0	ResetDet Reset Detected Interrupt The core asserts this interrupt in Device mode when it detects a reset on the USB in Partial Power-Down mode when the device is in Suspend. This interrupt is not asserted in Host mode.
22	W1C	0x0	FetSusp Data Fetch Suspended This interrupt is valid only in DMA mode. This interrupt indicates that the core has stopped fetching data for IN endpoints due to the unavailability of TxFIFO space or Request Queue space. This interrupt is used by the application for an endpoint mismatch algorithm. For example, after detecting an endpoint mismatch, the application: Sets a global non-periodic IN NAK handshake, Disables In endpoints, Flushes the FIFO, Determines the token sequence from the IN Token Sequence Learning Queue, Re-enables the endpoints, Clear the global non-periodic IN NAK handshake. If the global non-periodic IN NAK is cleared, the core has not yet fetched data for the IN endpoint, and the IN token is received: the core generates an "IN token received when FIFO empty" interrupt. The OTG then sends the host a NAK response. To avoid this scenario, the application can check the GINTSTS.FetSusp interrupt, which ensures that the FIFO is full before clearing a global NAK handshake. Alternatively, the application can mask the IN token received when FIFO empty interrupt when clearing a global IN NAK handshake.

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Bit	Attr	Reset Value	Description
21	W1C	0x0	incomplP Incomplete Periodic Transfer In Host mode, the core sets this interrupt bit when there are incomplete periodic transactions still pending which are scheduled for the current microframe. Incomplete Isochronous OUT Transfer (incompISOOUT) The Device mode, the core sets this interrupt to indicate that there is at least one isochronous OUT endpoint on which the transfer is not completed in the current microframe. This interrupt is asserted along with the End of Periodic Frame Interrupt (EOPF) bit in this register.
20	W1C	0x0	incompISOIN Incomplete Isochronous IN Transfer The core sets this interrupt to indicate that there is at least one isochronous IN endpoint on which the transfer is not completed in the current microframe. This interrupt is asserted along with the End of Periodic Frame Interrupt (EOPF) bit in this register. Note: This interrupt is not asserted in Scatter/Gather DMA mode.
19	RO	0x0	OEPInt OUT Endpoints Interrupt The core sets this bit to indicate that an interrupt is pending on one of the OUT endpoints of the core (in Device mode). The application must read the Device All Endpoints Interrupt (DAINT) register to determine the exact number of the OUT endpoint on which the interrupt occurred, and then read the corresponding Device OUT Endpoint-n Interrupt (DOEPINTn) register to determine the exact cause of the interrupt. The application must clear the appropriate status bit in the corresponding DOEPINTn register to clear this bit.
18	RO	0x0	IEPInt IN Endpoints Interrupt The core sets this bit to indicate that an interrupt is pending on one of the IN endpoints of the core (in Device mode). The application must read the Device All Endpoints Interrupt (DAINT) register to determine the exact number of the IN endpoint on which the interrupt occurred, and then read the corresponding Device IN Endpoint-n Interrupt (DIEPINTn) register to determine the exact cause of the interrupt. The application must clear the appropriate status bit in the corresponding DIEPINTn register to clear this bit.

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Bit	Attr	Reset Value	Description
17	W1C	0x0	EPMis Endpoint Mismatch Interrupt Note: This interrupt is valid only in shared FIFO operation. Indicates that an IN token has been received for a non-periodic endpoint, but the data for another endpoint is present in the top of the Non-periodic Transmit FIFO and the IN endpoint mismatch count programmed by the application has expired.
16	W1C	0x0	RstrDoneInt Restore Done Interrupt The core sets this bit to indicate that the restore command after Hibernation was completed by the core. The core continues from Suspended state into the mode dictated by PCGCCTL.RestoreMode field.This bit is valid only when Hibernation feature is enabled.
15	W1C	0x0	EOPF End of Periodic Frame Interrupt Indicates that the period specified in the Periodic Frame Interval field of the Device Configuration register (DCFG.PerFrInt) has been reached in the current microframe.
14	W1C	0x0	ISOOutDrop Isochronous OUT Packet Dropped Interrupt The core sets this bit when it fails to write an isochronous OUT packet into the RxFIFO because the RxFIFO does not have enough space to accommodate a maximum packet size packet for the isochronous OUT endpoint.
13	W1C	0x0	EnumDone Enumeration Done The core sets this bit to indicate that speed enumeration is complete. The application must read the Device Status (DSTS) register to obtain the enumerated speed.
12	W1C	0x0	USBRst USB Reset The core sets this bit to indicate that a reset is detected on the USB.
11	W1C	0x0	USBSusp USB Suspend The core sets this bit to indicate that a suspended was detected on the USB. The core enters the Suspended state when there is no activity on the utmi_linestate signal for an extended period of time.
10	W1C	0x0	ErlySusp Early Suspend The core sets this bit to indicate that an Idle state has been detected on the USB for 3ms.

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Bit	Attr	Reset Value	Description
9	W1C	0x0	I2CINT I2C Interrupt The core sets this interrupt when I2C access is completed on the I2C interface. This field is used only if the I2C interface was enabled. Otherwise, reads return 0.
8	W1C	0x0	ULPICKINT ULPI Carkit Interrupt This field is used only if the Carkit interface was enabled. Otherwise, reads return 0. The core sets this interrupt when a ULPI Carkit interrupt is received. The core's PHY sets ULPI Carkit interrupt in UART or Audio mode. I2C Carkit Interrupt (I2CCKINT) This field is used only if the I2C interface was enabled. Otherwise, reads return 0.The core sets this interrupt when a Carkit interrupt is received. The core's PHY sets the I2C Carkit interrupt in Audio mode.
7	RO	0x0	GOUTNakEff Global OUT NAK Effective Indicates that the Set Global OUT NAK bit in the Device Control register DCTL.SGOUTNak), set by the application, has taken effect in the core. This bit can be cleared by writing the Clear Global OUT NAK bit in the Device Control register (DCTL.CGOUTNak).
6	RO	0x0	GINNakEff Global IN Non-Periodic NAK Effective Indicates that the Set Global Non-periodic IN NAK bit in the Device Control register (DCTL.SGNPInNak), set by the application, have taken effect in the core. That is, the core has sampled the Global IN NAK bit set by the application. This bit can be cleared by clearing the Clear Global Nonperiodic IN NAK bit in the Device Control register (DCTL.CGNPInNak). This interrupt does not necessarily mean that a NAK handshake is sent out on the USB. The STALL bit takes precedence over the NAK bit.
5	RO	0x0	NPTxFEmp Non-Periodic TxFIFO Empty This interrupt is valid only when OTG_EN_DED_TX_FIFO = 0. This interrupt is asserted when the Non-periodic TxFIFO is either half or completely empty, and there is space for at least one entry to be written to the Non-periodic Transmit Request Queue. The half or completely empty status is determined by the Non-periodic TxFIFO Empty Level bit in the Core AHB Configuration register(GAHBCFG.NPTxFEmpLvl).
4	RO	0x0	RxFLvl RxFIFO Non-Empty Indicates that there is at least one packet pending to be read from the RxFIFO.

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Bit	Attr	Reset Value	Description
3	W1C	0x0	Sof Start of (micro)Frame In Host mode, the core sets this bit to indicate that an SOF (FS), micro-SOF(HS), or Keep-Alive (LS) is transmitted on the USB. The application must write a 1 to this bit to clear the interrupt. In Device mode, in the core sets this bit to indicate that an SOF token has been received on the USB. The application can read the Device Status register to get the current (micro)frame number. This interrupt is seen only when the core is operating at either HS or FS.
2	RO	0x0	OTGInt OTG Interrupt The core sets this bit to indicate an OTG protocol event. The application must read the OTG Interrupt Status (GOTGINT) register to determine the exact event that caused this interrupt. The application must clear the appropriate status bit in the GOTGINT register to clear this bit.
1	W1C	0x0	ModeMis Mode Mismatch Interrupt The core sets this bit when the application is trying to access: A Host mode register, when the core is operating in Device mode; A Device mode register, when the core is operating in Host mode. The register access is completed on the AHB with an OKAY response, but is ignored by the core internally and does not affect the operation of the core.
0	RO	0x0	CurMod Current Mode of Operation Indicates the current mode. 1'b0: Device mode 1'b1: Host mode

USBOTG_GINTMSK

Address: Operational Base + offset (0x0018)

Interrupt Mask Register

Bit	Attr	Reset Value	Description
31	RW	0x0	WkUpIntMsk Resume/Remote Wakeup Detected Interrupt Mask
30	RW	0x0	SessReqIntMsk Session Request/New Session Detected Interrupt Mask
29	RW	0x0	DisconnIntMsk Disconnect Detected Interrupt Mask
28	RW	0x0	ConIDStsChngMsk Connector ID Status Change Mask
27	RW	0x0	LPM_IntMsk LPM Transaction Received Interrupt Mask

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Bit	Attr	Reset Value	Description
26	RW	0x0	PTxFEmpMsk Periodic TxFIFO Empty Mask
25	RW	0x0	HChIntMsk Host Channels Interrupt Mask
24	RW	0x0	PrtIntMsk Host Port Interrupt Mask
23	RW	0x0	ResetDetMsk Reset Detected Interrupt Mask
22	RW	0x0	FetSuspMsk Data Fetch Suspended Mask
21	RW	0x0	incomplPMsk_incompISOOUTMsk Incomplete Periodic Transfer Mask(Host only) Incomplete Isochronous OUT Transfer Mask(Device only)
20	RW	0x0	incompISOINMsk Incomplete Isochronous IN Transfer Mask
19	RW	0x0	OEPIntMsk OUT Endpoints Interrupt Mask
18	RW	0x0	IEPIntMsk IN Endpoints Interrupt Mask
17	RW	0x0	EPMisMsk Endpoint Mismatch Interrupt Mask
16	RW	0x0	RstrDoneIntMsk Restore Done Interrupt Mask This field is valid only when Hibernation feature is enabled.
15	RW	0x0	EOPFMsk End of Periodic Frame Interrupt Mask
14	RW	0x0	ISOOutDropMsk Isochronous OUT Packet Dropped Interrupt Mask
13	RW	0x0	EnumDoneMsk Enumeration Done Mask
12	RW	0x0	USBRstMsk USB Reset Mask
11	RW	0x0	USBSuspMsk USB Suspend Mask
10	RW	0x0	ErlySuspMsk Early Suspend Mask
9	RW	0x0	I2CIntMsk I2C Interrupt Mask
8	RW	0x0	ULPICKINTMsk_I2CCKINTMsk ULPI Carkit Interrupt Mask (ULPICKINTMsk) I2C Carkit Interrupt Mask (I2CCKINTMsk)
7	RW	0x0	GOUTNakEffMsk Global OUT NAK Effective Mask

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Bit	Attr	Reset Value	Description
6	RW	0x0	GINNakEffMsk Global Non-periodic IN NAK Effective Mask
5	RW	0x0	NPTxFEmpMsk Non-periodic TxFIFO Empty Mask
4	RW	0x0	RxFLvlMsk Receive FIFO Non-Empty Mask
3	RW	0x0	SofMsk Start of (micro)Frame Mask
2	RW	0x0	OTGIntMsk OTG Interrupt Mask
1	RW	0x0	ModeMisMsk Mode Mismatch Interrupt Mask
0	RO	0x0	reserved

USBOTG_GRXSTSR
Address: Operational Base + offset (0x001c)
Receive Status Debug Read Register

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24:21	RO	0x0	FN Frame Number (Device Only)This is the least significant 4 bits of the (micro) frame number in which the packet is received on the USB. This field is supported only when isochronous OUT endpoints are supported.
20:17	RO	0x0	PktSts Packet Status Indicates the status of the received packet(Host Only) 4'b0010: IN data packet received 4'b0011: IN transfer completed (triggers an interrupt) 4'b0101: Data toggle error (triggers an interrupt) 4'b0111: Channel halted (triggers an interrupt) Others: Reserved Indicates the status of the received packet(Device only) 4'b0001: Global OUT NAK (triggers an interrupt) 4'b0010: OUT data packet received 4'b0011: OUT transfer completed (triggers an interrupt) 4'b0100: SETUP transaction completed (triggers an interrupt) 4'b0110: SETUP data packet received Others: Reserved

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Bit	Attr	Reset Value	Description
16:15	RO	0x0	DPID Data PID Indicates the Data PID of the received packet 2'b00: DATA0 2'b10: DATA1 2'b01: DATA2 2'b11: MDATA
14:4	RW	0x000	BCnt Byte Count Indicates the byte count of the received data packet.
3:0	RO	0x0	ChNum_EPNum Channel Number(Host) Endpoint Number(Device) (Host Only) Indicates the channel number to which the current received packet belongs. (Device Only) Indicates the endpoint number to which the current received packet belongs.

USBOTG_GRXSTSP
Address: Operational Base + offset (0x0020)
Receive Status Read and Pop Register

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24:21	RO	0x0	FN Frame Number (Device Only) This is the least significant 4 bits of the (micro)frame number in which the packet is received on the USB. This field is supported only when isochronous OUT endpoints are supported.
20:17	RO	0x0	PktSts Packet Status Indicates the status of the received packet(Host Only) 4'b0010: IN data packet received 4'b0011: IN transfer completed (triggers an interrupt) 4'b0101: Data toggle error (triggers an interrupt) 4'b0111: Channel halted (triggers an interrupt) Others: Reserved Indicates the status of the received packet(Device only) 4'b0001: Global OUT NAK (triggers an interrupt) 4'b0010: OUT data packet received 4'b0011: OUT transfer completed (triggers an interrupt) 4'b0100: SETUP transaction completed (triggers an interrupt) 4'b0110: SETUP data packet received Others: Reserved

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Bit	Attr	Reset Value	Description
16:15	RO	0x0	DPID Data PID Indicates the Data PID of the received OUT data packet 2'b00: DATA0 2'b10: DATA1 2'b01: DATA2 2'b11: MDATA
14:4	RO	0x000	BCnt Byte Count Indicates the byte count of the received data packet.
3:0	RO	0x0	ChNum_EPNum Channel Number(Host) Endpoint Number(Device) (Host Only) Indicates the channel number to which the current received packet belongs. (Device Only) Indicates the endpoint number to which the current received packet belongs.

USBOTG_GRXFSIZ
Address: Operational Base + offset (0x0024)
Receive FIFO Size Register

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0000	RxFDep RxFIFO Depth This value is in terms of 32-bit words. Minimum value is 16. Maximum value is 32,768. The power-on reset value of this register is specified as the Largest Rx Data FIFO Depth. If Enable Dynamic FIFO Sizing was deselected, these flops are optimized, and reads return the power-on value. If Enable Dynamic FIFO Sizing wasselected, you can write a new value in this field. You can write a new value in this field. Programmed values must not exceed the power-on value.

USBOTG_GNPTXFSIZ
Address: Operational Base + offset (0x0028)
Non-Periodic Transmit FIFO Size Register

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	NPTxFDep Non-periodic TxFIFO For host mode, this field is always valid. For Device mode, this field is valid only when OTG_EN_DED_TX_FIFO==0. This value is in terms of 32-bit words. Minimum value is 16. Maximum value is 32,768 This field is determined by Enable Dynamic FIFO Sizing. OTG_DFIFO_DYNAMIC = 0: These flops are optimized, and reads return the power-on value. OTG_DFIFO_DYNAMIC = 1: The application can write a new value in this field. Programmed values must not exceed the power-on value. The power-on reset value of this field is specified by OTG_EN_DED_TX_FIFO: OTG_EN_DED_TX_FIFO = 0:The reset value is the Largest Non-periodic Tx Data FIFO Depth parameter, OTG_TX_NPERIO_DFIFO_DEPTH. OTG_EN_DED_TX_FIFO = 1:The reset value is parameter OTG_TX_HNPERIO_DFIFO_DEPTH.
15:0	RW	0x0000	NPTxFStAddr Non-periodic Transmit RAM For host mode, this field is always valid. This field contains the memory start address for Non-periodic Transmit FIFO RAM. This field is determined by Enable Dynamic FIFO Sizing(OTG_DFIFO_DYNAMIC): OTG_DFIFO_DYNAMIC = 0:These flops are optimized, and reads return the power-on value. OTG_DFIFO_DYNAMIC = 1:The application can write a new value in this field. Programmed values must not exceed the power-on value. The power-on reset value of this field is specified by Largest Rx Data FIFO Depth (parameter OTG_RX_DFIFO_DEPTH).

USBOTG_GNPTXSTS

Address: Operational Base + offset (0x002c)

Non-Periodic Transmit FIFO/Queue Status Register

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved

Bit	Attr	Reset Value	Description
30:24	RO	0x00	NPTxQTop Top of the Non-periodic Transmit Request Queue Entry in the Non-periodic Tx Request Queue that is currently being processed by the MAC. Bits [30:27]: Channel/endpoint number Bits [26:25]: 2'b00: IN/OUT token 2'b01: Zero-length transmit packet (device IN/host OUT) 2'b10: PING/CSPLIT token 2'b11: Channel halt command Bit [24]: Terminate (last entry for selected channel/endpoint)
23:16	RO	0x00	NPTxQSpcAvail Non-periodic Transmit Request Queue Space Available Indicates the amount of free space available in the Non-periodic Transmit Request Queue. This queue holds both IN and OUT requests in Host mode. Device mode has only IN requests. 8'h0: Non-periodic Transmit Request Queue is full 8'h1: 1 location available 8'h2: 2 locations available n: n locations available (0 <=n <= 8) Others: Reserved
15:0	RO	0x0000	NPTxFSpcAvail Non-periodic TxFIFO Space Avail Indicates the amount of free space available in the Non-periodic TxFIFO. Values are in terms of 32-bit words. 16'h0: Non-periodic TxFIFO is full 16'h1: 1 word available 16'h2: 2 words available 16'hn: n words available (where 0 <=n <=32,768) 16'h8000: 32,768 words available Others: Reserved

USBOTG_GI2CCTL

Address: Operational Base + offset (0x0030)

I2C Address Register

Bit	Attr	Reset Value	Description
31	R/WSC	0x0	BsyDne I2C Busy/Done The application sets this bit to 1'b1 to start a request on the I2C interface. When the transfer is complete, the core de-asserts this bit to 1'b0. As long as the bit is set, indicating that the I2C interface is busy, the application cannot start another request on the interface.

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Bit	Attr	Reset Value	Description
30	RW	0x0	RW Read/Write Indicator Indicates whether a read or write register transfer must be performed on the interface.Read/write bursting is not supported for registers. 1'b1: Read 1'b0: Write
29	RO	0x0	reserved
28	RW	0x1	I2CDatSe0 I2C DatSe0 USB Mode Selects the FS interface USB mode. 1'b1: VP_VM USB mode 1'b0: DAT_SE0 USB mode
27:26	RW	0x0	I2CDevAdr I2C Device Address Selects the address of the I2C Slave on the USB 1.1 full-speed serial transceiver that the core uses for OTG signaling. 2'b00: 7'h2C 2'b01: 7'h2D 2'b10: 7'h2E 2'b11: 7'h2F
25	RW	0x0	I2CSuspCtl I2C Suspend Control Selects how Suspend is connected to a full-speed transceiver in I2C mode. 1'b0: Use the dedicated utmi_suspend_n pin 1'b1: Use an I2C write to program the Suspend bit in the PHY register
24	RO	0x1	Ack I2C ACK Indicates whether an ACK response was received from the I2C Slave. This bit is valid when BsyDne is cleared by the core, after application has initiated an I2C access. 1'b0: NAK 1'b1: ACK
23	RW	0x0	I2CEn I2C Enable Enables the I2C Master to initiate I2C transactions on the I2C interface
22:16	RW	0x00	Addr I2C Address This is the 7-bit I2C device address used by software to access any external I2C Slave,including the I2C Slave on a USB 1.1 OTG full-speed serial transceiver. Software can change this address to access different I2C Slaves.

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Bit	Attr	Reset Value	Description
15:8	RW	0x00	RegAddr I2C Register Addr This field programs the address of the register to be read from or written to.
7:0	RW	0x00	RWData I2C Read/Write Data After a register read operation, this field holds the read data for the application. During a write operation, the application can use this register to program the write data to be written to a register. During writes, this field holds the write data.

USBOTG_GPVNDCTL
Address: Operational Base + offset (0x0034)
PHY Vendor Control Register

Bit	Attr	Reset Value	Description
31	R/W SC	0x0	DisUlpiDrvr Disable ULPI Drivers This field is used only if the Carkit interface was enabled in coreConsultant (parameter OTG_ULPI_CARKIT = 1). Otherwise, reads return 0. The application sets this bit when it has finished processing the ULPI Carkit Interrupt (GINTSTS.ULPICKINT). When set, the DWC_otg core disables drivers for output signals and masks input signal for the ULPI interface. DWC_otg clears this bit before enabling the ULPI interface.
30:28	RO	0x0	reserved
27	R/W SC	0x0	VStsDone VStatus Done The core sets this bit when the vendor control access is done. This bit is cleared by the core when the application sets the New Register Request bit (bit 25).
26	RO	0x0	VStsBsy VStatus Busy The core sets this bit when the vendor control access is in progress and clears this bit when done.
25	R/W SC	0x0	NewRegReq New Register Request The application sets this bit for a new vendor control access.
24:23	RO	0x0	reserved
22	RW	0x0	RegWr Register Write Set this bit for register writes, and clear it for register reads.
21:16	RW	0x00	RegAddr Register Address The 6-bit PHY register address for immediate PHY Register Set access. Set to 6'h2F for Extended PHY Register Set access.

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Bit	Attr	Reset Value	Description
15:8	RW	0x00	VCtrl UTMI+ Vendor Control Register Address The 4-bit register address a vendor defined 4-bit parallel output bus. Bits 11:8 of this field are placed on utmi_vcontrol[3:0]. ULPI Extended Register Address (ExtRegAddr) The 6-bit PHY extended register address.
7:0	RW	0x00	RegData Register Data Contains the write data for register write. Read data for register read, valid when VStatus Done is set.

USBOTG_GGPIO
Address: Operational Base + offset (0x0038)
General Purpost Input/Output Register

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	GPO General Purpose Output This field is driven as an output from the core, gp_o[15:0]. The application can program this field to determine the corresponding value on the gp_o[15:0] output.
15:0	RO	0x0000	GPI General Purpose Input This field's read value reflects the gp_i[15:0] core input value.

USBOTG_GUID
Address: Operational Base + offset (0x003c)
User ID Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	UserID Application-programmable ID field.

USBOTG_GSNPSID
Address: Operational Base + offset (0x0040)
Core ID Register

Bit	Attr	Reset Value	Description
31:0	RO	0x00004f54	CoreID Release number of the core being used

USBOTG_GHWCFG1
Address: Operational Base + offset (0x0044)
User HW Config1 Register

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	epdir Endpoint Direction This 32-bit field uses two bits per endpoint to determine the endpoint direction. Endpoint Bits [31:30]: Endpoint 15 direction Bits [29:28]: Endpoint 14 direction ... Bits [3:2]: Endpoint 1 direction Bits[1:0]: Endpoint 0 direction (always BIDIR) Direction 2'b00: BIDIR (IN and OUT) endpoint 2'b01: IN endpoint 2'b10: OUT endpoint 2'b11: Reserved

USBOTG_GHWCFG2
Address: Operational Base + offset (0x0048)
User HW Config2 Register

Bit	Attr	Reset Value	Description
31	RO	0x0	OTG_ENABLE_IC_USB IC_USB mode specified for mode of operation (parameter OTG_ENABLE_IC_USB). To choose IC_USB_MODE, both OTG_FSPHY_INTERFACE and OTG_ENABLE_IC_USB must be 1.
30:26	RO	0x00	TknQDepth Device Mode IN Token Sequence Learning Queue Depth Range: 0-30
25:24	RO	0x0	PTxQDepth Host Mode Periodic Request Queue Depth 2'b00: 2 2'b01: 4 2'b10: 8 Others: Reserved
23:22	RO	0x0	NPTxQDepth Non-periodic Request Queue Depth 2'b00: 2 2'b01: 4 2'b10: 8 Others: Reserved
21	RO	0x0	reserved
20	RO	0x0	MultiProcIntrpt Multi Processor Interrupt Enabled 1'b0: No 1'b1: Yes

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Bit	Attr	Reset Value	Description
19	RO	0x0	DynFifoSizing Dynamic FIFO Sizing Enabled 1'b0: No 1'b1: Yes
18	RO	0x0	PerioSupport Periodic OUT Channels Supported in Host Mode 1'b0: No 1'b1: Yes
17:14	RO	0x0	NumHstChnl Number of Host Channels Indicates the number of host channels supported by the core in Host mode. The range of this field is 0-15: 0 specifies 1 channel, 15 specifies 16 channels.
13:10	RO	0x0	NumDevEps Number of Device Endpoints Indicates the number of device endpoints supported by the core in Device mode in addition to control endpoint 0. The range of this field is 1-15.
9:8	RO	0x0	FSPhyType Full-Speed PHY Interface Type 2'b00: Full-speed interface not supported 2'b01: Dedicated full-speed interface 2'b10: FS pins shared with UTMI+ pins 2'b11: FS pins shared with ULPI pins
7:6	RO	0x0	HSPhyType High-Speed PHY Interface Type 2'b00: High-Speed interface not supported 2'b01: UTMI+ 2'b10: ULPI 2'b11: UTMI+ and ULPI
5	RO	0x0	SingPnt Point-to-Point 1'b0: Multi-point application (hub and split support) 1'b1: Single-point application (no hub and no split support)
4:3	RO	0x0	OtgArch Architecture 2'b00: Slave-Only 2'b01: External DMA 2'b10: Internal DMA Others: Reserved

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Bit	Attr	Reset Value	Description
2:0	RO	0x0	OtgMode Mode of Operation 3'b000: HNP- and SRP-Capable OTG (Host and Device) 3'b001: SRP-Capable OTG (Host and Device) 3'b010: Non-HNP and Non-SRP Capable OTG (Host and Device) 3'b011: SRP-Capable Device 3'b100: Non-OTG Device 3'b101: SRP-Capable Host 3'b110: Non-OTG Host Others: Reserved

USBOTG_GHWCFG3
Address: Operational Base + offset (0x004c)
User HW Config3 Register

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	DfifoDepth DFIFO Depth This value is in terms of 32-bit words. Minimum value is 32 Maximum value is 32,768
15	RO	0x0	OTG_ENABLE_LPM LPM mode specified for Mode of Operation (parameter OTG_ENABLE_LPM).
14	RO	0x0	OTG_BC_SUPPORT This bit indicates the HS OTG controller support for Battery Charger. 0 : No Battery Charger Support 1 : Battery Charger support present.
13	RO	0x0	OTG_ENABLE_HSIC HSIC mode specified for Mode of Operation (parameter OTG_ENABLE_HSIC). Value Range: 0-1 1: HSIC-capable with shared UTMI PHY interface 0: Non-HSIC-capable
12	RO	0x0	OTG_ADP_SUPPORT This bit indicates whether ADP logic is present within or external to the HS OTG controller 0: No ADP logic present with HSOTG controller 1: ADP logic is present along with HSOTG controller.
11	RO	0x0	RstType Reset Style for Clocked always Blocks in RTL 1'b0: Asynchronous reset is used in the core 1'b1: Synchronous reset is used in the core

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Bit	Attr	Reset Value	Description
10	RO	0x0	OptFeature Optional Features Removed Indicates whether the User ID register, GPIO interface ports, and SOF toggle and counter ports were removed for gate count optimization by enabling Remove Optional Features? 1'b0: No 1'b1: Yes
9	RO	0x0	VndctlSupt Vendor Control Interface Support 1'b0: Vendor Control Interface is not available on the core. 1'b1: Vendor Control Interface is available.
8	RO	0x0	I2CIntSel I2C Selection 1'b0: I2C Interface is not available on the core. 1'b1: I2C Interface is available on the core.
7	RO	0x0	OtgEn OTG Function Enabled The application uses this bit to indicate the DWC_otg core's OTG capabilities. 1'b0: Not OTG capable 1'b1: OTG Capable
6:4	RO	0x0	PktSizeWidth Width of Packet Size Counters 3'b000: 4 bits 3'b001: 5 bits 3'b010: 6 bits 3'b011: 7 bits 3'b100: 8 bits 3'b101: 9 bits 3'b110: 10 bits Others: Reserved
3:0	RO	0x0	XferSizeWidth Width of Transfer Size Counters 4'b0000: 11 bits 4'b0001: 12 bits ... 4'b1000: 19 bits Others: Reserved

USBOTG_GHWCFG4
Address: Operational Base + offset (0x0050)
User HW Config4 Register

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Bit	Attr	Reset Value	Description
31	RO	0x0	SGDMA Scatter/Gather DMA 1'b1: Dynamic configuration
30	RO	0x0	SGDMACon Scatter/Gather DMA configuration 1'b0: Non-Scatter/Gather DMA configuration 1'b1: Scatter/Gather DMA configuration
29:26	RO	0x0	INEps Number of Device Mode IN Endpoints Including Control Endpoint Range 0 -15 0:1 IN Endpoint 1:2 IN Endpoints .... 15:16 IN Endpoints
25	RW	0x0	DedFifoMode Enable Dedicated Transmit FIFO for device IN Endpoints 1'b0: Dedicated Transmit FIFO Operation not enabled. 1'b1: Dedicated Transmit FIFO Operation enabled.
24	RW	0x0	SessEndFltr session_end Filter Enabled 1'b0: No filter 1'b1: Filter
23	RW	0x0	BValidFltr "b_valid" Filter Enabled 1'b0: No filter 1'b1: Filter
22	RO	0x0	AValidFltr "a_valid" Filter Enabled 1'b0: No filter 1'b1: Filter
21	RO	0x0	VBusValidFltr "vbus_valid" Filter Enabled 1'b0: No filter 1'b1: Filter
20	RO	0x0	IddgFltr "iddig" Filter Enable 1'b0: No filter 1'b1: Filter
19:16	RO	0x0	NumCtlEps Number of Device Mode Control Endpoints in Addition to Endpoin Range: 0-15

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Bit	Attr	Reset Value	Description
15:14	RO	0x0	PhyDataWidth UTMI+ PHY/ULPI-to-Internal UTMI+ Wrapper Data Width When a ULPI PHY is used, an internal wrapper converts ULPI to UTMI+. 2'b00: 8 bits 2'b01: 16 bits 2'b10: 8/16 bits, software selectable Others: Reserved
13:7	RO	0x0	reserved
6	RO	0x0	EnHiber Enable Hibernation 1'b0: Hibernation feature not enabled 1'b1: Hibernation feature enabled
5	RO	0x0	AhbFreq Minimum AHB Frequency Less Than 60 MHz 1'b0: No 1'b1: Yes
4	RO	0x0	EnParPwrDown Enable Partial Power Down 1'b0: Partial Power Down Not Enabled 1'b1: Partial Power Down Enabled
3:0	RO	0x0	NumDevPerioEps Number of Device Mode Periodic IN Endpoints Range: 0-15

USBOTG_GLPMCFG
Address: Operational Base + offset (0x0054)
Core LPM Configuration Register

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Bit	Attr	Reset Value	Description
31	RW	0x0	InvSelHsic HSIC-Invert Select HSIC The application uses this bit to control the DWC_otg core HSIC enable/disable. This bit overrides and functionally inverts the if_sel_hsic input port signal. If the core operates as non-HSIC-capable, it can only connect to non-HSIC-capable PHYs. If the core operates as HSIC-capable, it can only connect to HSICcapable PHYs. If the if_sel_hsic input signal is1: 1'b1: HSIC capability is not enabled. 1'b0: HSIC capability is enabled, If InvSelHsic = 1'b0: HSIC capability is enabled. If the if_sel_hsic input signal is 0: 1'b1: HSIC capability is enabled, 1'b0: HSIC capability is not enabled. This bit is writable only if an HSIC mode was specified for Mode of Operation (parameter OTG_ENABLE_HSIC). This bit is valid only if OTG_ENABLE_HSIC is enabled.
30	RW	0x0	HSICCon HSIC-Connect The application must use this bit to initiate the HSIC Attach sequence. Host Mode: Once this bit is set, the host core configures to drive the HSIC Idle state (STROBE = 1 & DATA = 0) on the bus. It then waits for the device to initiate the Connect sequence. Device Mode: Once this bit is set, the device core waits for the HSIC Idle line state on the bus. Upon receiving the Idle line state, it initiates the HSIC Connect sequence. This bit is valid only if OTG_ENABLE_HSIC is 1, if_sel_hsic = 1 and InvSelHSIC is 0. Otherwise, it is read-only.
29:28	RO	0x0	reserved
27:25	RO	0x0	LPM_RetryCnt_Sts LPM Retry Count Status Number of LPM host retries remaining to be transmitted for the current LPM sequence.
24	RW	0x0	SndLPM Send LPM Transaction Host Mode: When the application software sets this bit, an LPM transaction containing two tokens, EXT and LPM, is sent. The hardware clears this bit once a valid response (STALL, NYET, or ACK) is received from the device or the core has finished transmitting the programmed number of LPM retries. Note: This bit must only be set when the host is connected to a local port.

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Bit	Attr	Reset Value	Description
23:21	R/WSC	0x0	LPM_Retry_Cnt LPM Retry Count When the device gives an ERROR response, this is the number of additional LPM retries that the host performs until a valid device response (STALL, NYET, or ACK) is received.
20:17	RW	0x0	LPM_Chnl_Indx LPM Channel Index The channel number on which the LPM transaction must be applied while sending an LPM transaction to the local device. Based on the LPM channel index, the core automatically inserts the device address and endpoint number programmed in the corresponding channel into the LPM transaction.
16	RO	0x0	L1ResumeOK Sleep State Resume OK Indicates that the application or host can start a resume from the Sleep state. This bit is valid in the LPM Sleep (L1) state. It is set in Sleep mode after a delay of 50 us (TL1Residency). The bit is reset when SlpSts is 0 1'b1: The application/core can start resume from the Sleep state 1'b0: The application/core cannot start resume from the Sleep state

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Bit	Attr	Reset Value	Description
15	RO	0x0	SlpSts Port Sleep Status Device Mode: This bit is set as long as a Sleep condition is present on the USB bus. The core enters the Sleep state when an ACK response is sent to an LPM transaction and the timer TL1TokenRetry has expired. To stop the PHY clock, the application must set the Port Clock Stop bit, which asserts the PHY Suspend input pin. The application must rely on SlpSts and not ACK in CoreL1Res to confirm transition into sleep. The core comes out of sleep: When there is any activity on the USB line_state, When the application writes to the Remote Wakeup Signaling bit in the Device Control register (DCTL.RmtWkUpSig) or when the application resets or soft-disconnects the device. Host Mode: The host transitions to the Sleep (L1) state as a side-effect of a successful LPM transaction by the core to the local port with an ACK response from the device. The read value of this bit reflects the port's current sleep status. The core clears this bit after: The core detects a remote L1 Wakeup signal, The application sets the Port Reset bit or the Port L1Resume bit in the HPRT register or The application sets the L1Resume/ Remote Wakeup Detected Interrupt bit or Disconnect Detected Interrupt bit in the Core Interrupt register (GINTSTS.L1WkUpInt or GINTSTS.DisconnInt, respectively). Values: 1'b0: Core not in L1 1'b1: Core in L1
14:13	RO	0x0	CoreL1Res LPM Response Device Mode: The core's response to the received LPM transaction is reflected in these two bits. Host Mode: The handshake response received from the local device for LPM transaction. 11: ACK 10: NYET 01: STALL 00: ERROR (No handshake response)

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Bit	Attr	Reset Value	Description
12:8	RW	0x00	HIRD_Thres HIRD Threshold Device Mode: The core asserts L1SuspendM to put the PHY into Deep Low-Power mode in L1 when the HIRD value is greater than or equal to the value defined in this field (GLPMCFG.HIRD_Thres[3:0]), and HIRD_Thres[4] is set to 1'b1. Host Mode: The core asserts L1SuspendM to put the PHY into Deep Low-Power mode in L1 when HIRD_Thres[4] is set to 1'b1. HIRD_Thres[3:0] specifies the time for which resume signaling is to be reflected by the host TL1HubDrvResume2) on the USB when it detects device-initiated resume. HIRD_Thres must not be programmed with a value greater than 4'b1100 in Host mode, because this exceeds maximum TL1HubDrvResume2. Sl. No HIRD_Thres[3:0] Host mode resume time(us) 1 4'b0000 60 2 4'b0001 135 3 4'b0010 210 4 4'b0011 285 5 4'b0100 360 6 4'b0101 435 7 4'b0110 510 8 4'b0111 585 9 4'b1000 660 10 4'b1001 735 11 4'b1010 810 12 4'b1011 885 13 4'b1100 960 14 4'b1101 invalid 15 4'b1110 invalid 16 4'b1111 invalid

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Bit	Attr	Reset Value	Description
7	RW	0x0	EnblSlpM Enable utmi_sleep_n For ULPI interface: The application uses this bit to write to the function control [7] in the L1 state, to enable the PHY to go into Low Power mode. For the host, this bit is valid only in Local Device mode. 1'b0: Writes to the ULPI Function Control Bit[7] are disabled. 1'b1: The core is enabled to write to the ULPI Function Control Bit[7], which enables the PHY to enter Low-Power mode. Note: When a ULPI interface is configured, enabling this bit results in a write to Bit 7 of the ULPI Function Control register. The ULPI PHY supports writing to this bit, and in the L1 state asserts SleepM when utmi_l1_suspend_n cannot be asserted. When a ULPI interface is configured, this bit must always be set if you are using the ULPI PHY. Note: For ULPI interface, do not clear this bit during the resume. For all other interfaces: The application uses this bit to control utmi_sleep_n assertion to the PHY in the L1 state. For the host, this bit is valid only in Local Device mode. 1'b0: utmi_sleep_n assertion from the core is not transferred to the external PHY. 1'b1: utmi_sleep_n assertion from the core is transferred to the external PHY when utmi_l1_suspend_n cannot be asserted.
6	RW	0x0	bRemoteWake RemoteWakeEnable Host Mode: The remote wakeup value to be sent in the LPM transaction's wIndex field. Device Mode: This field is updated with the received bRemoteWake LPM token's bmAttribute when an ACK/NYET/STALL response is sent to an LPM transaction.

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Bit	Attr	Reset Value	Description
5:2	RW	0x0	HIRD Host-Initiated Resume Duration Host Mode: The value of HIRD to be sent in an LPM transaction. This value is also used to initiate resume for a durationL1HubDrvResume1 for host initiated resume. Device Mode: This field is updated with the Received LPM Token HIRD bmAttribute when an ACK/NYET/STALL response is sent to an LPM transaction Sl. No HIRD[3:0] THIRD (us) 1 4'b0000 50 2 4'b0001 125 3 4'b0010 200 4 4'b0011 275 5 4'b0100 350 6 4'b0101 425 7 4'b0110 500 8 4'b0111 575 9 4'b1000 650 10 4'b1001 725 11 4'b1010 800 12 4'b1011 875 13 4'b1100 950 14 4'b1101 1025 15 4'b1110 1100 16 4'b1111 1175
1	RW	0x0	AppL1Res LPM response programmed by application Handshake response to LPM token pre-programmed by device application software. The response depends on GLPMCFG.LPMCap. If GLPMCFG.LPMCap is 1'b0, the core always responds with a NYET. If GLPMCFG.LPMCap is 1'b1, the core responds as follows: 1: ACK. Even though an ACK is pre-programmed, the core responds with an ACK only on a successful LPM transaction. The LPM transaction is successful if: There are no PID/CRC5 errors in both the EXT token and the LPM token (else ERROR); A valid bLinkState = 0001B (L1) is received in the LPM transaction (else STALL); No data is pending in the Transmit queue (else NYET) 0: NYET. The pre-programmed software bit is overridden for response to LPM token when:(1)The received bLinkState is not L1 (STALL response); (2)An error is detected in either of the LPM token packets due to corruption (ERROR response).

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Bit	Attr	Reset Value	Description
0	RW	0x0	LPMCap LPM-Capable The application uses this bit to control the DWC_otg core LPM capabilities. If the core operates as a non-LPM-capable host, it cannot request the connected device/hub to activate LPM mode. If the core operates as a non-LPM-capable device, it cannot respond to any LPM transactions. 1'b0: LPM capability is not enabled. 1'b1: LPM capability is enabled. This bit is writable only if an LPM mode was specified for Mode of Operation (parameter OTG_ENABLE_LPM). Otherwise, reads return 0.

USBOTG_GPWRDN
Address: Operational Base + offset (0x0058)
Global Power Down Register

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	RO	0x00	MultValIdBC Multi Valued ID pin Battery Charger ACA inputs in the following order: Bit 26 - rid_float. Bit 25 - rid_gnd Bit 24 - rid_a Bit 23 - rid_b Bit 22 - rid_c These bits are present only if OTG_BC_SUPPORT = 1. Otherwise, these bits are reserved and will read 5'h0.
23	W1C	0x0	ADPInt ADP Interupt This bit is set whenever there is a ADP event.
22	RO	0x0	BSessVld B Session Valid This field reflects the B session valid status signal from the PHY. 1'b0: B-Valid is 0. 1'b1: B-Valid is 1. This bit is valid only when GPWRDN.PMUActv is 1.

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Bit	Attr	Reset Value	Description
21	RO	0x0	IDDIG This bit indicates the status of the signal IDDIG. The application must read this bit after receiving GPWRDN.StsChngInt and decode based on the previous value stored by the application. Indicates the current mode. 1'b1: Device mode 1'b0: Host mode This bit is valid only when GPWRDN.PMUActv is 1.
20:19	RO	0x0	LineState This field indicates the current linestate on USB as seen by the PMU module. 2'b00: DM = 0, DP = 0. 2'b01: DM = 0, DP = 1. 2'b10: DM = 1, DP = 0. 2'b11: Not-defined. This bit is valid only when GPWRDN.PMUActv is 1.
18	RW	0x0	StsChngIntMsk Mask For StsChng Interrupt
17	W1C	0x0	StsChngInt This field indicates a status change in either the IDDIG or BSessVld signal. 1'b0: No Status change 1'b1: status change detected After receiving this interrupt the application should read the GPWRDN register and interpret the change in IDDIG or BSesVld with respect to the previous value stored by the application.
16	RW	0x0	SRPDetectMsk Mask For SRPDetect Interrupt
15	W1C	0x0	SRPDetect This field indicates that SRP has been detected by the PMU.This field generates an interrupt. After detecting SRP during hibernation the application should not restore the core. The application should get into the initialization process. 1'b0: SRP not detected 1'b1: SRP detected
14	RW	0x0	ConnDetMsk Mask for ConnectDet interrupt This bit is valid only when OTG_EN_PWROPT = 2.
13	W1C	0x0	ConnectDet This field indicates that a new connect has been detected 1'b0: Connect not detected 1'b1: Connect detected This bit is valid only when OTG_EN_PWROPT = 2.

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Bit	Attr	Reset Value	Description
12	RW	0x0	DisconnectDetectMsk Mask For DisconnectDetect Interrupt This bit is valid only when OTG_EN_PWROPT = 2.
11	W1C	0x0	DisconnectDetect This field indicates that Disconnect has been detected by the PMU. This field generates an interrupt. After detecting disconnect during hibernation the application must not restore the core, but instead start the initialization process. 1'b0: Disconnect not detected 1'b1: Disconnect detected This bit is valid only when OTG_EN_PWROPT = 2.
10	RW	0x0	ResetDetMsk Mask For ResetDetected interrupt.This bit is valid only when OTG_EN_PWROPT = 2.
9	W1C	0x0	ResetDetected This field indicates that Reset has been detected by the PMU module. This field generates an interrupt. 1'b0: Reset Not Detected 1'b1: Reset Detected This bit is valid only when OTG_EN_PWROPT = 2.
8	RW	0x0	LineStageChangeMsk Mask For LineStateChange interrupt This bit is valid only when OTG_EN_PWROPT = 2.
7	W1C	0x0	LnStsChng Line State Change This interrupt is asserted when there is a Linestate Change detected by the PMU. The application should read GPWRDN.Linestate to determine the current linestate on USB. 1'b0: No LineState change on USB 1'b1: LineState change on USB This bit is valid only when GPWRDN.PMUActv is 1.This bit is valid only when OTG_EN_PWROPT = 2.
6	RW	0x0	DisableVBUS The application should program this bit if HPRT0.PrtPwr was programmed to 0 before entering Hibernation. This is to indicate PMU whether session was ended before entering Hibernation. 1'b0: HPRT0.PrtPwr was not programmed to 0. 1'b1: HPRT0.PrtPwr was programmed to 0.

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Bit	Attr	Reset Value	Description
5	RW	0x0	PwrDnSwtch Power Down Switch This bit indicates to the DWC_otg core VDD switch is in ON/OFF state 1'b0: DWC_otg is in ON state 1'b1: DWC_otg is in OFF state *Note: This bit must not be written to during normal mode of operation.*
4	RW	0x0	PwrDnRst_n Power Down ResetN The application must program this bit to reset the DWC OTG core during the Hibernation exit process or during ADP when powering up the core (in case the DWC OTG core was powered off during ADP process). 1'b1: DWC_otg is in normal operation 1'b0: reset DWC_otg *Note: This bit must not be written to during normal mode of operation.*
3	RW	0x0	PwrDnClmp Power Down Clamp The application must program this bit to enable or disable the clamps to all the outputs of the DWC OTG core module to prevent the corruption of other active logic. 1'b0: Disable PMU power clamp 1'b1: Enable PMU power clamp
2	RW	0x0	Restore The application should program this bit to enable or disable restore mode from the PMU module. 1'b0: DWC_otg in normal mode of operation 1'b1: DWC_otg in restore mode *Note: This bit must not be written to during normal mode of operation. This bit is valid only when OTG_EN_PWROPT = 2*.
1	RW	0x0	PMUActv PMU Active This is bit is to enable or disable the PMU logic. 1'b0: Disable PMU module 1'b1: Enable PMU module *Note: This bit must not be written to during normal mode of operation.*

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Bit	Attr	Reset Value	Description
0	RW	0x0	PMUIntSel PMU Interrupt Select When the hibernation functionality is selected using the configuration option OTG_EN_PWR_OPT = 2, a write to this bit with 1'b1 enables the PMU to generate interrupts to the application. During this state all interrupts from the core module are blocked to the application. Note: This bit must be set to 1'b1 before the core is put into hibernation 1'b0: Internal DWC_otg_core interrupt is selected 1'b1: the external DWC_otg_pmu interrupt is selected Note: This bit must not be written to during normal mode of operation.

USBOTG_GDFIFOCFG
Address: Operational Base + offset (0x005c)
Global DFIFO Software Config Register

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	EPInfoBaseAddr This field provides the start address of the EP info controller.
15:0	RW	0x0000	GDFIFOCfg This field is for dynamic programming of the DFIFO Size. This value takes effect only when the application programs a non-zero value to this register.The core does not have any corrective logic if the FIFO sizes are programmed incorrectly.

USBOTG_GADPCTL
Address: Operational Base + offset (0x0060)
ADP Timer,Control and Status Register

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:27	R/W SC	0x0	AR Access Request 2'b00 Read/Write Valid (updated by the core) 2'b01 Read 2'b10 Write 2'b11 Reserved
26	RW	0x0	AdpTmoutMsk ADP Timeout Interrupt Mask When this bit is set, it unmasks the interrupt because of AdpTmoutInt. This bit is valid only if OTG_Ver = 1'b1(GOTGCTL[20]).

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Bit	Attr	Reset Value	Description
25	RW	0x0	AdpSnsIntMsk ADP Sense Interrupt Mask When this bit is set, it unmasks the interrupt due to AdpSnsInt. This bit is valid only if OTG_Ver = 1'b1(GOTGCTL[20]).
24	RW	0x0	AdpPrbIntMsk ADP Probe Interrupt Mask When this bit is set, it unmasks the interrupt due to AdpPrbInt.This bit is valid only if OTG_Ver = 1'b1(GOTGCTL[20]).
23	W1C	0x0	AdpTmoutInt ADP Timeout Interrupt This bit is relevant only for an ADP probe. When this bit is set, it means that the ramp time has completed (GADPCTL.RTIM has reached its terminal value of 0x7FF). This is a debug feature that allows software to read the ramp time after each cycle. This bit is valid only if OTG_Ver = 1'b1.
22	W1C	0x0	AdpSnsInt ADP Sense Interrupt When this bit is set, it means that the VBUS voltage is greater than VadpSns value or VadpSns is reached. This bit is valid only if OTG_Ver = 1'b1 (GOTGCTL[20]).
21	W1C	0x0	AdpPrbInt ADP Probe Interrupt When this bit is set, it means that the VBUS voltage is greater than VadpPrb or VadpPrb is reached. This bit is valid only if OTG_Ver = 1'b1 (GOTGCTL[20]).
20	RW	0x0	ADPEn ADP Enable When set, the core performs either ADP probing or sensing based on EnaPrb or EnaSns. This bit is valid only if OTG_Ver = 1'b1 (GOTGCTL[20]).
19	R/W SC	0x0	ADPRes ADP Reset When set, ADP controller is reset. This bit is auto-cleared after the reset procedure is complete in ADP controller.This bit is valid only if OTG_Ver = 1'b1 (GOTGCTL[20]).
18	RW	0x0	EnaSns Enable Sense When programmed to 1'b1, the core performs a sense operation. This bit is valid only if OTG_Ver = 1'b1 (GOTGCTL[20]).
17	RW	0x0	EnaPrb Enable Probe When programmed to 1'b1, the core performs a probe operation. This bit is valid only if OTG_Ver = 1'b1 (GOTGCTL[20]).

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Bit	Attr	Reset Value	Description
16:6	RO	0x000	RTIM RAMP TIME These bits capture the latest time it took for VBUS to ramp from VADP_SINK to VADP_PRB. The bits are defined in units of 32 kHz clock cycles as follows: 0x000 - 1 cycles 0x001 - 2 cycles 0x002 - 3 cycles and so on till 0x7FF - 2048 cycles A time of 1024 cycles at 32 kHz corresponds to a time of 32 msec. (Note for scaledown ramp_timeout = prb_delta == 2'b00 => 200 cycles prb_delta == 2'b01 => 100 cycles prb_delta == 2'b01 => 50 cycles prb_delta == 2'b01 => 25 cycles.)
5:4	RW	0x0	PrbPer Probe Period These bits sets the TadpPrd as follows: 2'b00 - 0.625 to 0.925 sec (typical 0.775 sec) 2'b01 - 1.25 to 1.85 sec (typical 1.55 sec) 2'b10 - 1.9 to 2.6 sec (typical 2.275 sec) 2'b11 - Reserved (PRB_PER is also scaledown prb_per== 2'b00 => 400 ADP clocks prb_per== 2'b01 => 600 ADP clocks prb_per== 2'b10 => 800 ADP clocks prb_per==2'b11 => 1000 ADP clocks)
3:2	RW	0x0	PrbDelta Probe Delta These bits set the resolution for RTIM value. The bits are defined in units of 32 kHz clock cycles as follows: 2'b00 - 1 cycles 2'b01 - 2 cycles 2'b10 - 3 cycles 2'b11 - 4 cycles For example if this value is chosen to 2'b01, it means that RTIM increments forevery three 32Khz clock cycles.

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Bit	Attr	Reset Value	Description
1:0	RW	0x0	PrbDschg Probe Discharge These bits set the times for TadpDschg. These bits are defined as follows: 2'b00 4 msec (Scaledown 2 32Khz clock cycles) 2'b01 8 msec (Scaledown 4 32Khz clock cycles) 2'b10 16 msec (Scaledown 8 32Khz clock cycles) 2'b11 32 msec (Scaledown 16 32Khz clock cycles)

USBOTG_HPTXFSIZ
Address: Operational Base + offset (0x0100)
Host Periodic Transmit FIFO Size Register

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	PTxFSize Host Periodic TxFIFO Depth This value is in terms of 32-bit words. Minimum value is 16 Maximum value is 32,768 The power-on reset value of this register is specified as the Largest Host Mode Periodic Tx Data FIFO Depth (parameter OTG_TX_HPERIO_DFIFO_DEPTH). If Enable Dynamic FIFO Sizing was deselected (parameter OTG_DFIFO_DYNAMIC = 0), these flops are optimized, and reads returnthe power-on value. If Enable Dynamic FIFO Sizing was selected (parameter OTG_DFIFO_DYNAMIC = 1), you can write a new value in this field. Programmed values must not exceed the power-on value set.
15:0	RW	0x0000	PTxFStAddr Host Periodic TxFIFO Start Address The power-on reset value of this register is the sum of the Largest Rx Data FIFO Depth and Largest Non-periodic Tx Data FIFO Depth specified. These parameters are: In shared FIFO operation: OTG_RX_DFIFO_DEPTH + OTG_TX_NPERIO_DFIFO_DEPTH. In dedicated FIFO mode: OTG_RX_DFIFO_DEPTH + OTG_TX_HNPERIO_DFIFO_DEPTH. If Enable Dynamic FIFO Sizing was deselected (parameter OTG_DFIFO_DYNAMIC = 0), these flops are optimized, and reads return the power-on value. If Enable Dynamic FIFO Sizing was selected(parameter OTG_DFIFO_DYNAMIC = 1), you can write a new value in this field.Programmed values must not exceed the power-on value.

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USBOTG_DIEPTXFn
Address: Operational Base + offset (0x0104)
Device Periodic Transmit FIFO-n Size Register

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	INEP1TxFDep IN Endpoint TxFIFO Depth This value is in terms of 32-bit words. Minimum value is 16 Maximum value is 32,768 The power-on reset value of this register is specified as the Largest IN Endpoint FIFO number Depth (parameter OTG_TX_DINEP_DFIFO_DEPTH_n)(0 < n <= 15). If Enable Dynamic FIFO Sizing was deselected (parameter OTG_DFIFO_DYNAMIC = 0), these flops are optimized, and reads return the power-on value. If Enable Dynamic FIFO Sizing was selected (parameter OTG_DFIFO_DYNAMIC = 1), you can write a new value in this field.Programmed values must not exceed the power-on value.
15:0	RW	0x0000	INEP1TxFStAddr IN Endpoint FIFO1 Transmit RAM Start Address This field contains the memory start address for IN endpoint Transmit FIFOn (0 < n <= 15). The power-on reset value of this register is specified as the Largest Rx Data FIFO Depth (parameter OTG_RX_DFIFO_DEPTH). OTG_RX_DFIFO_DEPTH + SUM 0 to n-1 (OTG_DINEP_TXFIFO_DEPTH_n) For example start address of IN endpoint FIFO 1 is OTG_RX_DFIFO_DEPTH + OTG_DINEP_TXFIFO_DEPTH_0. The start address of IN endpoint FIFO 2 is OTG_RX_DFIFO_DEPTH + OTG_DINEP_TXFIFO_DEPTH_0 + OTG_DINEP_TXFIFO_DEPTH_1. If Enable Dynamic FIFO Sizing? was deselected (parameter OTG_DFIFO_DYNAMIC = 0), these flops are optimized, and reads return the power-on value. If Enable Dynamic FIFO Sizing was selected (parameter OTG_DFIFO_DYNAMIC = 1), and you have programmed a new value for RxFIFO depth, you can write that value in this field. Programmed values must not exceed the power-on value set.

USBOTG_HCFG
Address: Operational Base + offset (0x0400)
Host Configuration Register

Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
26	RW	0x0	PerSchedEna Enable Periodic Scheduling Applicable in Scatter/Gather DMA mode only. Enables periodic scheduling within the core. Initially, the bit is reset. The core will not process any periodic channels. As soon as this bit is set, the core will get ready to start scheduling periodic channels and sets HCFG.PerSchedStat. The setting of HCFG.PerSchedStat indicates the core has enabled periodic scheduling. Once HCFG.PerSchedEna is set, the application is not supposed to again reset the bit unless HCFG.PerSchedStat is set. As soon as this bit is reset, the core will get ready to stop scheduling periodic channels and resets HCFG.PerSchedStat. In non Scatter/Gather DMA mode, this bit is reserved.
25:24	RW	0x0	FrListEn Frame List Entries The value in the register specifies the number of entries in the Frame list. This field is valid only in Scatter/Gather DMA mode.
23	RW	0x0	DescDMA Enable Scatter/gather DMA in Host mode When the Scatter/Gather DMA option selected during configuration of the RTL, the application can set this bit during initialization to enable the Scatter/Gather DMA operation. NOTE: This bit must be modified only once after a reset. The following combinations are available for programming: GAHBCFG.DMAEn=0, HCFG.DescDMA=0 => Slave mode GAHBCFG.DMAEn=0, HCFG.DescDMA=1 => Invalid GAHBCFG.DMAEn=1, HCFG.DescDMA=0 => Buffered DMA mode GAHBCFG.DMAEn=1, HCFG.DescDMA=1 => Scatter/Gather DMA mode In non-Scatter/Gather DMA mode, this bit is reserved.
22:16	RO	0x0	reserved
15:8	RW	0x00	ResValid Resume Validation Period This field is effective only when HCFG.Ena32KHzS is set. It controls the resume period when the core resumes from suspend. The core counts the ResValid number of clock cycles to detect a valid resume when this is set.
7	RW	0x0	Ena32KHzS Enable 32-KHz Suspend Mode This bit can only be set if the USB 1.1 Full-Speed Serial Transceiver Interface has been selected. If USB 1.1 Full-Speed Serial Transceiver Interface has not been selected, this bit must be zero. When the USB 1.1 Full-Speed Serial Transceiver Interface is chosen and this bit is set, the core expects the 48-MHz PHY clock to be switched to 32 KHz during a suspend.

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Bit	Attr	Reset Value	Description
6:3	RO	0x0	reserved
2	RW	0x0	FSLSSupp FS- and LS-Only Support The application uses this bit to control the core enumeration speed. Using this bit, the application can make the core enumerate as a FS host, even if the connected device supports HS traffic. Do not make changes to this field after initial programming. 1'b0: HS/FS/LS, based on the maximum speed supported by the connected device 1'b1: FS/LS-only, even if the connected device can support HS
1:0	RW	0x0	FSLSPclkSel FS/LS PHY Clock Select 2'b00: PHY clock is running at 30/60 MHz 2'b01: PHY clock is running at 48 MHz Others: Reserved

USBOTG_HFIR
Address: Operational Base + offset (0x0404)
Host Frame Interval Register

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0000	FrInt Frame Interval The value that the application programs to this field specifies the interval between two consecutive SOFs (FS) or micro-SOFs (HS) or Keep-Alive tokens (HS). This field contains the number of PHY clocks that constitute the required frame interval. The default value set in this field for a FS operation when the PHY clock frequency is 60MHz. The application can write a value to this register only after the Port Enable bit of the Host Port Control and Status register (HPRT.PrtEnaPort) has been set. If no value is programmed, the core calculates the value based on the PHY clock specified in the FS/LS PHY Clock Select field of the Host Configuration register (HCFG.FSLSPclkSel). Do not change the value of this field after the initial configuration. 125 us * (PHY clock frequency for HS) 1 ms * (PHY clock frequency for FS/LS)

USBOTG_HFNUM
Address: Operational Base + offset (0x0408)

Host Frame Number/Frame Time Remaining Register

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	FrRem Frame Time Remaining Indicates the amount of time remaining in the current microframe (HS) or frame (FS/LS), in terms of PHY clocks. This field decrement on each PHY clock. When it reaches zero, this field is reloaded with the value in the Frame Interval register and a new SOF is transmitted on the USB.
15:0	RO	0xffff	FrNum Frame Number This field increment when a new SOF is transmitted on the USB, and is reset to 0 when it reaches 16'h3FFF. This field is writable only if Remove Optional Features was not selected (OTG_RM_OTG_FEATURES = 0). Otherwise, reads return the frame number value.

USBOTG_HPTXSTS

Address: Operational Base + offset (0x0410)

Host Periodic Transmit FIFO/Queue Status Register

Bit	Attr	Reset Value	Description
31:24	RO	0x00	PTxQTop Top of the Periodic Transmit Request Queue This indicates the entry in the Periodic Tx Request Queue that is currently being processes by the MAC. This register is used for debugging. Bit [31]: Odd/Even (micro)frame 1'b0: send in even (micro)frame 1'b1: send in odd (micro)frame Bits [30:27]: Channel/endpoint number Bits [26:25]: Type 2'b00: IN/OUT 2'b01: Zero-length packet 2'b10: CSPLIT 2'b11: Disable channel command Bit [24]: Terminate (last entry for the selected channel/endpoint)
23:16	RO	0x00	PTxQSpcAvail Periodic Transmit Request Queue Space Available Indicates the number of free locations available to be written in the Periodic Transmit Request Queue. This queue holds both IN and OUT requests. 8'h0: Periodic Transmit Request Queue is full 8'h1: 1 location available 8'h2: 2 locations available n: n locations available (0 <=n <= 16) Others: Reserved

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Bit	Attr	Reset Value	Description
15:0	RW	0x0000	PTxFSpcAvail Periodic Transmit Data FIFO Space Available Indicates the number of free locations available to be written to in the Periodic TxFIFO. Values are in terms of 32-bit words 16'h0: Periodic TxFIFO is full 16'h1: 1 word available 16'h2: 2 words available 16'hn: n words available (where 0 . n . 32,768) 16'h8000: 32,768 words available Others: Reserved

USBOTG_HAINT
Address: Operational Base + offset (0x0414)
Host All Channels Interrupt Reigster

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RO	0x0000	HAINT Channel Interrupts One bit per channel: Bit 0 for Channel 0, bit 15 for Channel 15

USBOTG_HAINTMSK
Address: Operational Base + offset (0x0418)
Host All Channels Interrupt Mask Register

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0000	HAINTMsk Channel Interrupt Mask One bit per channel: Bit 0 for channel 0, bit 15 for channel 15

USBOTG_HPRT
Address: Operational Base + offset (0x0440)
Host Port Control and Status Register

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:17	RO	0x0	PrtSpd Port Speed Indicates the speed of the device attached to this port. 2'b00: High speed 2'b01: Full speed 2'b10: Low speed 2'b11: Reserved

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Bit	Attr	Reset Value	Description
16:13	RW	0x0	PrtTstCtl Port Test Control The application writes a nonzero value to this field to put the port into a Test mode,and the corresponding pattern is signaled on the port. 4'b0000: Test mode disabled 4'b0001: Test_J mode 4'b0010: Test_K mode 4'b0011: Test_SE0_NAK mode 4'b0100: Test_Packet mode 4'b0101: Test_Force_Enable Others: Reserved
12	R/WSC	0x0	PrtPwr Port Power The application uses this field to control power to this port (write 1'b1 to set to 1'b1and write 1'b0 to set to 1'b0), and the core can clear this bit on an over current condition. 1'b0: Power off 1'b1: Power on
11:10	RO	0x0	PrtLnSts Port Line Status Indicates the current logic level USB data lines Bit [10]: Logic level of D+ Bit [11]: Logic level of D
9	RO	0x0	reserved
8	RW	0x0	PrtRst Port Reset When the application sets this bit, a reset sequence is started on this port. The application must time the reset period and clear this bit after the reset sequence is complete. 1'b0: Port not in reset 1'b1: Port in reset To start a reset on the port, the application must leave this bit set for at least the minimum duration mentioned below, as specified in the USB 2.0 specification, Section 7.1.7.5. The application can leave it set for another 10 ms in addition to the required minimum duration, before clearing the bit, even though there is no maximum limit set by the USB standard. High speed: 50 ms Full speed/Low speed: 10 ms

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Bit	Attr	Reset Value	Description
7	R/W SC	0x0	PrtSusp Port Suspend The application sets this bit to put this port in Suspend mode. The core only stops sending SOFs when this is set. To stop the PHY clock, the application must set the Port Clock Stop bit, which asserts suspend input pin of the PHY. The read value of this bit reflects the current suspend status of the port. This bit is cleared by the core after a remote wakeup signal is detected or the application sets the Port Reset bit or Port Resume bit in this register or the Resume/Remote Wakeup Detected Interrupt bit or Disconnect Detected Interrupt bit in the Core Interrupt register (GINTSTS.WkUpInt or GINTSTS.DisconnInt, respectively). 1'b0: Port not in Suspend mode 1'b1: Port in Suspend mode
6	R/W SC	0x0	PrtRes Port Resume The application sets this bit to drive resume signaling on the port. The core continues to drive the resume signal until the application clears this bit. If the core detects a USB remote wakeup sequence, as indicated by the Port Resume/Remote Wakeup Detected Interrupt bit of the Core Interrupt register (GINTSTS.WkUpInt), the core starts driving resume signaling without application intervention and clears this bit when it detects a disconnect condition. The read value of this bit indicates whether the core is currently driving resume signaling. 1'b0: No resume driven 1'b1: Resume driven When LPM is enabled and the core is in the L1 (Sleep) state, setting this bit results in the following behavior: The core continues to drive the resume signal until a pre-determined time specified in the GLPMCFG.HIRD_Thres[3:0] field. If the core detects a USB remote wakeup sequence, as indicated by the Port L1 Resume/Remote L1 Wakeup Detected Interrupt bit of the Core Interrupt register (GINTSTS.L1WkUpInt), the core starts driving resume signaling without application intervention and clears this bit at the end of the resume. The read value of this bit indicates whether the core is currently driving resume signaling. 1'b0: No resume driven 1'b1: Resume driven

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Bit	Attr	Reset Value	Description
5	W1C	0x0	PrtOvrCurrChng Port Overcurrent Change The core sets this bit when the status of the Port Over-current Active bit (bit 4) in this register changes.
4	RO	0x0	PrtOvrCurrAct Port Overcurrent Active Indicates the overcurrent condition of the port. 1'b0: No overcurrent condition 1'b1: Overcurrent condition
3	W1C	0x0	PrtEnChng Port Enable/Disable Change The core sets this bit when the status of the Port_Enable bit[2] of this register changes.
2	W1C	0x0	PrtEna Port Enable A port is enabled only by the core after a reset sequence, and is disabled by an over-current condition, a disconnect condition, or by the application clearing this bit. The application cannot set this bit by a register write. It can only clear it to disable the port. This bit does not trigger any interrupt to the application. 1'b0: Port disabled 1'b1: Port enabled
1	W1C	0x0	PrtConnDet Port Connect Detected The core sets this bit when a device connection is detected to trigger an interrupt to the application using the Host Port Interrupt bit of the Core Interrupt register (GINTSTS.PrtInt). The application must write a 1 to this bit to clear the interrupt.
0	RO	0x0	PrtConnSts Port Connect Status 0: No device is attached to the port. 1: A device is attached to the port.

USBOTG_HCCHARn
Address: Operational Base + offset (0x0500)
Host Channel-n Characteristics Register

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Bit	Attr	Reset Value	Description
31	R/W SC	0x0	ChEna Channel Enable When Scatter/Gather mode is enabled 1'b0: Indicates that the descriptor structure is not yet ready. 1'b1: Indicates that the descriptor structure and data buffer with data is setup and this channel can access the descriptor. When Scatter/Gather mode is disabled, This field is set by the application and cleared by the OTG host. 1'b0: Channel disabled 1'b1: Channel enabled
30	R/W SC	0x0	ChDis Channel Disable The application sets this bit to stop transmitting/receiving data on a channel, even before the transfer for that channel is complete. The application must wait for the Channel Disabled interrupt before treating the channel as disabled.
29	RW	0x0	OddFrm Odd Frame This field is set (reset) by the application to indicate that the OTG host must perform a transfer in an odd (micro) frame. This field is applicable for only periodic (isochronous and interrupt) transactions. 1'b0: Even (micro)frame 1'b1: Odd (micro)frame This field is not applicable for Scatter/Gather DMA mode and need not be programmed by the application and is ignored by the core.
28:22	RW	0x00	DevAddr Device Address This field selects the specific device serving as the data source or sink.

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Bit	Attr	Reset Value	Description
21:20	RW	0x0	MC_EC Multi Count (MC) / Error Count (EC) When the Split Enable bit of the Host Channel-n Split Control register (HCSPLTn.SpltEna) is reset (1'b0), this field indicates to the host the number of transactions that must be executed per microframe for this periodic endpoint. For non-periodic transfers, this field is used only in DMA mode, and specifies the number packets to be fetched for this channel before the internal DMA engine changes arbitration. 2'b00: Reserved This field yields undefined results. 2'b01: 1 transaction 2'b10: 2 transactions to be issued for this endpoint per micro-frame 2'b11: 3 transactions to be issued for this endpoint per micro-frame When HCSPLTn.SpltEna is set (1'b1), this field indicates the number of immediate retries to be performed for a periodic split transactions on transaction errors. This field must be set to at least 2'b01.
19:18	RW	0x0	EPType Endpoint Type Indicates the transfer type selected. 2'b00: Control 2'b01: Isochronous 2'b10: Bulk 2'b11: Interrupt
17	RW	0x0	LSpdDev Low-Speed Device This field is set by the application to indicate that this channel is communicating to a low-speed device.
16	RO	0x0	reserved
15	RW	0x0	EPDir Endpoint Direction Indicates whether the transaction is IN or OUT. 1'b0: OUT 1'b1: IN
14:11	RW	0x0	EPNum Endpoint Number Indicates the endpoint number on the device serving as the data source or sink.
10:0	RW	0x000	MPS Maximum Packet Size Indicates the maximum packet size of the associated endpoint.

USBOTG_HCSPLTn

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Address: Operational Base + offset (0x0504)
Host Channel-n Split Control Register

Bit	Attr	Reset Value	Description
31	RW	0x0	SpltEna Split Enable The application sets this field to indicate that this channel is enabled to perform split transactions.
30:17	RO	0x0	reserved
16	RW	0x0	CompSplt Do Complete Split The application sets this field to request the OTG host to perform a complete split transaction.
15:14	RW	0x0	XactPos Transaction Position This field is used to determine whether to send all, first, middle, or last payloads with each OUT transaction. 2'b11: All. This is the entire data payload is of this transaction (which is less than or equal to 188 bytes). 2'b10: Begin. This is the first data payload of this transaction (which is larger than 188 bytes). 2'b00: Mid. This is the middle payload of this transaction (which is larger than 188bytes). 2'b01: End. This is the last payload of this transaction (which is larger than 188 bytes).
13:7	RW	0x00	HubAddr Hub Address This field holds the device address of the transaction translator's hub.
6:1	RO	0x0	reserved
0	RW	0x0	PrtAddr Port Address This field is the port number of the recipient transaction translator.

USBOTG_HCINTn
Address: Operational Base + offset (0x0508)
Host Channel-n Interrupt Register

Bit	Attr	Reset Value	Description
31:14	RO	0x0	reserved
13	W1C	0x0	DESC_LST_ROLLIntr Descriptor rollover interrupt This bit is valid only when Scatter/Gather DMA mode is enabled. The core sets this bit when the corresponding channel's descriptor list rolls over. For non-Scatter/Gather DMA mode, this bit is reserved.

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Bit	Attr	Reset Value	Description
12	W1C	0x0	XCS_XACT_ERR Excessive Transaction Error This bit is valid only when Scatter/Gather DMA mode is enabled. The core sets this bit when 3 consecutive transaction errors occurred on the USB bus. XCS_XACT_ERR will not be generated for Isochronous channels. For non-Scatter/Gather DMA mode, this bit is reserved.
11	W1C	0x0	BNAIntr BNA (Buffer Not Available) Interrupt This bit is valid only when Scatter/Gather DMA mode is enabled. The core generates this interrupt when the descriptor accessed is not ready for the Core to process. BNA will not be generated for Isochronous channels. For non-Scatter/Gather DMA mode, this bit is reserved.
10	W1C	0x0	DataTglErr Data Toggle Error In Scatter/Gather DMA mode, the interrupt due to this bit is masked in the core.
9	W1C	0x0	FrmOvrun Frame Overrun In Scatter/Gather DMA mode, the interrupt due to this bit is masked in the core
8	W1C	0x0	BblErr Babble Error In Scatter/Gather DMA mode, the interrupt due to this bit is masked in the core.
7	W1C	0x0	XactErr Transaction Error Indicates one of the following errors occurred on the USB: CRC check failure, Timeout, Bit stuff error, False EOP. In Scatter/Gather DMA mode, the interrupt due to this bit is masked in the core.
6	WO	0x0	NYET NYET Response Received Interrupt In Scatter/Gather DMA mode, the interrupt due to this bit is masked in the core.
5	W1C	0x0	ACK ACK Response Received/Transmitted Interrupt In Scatter/Gather DMA mode, the interrupt due to this bit is masked in the core.
4	W1C	0x0	NAK NAK Response Received Interrupt In Scatter/Gather DMA mode, the interrupt due to this bit is masked in the core.

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Bit	Attr	Reset Value	Description
3	W1C	0x0	STALL STALL Response Received Interrupt In Scatter/Gather DMA mode, the interrupt due to this bit is masked in the core.
2	W1C	0x0	AHBErr AHB Error This is generated only in DMA mode when there is an AHB error during AHB read/write. The application can read the corresponding channel's DMA address register to get the error address.
1	W1C	0x0	ChHltd Channel Halted In non-Scatter/Gather DMA mode, it indicates the transfer completed abnormally either because of any USB transaction error or in response to disable request by the application or because of a completed transfer. In Scatter/Gather DMA mode, this indicates that transfer completed due to any of the following: EOL being set in descriptor, AHB error, Excessive transaction errors, In response to disable request by the application, Babble, Stall, Buffer Not Available (BNA)
0	W1C	0x0	XferCompl Transfer Completed For Scatter/Gather DMA mode, it indicates that current descriptor processing got completed with IOC bit set in its descriptor. In non-Scatter/Gather DMA mode, it indicates that Transfer completed normally without any errors.

USBOTG_HCINTMSKn

Address: Operational Base + offset (0x050c)

Host Channel-n Interrupt Mask Register

Bit	Attr	Reset Value	Description
31:14	RO	0x0	reserved
13	RW	0x0	DESC_LST_ROLLIntrMsk Descriptor rollover interrupt Mask register This bit is valid only when Scatter/Gather DMA mode is enabled. In non-Scatter/Gather DMA mode, this bit is reserved.
12	RO	0x0	reserved
11	RW	0x0	BNAIntrMsk BNA (Buffer Not Available) Interrupt mask register This bit is valid only when Scatter/Gather DMA mode is enabled. In non-Scatter/Gather DMA mode, this bit is reserved.
10	RW	0x0	DataTglErrMsk Data Toggle Error Mask This bit is not applicable in Scatter/Gather DMA mode.

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Bit	Attr	Reset Value	Description
9	RW	0x0	FrmOvrunMsk Frame Overrun Mask This bit is not applicable in Scatter/Gather DMA mode.
8	RW	0x0	BblErrMsk Babble Error Mask This bit is not applicable in Scatter/Gather DMA mode.
7	RW	0x0	XactErrMsk Transaction Error Mask This bit is not applicable in Scatter/Gather DMA mode
6	RW	0x0	NyetMsk NYET Response Received Interrupt Mask This bit is not applicable in Scatter/Gather DMA mode.
5	RW	0x0	AckMsk ACK Response Received/Transmitted Interrupt Mask This bit is not applicable in Scatter/Gather DMA mode.
4	RW	0x0	NakMsk NAK Response Received Interrupt Mask This bit is not applicable in Scatter/Gather DMA mode.
3	RW	0x0	StallMsk STALL Response Received Interrupt Mask This bit is not applicable in Scatter/Gather DMA mode.
2	RW	0x0	AHBErrMsk AHB Error Mask Note: This bit is only accessible when OTG_ARCHITECTURE = 2
1	RW	0x0	ChHltdMsk Channel Halted Mask
0	RW	0x0	XferComplMsk Transfer Completed Mask This bit is valid only when Scatter/Gather DMA mode is enabled. In non-Scatter/Gather DMA mode, this bit is reserved.

USBOTG_HCTSIZn

Address: Operational Base + offset (0x0510)

Host Channel-n Transfer Size Register

Bit	Attr	Reset Value	Description
31	RW	0x0	DoPng Do Ping This bit is used only for OUT transfers. Setting this field to 1 directs the host to do PING protocol. Note: Do not set this bit for IN transfers. If this bit is set for IN transfers it disables the channel.

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Bit	Attr	Reset Value	Description
30:29	RW	0x0	Pid PID The application programs this field with the type of PID to use for the initial transaction. The host maintains this field for the rest of the transfer. 2'b00: DATA0 2'b01: DATA2 2'b10: DATA1 2'b11: MDATA (non-control)/SETUP (control)
28:19	RW	0x000	PktCnt Packet Count This field is programmed by the application with the expected number of packets to be transmitted (OUT) or received (IN).The host decrements this count on every successful transmission or reception of an OUT/IN packet. Once this count reaches zero, the application is interrupted to indicate normal completion. The width of this counter is specified as Width of Packet Counters (parameter OTG_PACKET_COUNT_WIDTH).
18:0	RW	0x00000	XferSize Transfer Size For an OUT, this field is the number of data bytes the host sends during the transfer. For an IN, this field is the buffer size that the application has Reserved for the transfer. The application is expected to program this field as an integer multiple of the maximum packet size for IN transactions (periodic and non-periodic). The width of this counter is specified as Width of Transfer Size Counters (parameter OTG_TRANS_COUNT_WIDTH).

USBOTG_HCDMAn
Address: Operational Base + offset (0x0514)
Host Channel-n DMA Address Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	DMAAddr DMA Address This field holds the start address in the external memory from which the data for the endpoint must be fetched or to which it must be stored. This register is incremented on every AHB transaction.

USBOTG_HCDMABn
Address: Operational Base + offset (0x051c)
Host Channel-n DMA Buffer Address Register

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Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	HCDMABn Holds the current buffer address This register is updated as and when the data transfer for the corresponding end point is in progress. This register is present only in Scatter/Gather DMA mode. Otherwise this field is reserved.

USBOTG_DCFG
Address: Operational Base + offset (0x0800)
Device Cconfiguration Register

Bit	Attr	Reset Value	Description
31:26	RW	0x02	ResValid Resume Validation Period This field controls the period when the core resumes from a suspended. When this bit is set, the core counts for the Resume Valid number of clock cycles to detect a valid resume. This field is effective only when DCFG.Ena32KHzSusp is set.
25:24	RW	0x0	PerSchIntvl Periodic Scheduling Interval PerSchIntvl must be programmed only for Scatter/Gather DMA mode. Description: This field specifies the amount of time the Internal DMA engine must allocate for fetching periodic IN endpoint data. Based on the number of periodic endpoints, this value must be specified as 25, 50 or 75% of (micro) frame. When any periodic endpoints are active, the internal DMA engine allocates the specified amount of time in fetching periodic IN endpoint data. When no periodic endpoints are active, then the internal DMA engine services non-periodic endpoints, ignoring this field. After the specified time within a (micro) frame, the DMA switches to fetching for non-periodic endpoints. 2'b00: 25% of (micro) frame. 2'b01: 50% of (micro) frame. 2'b10: 75% of (micro) frame. 2'b11: Reserved.

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Bit	Attr	Reset Value	Description
23	RW	0x0	DescDMA Enable Scatter/Gather DMA in Device mode When the Scatter/Gather DMA option selected during configuration of the RTL, the application can set this bit during initialization to enable the Scatter/Gather DMA operation. NOTE: This bit must be modified only once after a reset. The following combinations are available for programming: GAHBCFG.DMAEn=0,DCFG.DescDMA=0 => Slave mode GAHBCFG.DMAEn=0,DCFG.DescDMA=1 => Invalid GAHBCFG.DMAEn=1,DCFG.DescDMA=0 => Buffered DMA mode GAHBCFG.DMAEn=1,DCFG.DescDMA=1 => Scatter/Gather DMA mode
22:18	RW	0x08	EPMisCnt IN Endpoint Mismatch Count This field is valid only in shared FIFO operation. The application programs this filed with a count that determines when the core generates an Endpoint Mismatch interrupt (GINTSTS.EPMis). The core loads this value into an internal counter and decrements it. The counter is reloaded whenever there is a match or when the counter expires. The width of this counter depends on the depth of the Token Queue.
17:13	RO	0x0	reserved
12:11	RW	0x0	PerFrInt Periodic Frame Interval Indicates the time within a (micro) frame at which the application must be notified using the End Of Periodic Frame Interrupt. This can be used to determine if all the isochronous traffic for that (micro) frame is complete. 2'b00: 80% of the (micro) frame interval 2'b01: 85% 2'b10: 90% 2'b11: 95%
10:4	RW	0x00	DevAddr Device Address The application must program this field after every SetAddress control command.
3	RW	0x0	Ena32KHzS Enable 32-KHz Suspend Mode When the USB 1.1 Full-Speed Serial Transceiver Interface is chosen and this bit is set, the core expects the 48-MHz PHY clock to be switched to 32 KHz during a suspend. This bit can only be set if USB 1.1 Full-Speed Serial Transceiver Interface has been selected. If USB 1.1 Full-Speed Serial Transceiver Interface has not been selected, this bit must be zero.

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Bit	Attr	Reset Value	Description
2	RW	0x0	NZStsOUTHShk Non-Zero-Length Status OUT Handshake The application can use this field to select the handshake the core sends on receiving a nonzero-length data packet during the OUT transaction of a control transfer's Status stage. 1'b1: Send a STALL handshake on a nonzero-length status OUT transaction and do not send the received OUT packet to the application. 1'b0: Send the received OUT packet to the application (zero-length or non-zero length) and send a handshake based on the NAK and STALL bits for the endpoint in the Device Endpoint Control register.
1:0	RW	0x0	DevSpd Device Speed Indicates the speed at which the application requires the core to enumerate, or the maximum speed the application can support. However, the actual bus speed is determined only after the chirp sequence is completed, and is based on the speed of the USB host to which the core is connected. 2'b00: High speed (USB 2.0 PHY clock is 30 MHz or 60 MHz) 2'b01: Full speed (USB 2.0 PHY clock is 30 MHz or 60 MHz) 2'b10: Reserved 2'b11: Full speed (USB 1.1 transceiver clock is 48 MHz)

USBOTG_DCTL
Address: Operational Base + offset (0x0804)
Device Control Register

Bit	Attr	Reset Value	Description
31:17	RO	0x0	reserved
16	RW	0x0	NakOnBble Set NAK automatically on babble The core sets NAK automatically for the endpoint on which babble is received.

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Bit	Attr	Reset Value	Description
15	RW	0x0	IgnrFrmNum Ignore frame number for isochronous endpoints in case of Scatter Do NOT program IgnrFrmNum bit to 1'b1 when the core is operating in Threshold mode. Note: When Scatter/Gather DMA mode is enabled this feature is not applicable to high speed, high-bandwidth transfers. When this bit is enabled, there must be only one packet per descriptor. 0: The core transmits the packets only in the frame number in which they are intended to be transmitted. 1: The core ignores the frame number, sending packets immediately as the packets are ready. Scatter/Gather: In Scatter/Gather DMA mode, when this bit is enabled, the packets are not flushed when an ISOC IN token is received for an elapsed frame. When Scatter/Gather DMA mode is disabled, this field is used by the application to enable periodic transfer interrupt. The application can program periodic endpoint transfers for multiple micro) frames. 0: Periodic transfer interrupt feature is disabled; the application must program transfers for periodic endpoints every (micro)frame 1: Periodic transfer interrupt feature is enabled; the application can program transfers for multiple (micro) frames for periodic endpoints. In non-Scatter/Gather DMA mode, the application receives transfer complete interrupt after transfers for multiple (micro) frames are completed.
14:13	RW	0x1	GMC Global Multi Count GMC must be programmed only once after initialization. Applicable only for Scatter/Gather DMA mode. This indicates the number of packets to be serviced for that end point before moving to the next end point. It is only for non-periodic endpoints. 2'b00: Invalid. 2'b01: 1 packet. 2'b10: 2 packets. 2'b11: 3 packets. When Scatter/Gather DMA mode is disabled, this field is reserved, and reads 2'b00.
12	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
11	RW	0x0	PWROnPrgDone Power-On Programming Done The application uses this bit to indicate that register programming is completed after a wake-up from Power Down mode.
10	WO	0x0	CGOUTNak Clear Global OUT NAK A write to this field clears the Global OUT NAK.
9	WO	0x0	SGOUTNak Set Global OUT NAK A write to this field sets the Global OUT NAK. The application uses this bit to send a NAK handshake on all OUT endpoints. The application must set this bit only after making sure that the Global OUT NAK Effective bit in the Core Interrupt Register (GINTSTS.GOUTNakEff) is cleared.
8	WO	0x0	CGNPInNak Clear Global Non-periodic IN NAK A write to this field clears the Global Non-periodic IN NAK.
7	WO	0x0	SGNPInNak Set Global Non-periodic IN NAK A write to this field sets the Global Non-periodic IN NAK.The application uses this bit to send a NAK handshake on all non-periodic IN endpoints. The core can also set this bit when a timeout condition is detected on a non-periodic endpoint in shared FIFO operation. The application must set this bit only after making sure that the Global IN NAK Effective bit in the Core Interrupt Register (GINTSTS.GINNakEff) is cleared.
6:4	RW	0x0	TstCtl Test Control 3'b000: Test mode disabled 3'b001: Test_J mode 3'b010: Test_K mode 3'b011: Test_SE0_NAK mode 3'b100: Test_Packet mode 3'b101: Test_Force_Enable Others: Reserved
3	RO	0x0	GOUTNakSts Global OUT NAK Status 1'b0: A handshake is sent based on the FIFO Status and the NAK and STALL bit settings. 1'b1: No data is written to the RxFIFO, irrespective of space availability. Sends a NAK handshake on all packets, except on SETUP transactions. All isochronous OUT packets are dropped

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Bit	Attr	Reset Value	Description
2	RO	0x0	GNPINNakSts Global Non-periodic IN NAK Status 1'b0: A handshake is sent out based on the data availability in the transmit FIFO. 1'b1: A NAK handshake is sent out on all non-periodic IN endpoints, irrespective of the data availability in the transmit FIFO.
1	RW	0x0	SftDiscon Soft Disconnect The application uses this bit to signal the DWC_otg core to do a soft disconnect. As long as this bit is set, the host does not see that the device is connected, and the device does not receive signals on the USB. The core stays in the disconnected state until the application clears this bit. 1'b0: Normal operation. When this bit is cleared after a soft disconnect, the core drives the phy_opmode_o signal on the UTMI+ to 2'b00, which generates a device connect event to the USB host. When the device is reconnected, the USB host restarts device enumeration. 1'b1: The core drives the phy_opmode_o signal on the UTMI+ to 2'b01, which generates a device disconnect event to the USB host.
0	RW	0x0	RmtWkUpSig Remote Wakeup Signaling When the application sets this bit, the core initiates remote signaling to wake the USB host. The application must set this bit to instruct the core to exit the Suspend state. As specified in the USB 2.0 specification, the application must clear this bit 1ms after setting it. If LPM is enabled and the core is in the L1 (Sleep) state, when the application sets this bit, the core initiates L1 remote signaling to wake up the USB host. The application must set this bit to instruct the core to exit the Sleep state. As specified in the LPM specification, the hardware automatically clears this bit 50 us (TL1DevDrvResume) after being set by the application. The application must not set this bit when GLPMCFG bRemoteWake from the previous LPM transaction is zero.

USBOTG_DSTS

Address: Operational Base + offset (0x0808)

Device Status Register

Bit	Attr	Reset Value	Description
31:22	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
21:8	RW	0x0000	SOFFN Frame or Micro-frame Number of the Received SOF When the core is operating at high speed, this field contains a micro-frame number. When the core is operating at full or low speed, this field contains a frame number.
7:4	RO	0x0	reserved
3	RW	0x0	ErrticErr Erratic Error The core sets this bit to report any erratic errors (phy_rxvalid_i/phy_rxvldh_i or phy_rxactive_i is asserted for at least 2ms, due to PHY error) seen on the UTMI+. Due to erratic errors, the DWC_otg core goes into Suspended state and an interrupt is generated to the application with Early Suspend bit of the Core Interrupt register (GINTSTS.ErlySusp). If the early suspend is asserted due to an erratic error, the application can only perform a soft disconnect recover.
2:1	RW	0x0	EnumSpd Enumerated Speed Indicates the speed at which the DWC_otg core has come up after speed detection through a chirp sequence. 2'b00: High speed (PHY clock is running at 30 or 60 MHz) 2'b01: Full speed (PHY clock is running at 30 or 60 MHz) 2'b10: Low speed (PHY clock is running at 48 MHz, internal phy_clk at 6 MHz) 2'b11: Full speed (PHY clock is running at 48 MHz) Low speed is not supported for devices using a UTMI+ PHY.
0	RW	0x0	SuspSts Suspend Status In Device mode, this bit is set as long as a Suspend condition is detected on the USB. The core enters the Suspended state when there is no activity on the utmi_linestate signal for an extended period of time. The core comes out of the suspend: When there is any activity on the utmi_linestate signal, When the application writes to the Remote Wakeup Signaling bit in the Device Control register (DCTL.RmtWkUpSig).

USBOTG_DIEPMSK

Address: Operational Base + offset (0x0810)

Device IN Endpoint common interrupt mask register

Bit	Attr	Reset Value	Description
31:14	RO	0x0	reserved
13	RW	0x0	NAKMsk NAK interrupt Mask
12:10	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
9	RW	0x0	BNAInIntrMsk BNA Interrupt Mask
8	RW	0x0	TxfifoUndrnMsk Fifo Underrun Mask
7	RO	0x0	reserved
6	RW	0x0	INEPNakEffMsk IN Endpoint NAK Effective Mask
5	RW	0x0	INTknEPMisMsk IN Token received with EP Mismatch Mask
4	RW	0x0	INTknTXFEmpMsk IN Token Received When TxFIFO Empty Mask
3	RW	0x0	TimeOUTMsk Timeout Condition Mask
2	RW	0x0	AHBErrMsk AHB Error Mask
1	RW	0x0	EPDisbldMsk Endpoint Disabled Interrupt Mask
0	RW	0x0	XferComplMsk Transfer Completed Interrupt Mask

USBOTG_DOEPMSK
Address: Operational Base + offset (0x0814)
Device OUT Endpoint common interrupt mask register

Bit	Attr	Reset Value	Description
31:15	RO	0x0	reserved
14	RW	0x0	NYETMsk NYET Interrupt Mask
13	RW	0x0	NAKMsk NAK Interrupt Mask
12	RW	0x0	BbleErrMsk Babble Interrupt Mask
11:10	RO	0x0	reserved
9	RW	0x0	BnaOutIntrMsk BNA interrupt Mask
8	RW	0x0	OutPktErrMsk OUT Packet Error Mask
7	RO	0x0	reserved
6	RW	0x0	Back2BackSETup Back-to-Back SETUP Packets Received Mask Applies to control OUT endpoints only.
5	RO	0x0	reserved
4	RW	0x0	OUTTknEPdisMsk OUT Token Received when Endpoint Disabled Mask Applies to control OUT endpoints only.

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Bit	Attr	Reset Value	Description
3	RW	0x0	SetUPMsk SETUP Phase Done Mask Applies to control endpoints only.
2	RW	0x0	AHBErrMsk AHB Error
1	RW	0x0	EPDisbldMsk Endpoint Disabled Interrupt Mask
0	RW	0x0	XferComplMsk Transfer Completed Interrupt Mask

USBOTG_DAINT
Address: Operational Base + offset (0x0818)
Device All Endpoints interrupt register

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	OutEPInt OUT Endpoint Interrupt Bits One bit per OUT endpoint: Bit 16 for OUT endpoint 0, bit 31 for OUT endpoint 15
15:0	RO	0x0000	InEpInt IN Endpoint Interrupt Bits One bit per IN Endpoint: Bit 0 for IN endpoint 0, bit 15 for endpoint 15

USBOTG_DAINTMSK
Address: Operational Base + offset (0x081c)
Device All Endpoint interrupt mask register

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	OutEpMsk OUT EP Interrupt Mask Bits One per OUT Endpoint: Bit 16 for OUT EP 0, bit 31 for OUT EP 15
15:0	RW	0x0000	InEpMsk IN EP Interrupt Mask Bits One bit per IN Endpoint: Bit 0 for IN EP 0, bit 15 for IN EP 15

USBOTG_DTKNQR1
Address: Operational Base + offset (0x0820)
Device IN token sequence learning queue read register1

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Bit	Attr	Reset Value	Description
31:8	RO	0x000000	EPTkn Endpoint Token Four bits per token represent the endpoint number of the token: Bits [31:28]: Endpoint number of Token 5 Bits [27:24]: Endpoint number of Token 4 ..... Bits [15:12]: Endpoint number of Token 1 Bits [11:8]: Endpoint number of Token 0
7	RO	0x0	WrapBit Wrap Bit This bit is set when the write pointer wraps. It is cleared when the learning queue is cleared.
6:5	RO	0x0	reserved
4:0	RO	0x00	INTknWPtr IN Token Queue Write Pointer

USBOTG_DTKNQR2
Address: Operational Base + offset (0x0824)
Device IN token sequence learning queue read register2

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	EPTkn Endpoint Token Four bits per token represent the endpoint number of the token: Bits [31:28]: Endpoint number of Token 13 Bits [27:24]: Endpoint number of Token 12 ..... Bits [7:4]: Endpoint number of Token 7 Bits [3:0]: Endpoint number of Token 6

USBOTG_DVBUSDIS
Address: Operational Base + offset (0x0828)
Device VBUS discharge time register

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0b8f	DVBUSDis Device VBUS Discharge Time Specifies the VBUS discharge time after VBUS pulsing during SRP. This value equals: VBUS discharge time in PHY clocks / 1,024.The value you use depends whether the PHY is operating at 30 MHz (16-bit data width) or 60 MHz (8-bit data width). Depending on your VBUS load, this value can need adjustment.

USBOTG_DVBUSPULSE
Address: Operational Base + offset (0x082c)
Device VBUS Pulsing Timer Register

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Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0x000	DVBUSPulse Device VBUS Pulsing Time Specifies the VBUS pulsing time during SRP. This value equals: VBUS pulsing time in PHY clocks / 1,024.The value you use depends whether the PHY is operating at 30 MHz (16-bit data width) or 60 MHz (8-bit data width).

USBOTG_DTHRCTL
Address: Operational Base + offset (0x0830)
Device Threshold Control Register

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27	RW	0x1	ArbPrkEn Arbiter Parking Enable This bit controls internal DMA arbiter parking for IN endpoints. When threshold is enabled and this bit is set to one, then the arbiter parks on the IN endpoint for which there is a token received on the USB. This is done to avoid getting into under-run conditions. By default the parking is enabled.
26	RO	0x0	reserved
25:17	RW	0x008	RxThrLen Receive Threshold Length This field specifies Receive threshold size in DWORDS. This field also specifies the amount of data received on the USB before the core can start transmitting on the AHB. The threshold length has to be at least eight DWORDS. The recommended value for ThrLen is to be the same as the programmed AHB Burst Length (GAHBCFG.HBstLen).
16	RW	0x0	RxThrEn Receive Threshold Enable When this bit is set, the core enables threshold in the receive direction.
15:13	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
12:11	RW	0x0	AHBThrRatio AHB Threshold Ratio These bits define the ratio between the AHB threshold and the MAC threshold for the transmit path only. The AHB threshold always remains less than or equal to the USB threshold, because this does not increase overhead. Both the AHB and the MAC threshold must be DWORD-aligned. The application needs to program TxThrLen and the AHBThrRatio to make the AHB Threshold value DWORD aligned. If the AHB threshold value is not DWORD aligned, the core might not behave correctly. When programming the TxThrLen and AHBThrRatio, the application must ensure that the minimum AHB threshold value does not go below 8 DWORDS to meet the USB turnaround time requirements. 2'b00: AHB threshold = MAC threshold 2'b01: AHB threshold = MAC threshold / 2 2'b10: AHB threshold = MAC threshold / 4 2'b11: AHB threshold = MAC threshold / 8
10:2	RW	0x008	TxThrLen Transmit Threshold Length This field specifies Transmit threshold size in DWORDS. This field also forms the MAC threshold and specifies the amount of data, in bytes, to be in the corresponding endpoint transmit FIFO before the core can start transmit on the USB. When the value of AHBThrRatio is 2'h00, the threshold length must be at least 8 DWORDS. If the AHBThrRatio is nonzero, the application must ensure that the AHB threshold value does not go below the recommended 8 DWORDs. This field controls both isochronous and non-isochronous IN endpoint thresholds. The recommended value for ThrLen is to be the same as the programmed AHB Burst Length (GAHBCFG.HBstLen).
1	RW	0x0	ISOThrEn ISO IN Endpoints Threshold Enable When this bit is set, the core enables threshold for isochronous IN endpoints.
0	RW	0x0	NonISOThrEn Non-ISO IN Endpoints Threshold Enable When this bit is set, the core enables threshold for Non Isochronous IN endpoints.

USBOTG_DIEPEMPMSK
Address: Operational Base + offset (0x0834)
Device IN endpoint FIFO empty interrupt mask register

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Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0000	InEpTxfEmpMsk IN EP Tx FIFO Empty Interrupt Mask Bits These bits act as mask bits for DIEPINTn. TxFEmp interrupt One bit per IN Endpoint: Bit 0 for IN endpoint 0 ... Bit 15 for endpoint 15

USBOTG_DEACHINT
Address: Operational Base + offset (0x0838)
Device each endpoint interrupt register

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	EchOutEPInt OUT Endpoint Interrupt Bits One bit per OUT endpoint: Bit 16 for OUT endpoint 0 ... Bit 31 for OUT endpoint 15
15:0	RO	0x0000	EchInEpInt IN Endpoint Interrupt Bits One bit per IN Endpoint: Bit 0 for IN endpoint 0 ... Bit 15 for endpoint 15

USBOTG_DEACHINTMSK
Address: Operational Base + offset (0x083c)
Device each endpoint interrupt register mask

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	EchOutEpMsk OUT EP Interrupt Mask Bits One per OUT Endpoint: Bit 16 for IN endpoint 0 ... Bit 31 for endpoint 15
15:0	RW	0x0000	EchInEpMsk IN EP Interrupt Mask Bits One bit per IN Endpoint: Bit 0 for IN endpoint 0 ... Bit 15 for endpoint 15

USBOTG_DIEPEACHMSKn
Address: Operational Base + offset (0x0840)

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Device each IN endpoint -n interrupt Register

Bit	Attr	Reset Value	Description
31:14	RO	0x0	reserved
13	RW	0x0	NAKMsk NAK interrupt Mask
12:10	RO	0x0	reserved
9	RW	0x0	BNAInIntrMsk BNA interrupt Mask
8	RW	0x0	TxfifoUndrnMsk Fifo Under run Mask
7	RO	0x0	reserved
6	RW	0x0	INEPNakEffMsk IN Endpoint NAK Effective Mask
5	RW	0x0	INTknEPMisMsk IN Token received with EP Mismatch Mask
4	RW	0x0	INTknTXFEmpMsk IN Token Received When TxFIFO Empty Mask
3	RW	0x0	TimeOUTMsk Timeout Condition Mask(Non-isochronous endpoints)
2	RW	0x0	AHBErrMsk AHB Error Mask
1	RW	0x0	EPDisbldMsk Endpoint Disabled Interrupt Mask
0	RW	0x0	XferComplMsk Transfer Completed Interrupt Mask

USBOTG_DOEPEACHMSKn

Address: Operational Base + offset (0x0880)

Device each out endpoint-n interrupt register

Bit	Attr	Reset Value	Description
31:15	RO	0x0	reserved
14	RW	0x0	NYETMsk NYET interrupt Mask
13	RW	0x0	NAKMsk NAK interrupt Mask
12	RW	0x0	BbleErrMsk Babble interrupt Mask
11:10	RO	0x0	reserved
9	RW	0x0	BnaOutIntrMsk BNA interrupt Mask
8	RW	0x0	OutPktErrMsk OUT Packet Error Mask
7	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
6	RW	0x0	Back2BackSETup Back-to-Back SETUP Packets Received Mask Applies to control OUT endpoints only.
5	RO	0x0	reserved
4	RW	0x0	OUTTknEPdisMsk OUT Token Received when Endpoint Disabled Mask Applies to control OUT endpoints only.
3	RW	0x0	SetUPMsk SETUP Phase Done Mask Applies to control endpoints only.
2	RW	0x0	AHBErrMsk AHB Error
1	RW	0x0	EPDisbldMsk Endpoint Disabled Interrupt Mask
0	RW	0x0	XferComplMsk Transfer Completed Interrupt Mask

USBOTG_DIEPCTL0
Address: Operational Base + offset (0x0900)
Device control IN endpoint 0 control register

Bit	Attr	Reset Value	Description
31	R/W SC	0x0	EPEna Endpoint Enable When Scatter/Gather DMA mode is enabled, for IN endpoints this bit indicates that the descriptor structure and data buffer with data ready to transmit is setup. When Scatter/Gather DMA mode is disabled-such as in buffer-pointer based DMA mode-this bit indicates that data is ready to be transmitted on the endpoint. The core clears this bit before setting the following interrupts on this endpoint: Endpoint Disabled; Transfer Completed.
30	R/W SC	0x0	EPDis Endpoint Disable The application sets this bit to stop transmitting data on an endpoint, even before the transfer for that endpoint is complete. The application must wait for the Endpoint Disabled interrupt before treating the endpoint as disabled. The core clears this bit before setting the Endpoint Disabled Interrupt. The application must set this bit only if Endpoint Enable is already set for this endpoint.
29:28	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
27	WO	0x0	SNAK Set NAK A write to this bit sets the NAK bit for the endpoint. Using this bit, the application can control the transmission of NAK handshakes on an endpoint. The core can also set this bit for an endpoint after a SETUP packet is received on that endpoint.
26	WO	0x0	CNAK Clear NAK A write to this bit clears the NAK bit for the endpoint.
25:23	RO	0x0	reserved
22	RW	0x0	TxFNum TxFIFO Number For Shared FIFO operation, this value is always set to 0, indicating that control IN endpoint 0 data is always written in the Non-Periodic Transmit FIFO. For Dedicated FIFO operation, this value is set to the FIFO number that is assigned to IN Endpoint 0.
21	R/WSC	0x0	Stall STALL Handshake The application can only set this bit, and the core clears it, when a SETUP token is received for this endpoint. If a NAK bit, Global Non-periodic IN NAK, or Global OUT NAK is set along with this bit, the STALL bit takes priority.
20	RO	0x0	reserved
19:18	RO	0x0	EPType Endpoint Type Hardcoded to 00 for control
17	RO	0x0	NAKSts NAK Status Indicates the following: 1'b0: The core is transmitting non-NAK handshakes based on the FIFO status 1'b1: The core is transmitting NAK handshakes on this endpoint. When this bit is set, either by the application or core, the core stops transmitting data, even if there is data available in the TxFIFO. Irrespective of this bit's setting, the core always responds to SETUP data packets with an ACK handshake.
16	RO	0x0	reserved
15	RO	0x1	USBActEP USB Active Endpoint This bit is always set to 1, indicating that control endpoint 0 is always active in all configurations and interfaces.

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Bit	Attr	Reset Value	Description
14:11	RW	0x0	NextEp Next Endpoint Applies to non-periodic IN endpoints only. Indicates the endpoint number to be fetched after the data for the current endpoint is fetched. The core can access this field, even when the Endpoint Enable (EPEna) bit is not set. This field is not valid in Slave mode. Note: This field is valid only for Shared FIFO operations.
10:2	RO	0x0	reserved
1:0	RW	0x0	MPS Maximum Packet Size Applies to IN and OUT endpoints. The application must program this field with the maximum packet size for the current logical endpoint. 2'b00: 64 bytes 2'b01: 32 bytes 2'b10: 16 bytes 2'b11: 8 bytes

USBOTG_DIEPINTn
Address: Operational Base + offset (0x0908)
Device Endpoint-n Interrupt Register

Bit	Attr	Reset Value	Description
31:15	RO	0x0	reserved
14	W1C	0x0	NYETIntrpt NYET interrupt The core generates this interrupt when a NYET response is transmitted for a non-isochronous OUT endpoint.
13	W1C	0x0	NAKIntrpt NAK interrupt The core generates this interrupt when a NAK is transmitted or received by the device.In case of isochronous IN endpoints the interrupt gets generated when a zero length packet is transmitted due to un-availability of data in the TXFifo.
12	W1C	0x0	BbleErrIntrpt BbleErr (Babble Error) interrupt The core generates this interrupt when babble is received for the endpoint.
11	W1C	0x0	PktDrpSts Packet Dropped Status This bit indicates to the application that an ISOC OUT packet has been dropped. This bit does not have an associated mask bit and does not generate an interrupt. Dependency: This bit is valid in non-Scatter/Gather DMA mode when periodic transfer interrupt feature is selected.

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Bit	Attr	Reset Value	Description
10	RO	0x0	reserved
9	W1C	0x0	BNAIntr BNA (Buffer Not Available) Interrupt The core generates this interrupt when the descriptor accessed is not ready for the Core to process, such as Host busy or DMA done Dependency: This bit is valid only when Scatter/Gather DMA mode is enabled.
8	W1C	0x0	TxfifoUndrn FIFO Underrun Applies to IN endpoints only. The core generates this interrupt when it detects a transmit FIFO under-run condition for this endpoint. Dependency: This interrupt is valid only when both of the following conditions are true: Parameter OTG_EN_DED_TX_FIFO==1; Threshold is enabled; OUT Packet Error(OutPktErr). Applies to OUT endpoints only. This interrupt is asserted when the core detects an overflow or a CRC error for an OUT packet. Dependency: This interrupt is valid only when both of the following conditions are true: Parameter OTG_EN_DED_TX_FIFO==1; Threshold is enabled.
7	W1C	0x0	TxFEmp Transmit FIFO Empty This bit is valid only for IN Endpoints. This interrupt is asserted when the TxFIFO for this endpoint is either half or completely empty. The half or completely empty status is determined by the TxFIFO Empty Level bit in the Core AHB Configuration register (GAHBCFG.NPTxFEmpLvl)).
6	W1C	0x0	INEPNakEff IN Endpoint NAK Effective Applies to periodic IN endpoints only. This bit can be cleared when the application clears the IN endpoint NAK by writing to DIEPCTLn.CNAK. This interrupt indicates that the core has sampled the NAK bit set (either by the application or by the core). The interrupt indicates that the IN endpoint NAK bit set by the application has taken effect in the core. This interrupt does not guarantee that a NAK handshake is sent on the USB. A STALL bit takes priority over a NAK bit. This bit is applicable only when the endpoint is enabled. Back-to-Back SETUP Packets Received (Back2BackSETup) Applies to Control OUT endpoints only. This bit indicates that the core has received more than three back-to-back SETUP packets for this particular endpoint.

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Bit	Attr	Reset Value	Description
5	W1C	0x0	INTknEPMis IN Token Received with EP Mismatch Applies to non-periodic IN endpoints only. Indicates that the data in the top of the non-periodic TxFIFO belongs to an endpoint other than the one for which the IN token was received. This interrupt is asserted on the endpoint for which the IN token was received. Status Phase Received For Control Write (StsPhseRcvd) This interrupt is valid only for Control OUT endpoints and only in Scatter Gather DMA mode. This interrupt is generated only after the core has transferred all the data that the host has sent during the data phase of a control write transfer, to the system memory buffer. The interrupt indicates to the application that the host has switched from data phase to the status phase of a Control Write transfer. The application can use this interrupt to ACK or STALL the Status phase, after it has decoded the data phase. This is applicable only in case of Scatter Gather DMA mode.
4	W1C	0x0	INTknTXFEmp IN Token Received When TxFIFO is Empty Indicates that an IN token was received when the associated TxFIFO periodic/non-periodic) was empty. This interrupt is asserted on the endpoint for which the IN token was received. OUT Token Received When Endpoint Disabled (OUTTknEPdis) Indicates that an OUT token was received when the endpoint was not yet enabled. This interrupt is asserted on the endpoint for which the OUT token was received.
3	W1C	0x0	TimeOUT Timeout Condition In shared TX FIFO mode, applies to non-isochronous IN endpoints only. In dedicated FIFO mode, applies only to Control IN endpoints. In Scatter/Gather DMA mode, the TimeOUT interrupt is not asserted. Indicates that the core has detected a timeout condition on the USB for the last IN token on this endpoint. SETUP Phase Done (SetUp) Applies to control OUT endpoints only. Indicates that the SETUP phase for the control endpoint is complete and no more back-to-back SETUP packets were received for the current control transfer. On this interrupt, the application can decode the received SETUP data packet.
2	W1C	0x0	AHBErr AHB Error Applies to IN and OUT endpoints. This is generated only in Internal DMA mode when there is an AHB error during an AHB read/write. The application can read the corresponding endpoint DMA address register to get the error address.

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Bit	Attr	Reset Value	Description
1	W1C	0x0	EPDisbld Endpoint Disabled Interrupt Applies to IN and OUT endpoints. This bit indicates that the endpoint is disabled per the application's request.
0	W1C	0x0	XferCompl Transfer Completed Interrupt Applies to IN and OUT endpoints. When Scatter/Gather DMA mode is enabled: For IN endpoint this field indicates that the requested data from the descriptor is moved from external system memory to internal FIFO. For OUT endpoint this field indicates that the requested data from the internal FIFO is moved to external system memory. This interrupt is generated only when the corresponding endpoint descriptor is closed, and the IOC bit for the corresponding descriptor is set. When Scatter/Gather DMA mode is disabled, this field indicates that the programmed transfer is complete on the AHB as well as on the USB, for this endpoint.

USBOTG_DIEPTSIZn

Address: Operational Base + offset (0x0910)

Device endpoint n transfer size register

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved

Bit	Attr	Reset Value	Description
30:29	RW	0x0	MC Multi Count Applies to IN endpoints only. For periodic IN endpoints, this field indicates the number of packets that must be transmitted per microframe on the USB. The core uses this field to calculate the data PID for isochronous IN endpoints. 2'b01: 1 packet 2'b10: 2 packets 2'b11: 3 packets For non-periodic IN endpoints, this field is valid only in Internal DMA mode. It specifies the number of packets the core must fetch for an IN endpoint before it switches to the endpoint pointed to by the Next Endpoint field of the Device Endpoint-n Control register (DIEPCTLn.NextEp). Received Data PID (RxDPID) Applies to isochronous OUT endpoints only. This is the data PID received in the last packet for this endpoint. 2'b00: DATA0 2'b01: DATA2 2'b10: DATA1 2'b11: MDATA SETUP Packet Count (SUPCnt).Applies to control OUT Endpoints only.This field specifies the number of back-to-back SETUP data packets the endpoint can receive. 2'b01: 1 packet 2'b10: 2 packets 2'b11: 3 packets
28:19	RW	0x000	PktCnt Packet Count Indicates the total number of USB packets that constitute the Transfer Size amount of data for this endpoint. The power-on value is specified for Width of Packet Counters during configuration (parameter OTG_PACKET_COUNT_WIDTH). IN Endpoints: This field is decremented every time a packet (maximum size or short packet) is read from the TxFIFO. OUT Endpoints: This field is decremented every time a packet (maximum size or short packet) is written to the RxFIFO.

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Bit	Attr	Reset Value	Description
18:0	RW	0x00000	XferSize Transfer Size This field contains the transfer size in bytes for the current endpoint. The power-on value is specified for Width of Transfer Size Counters during configuration (parameter OTG_TRANS_COUNT_WIDTH). The core only interrupts the application after it has exhausted the transfer size amount of data. The transfer size can be set to the maximum packet size of the endpoint, to be interrupted at the end of each packet. IN Endpoints: The core decrements this field every time a packet from the external memory is written to the TxFIFO.OUT Endpoints: The core decrements this field every time a packet is read from the RxFIFO and written to the external memory.

USBOTG_DIEPDMAn
Address: Operational Base + offset (0x0914)
Device endpoint-n DMA Address Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	DMAAddr DMA Address Holds the start address of the external memory for storing or fetching endpoint data. Note: For control endpoints, this field stores control OUT data packets as well as SETUP transaction data packets. When more than three SETUP packets are received back-to-back, the SETUP data packet in the memory is overwritten. This register is incremented on every AHB transaction. The application can give only a DWORD-aligned address. When Scatter/Gather DMA mode is not enabled, the application programs the start address value in this field. When Scatter/Gather DMA mode is enabled, this field indicates the base pointer for the descriptor list.

USBOTG_DTXFSTSn
Address: Operational Base + offset (0x0918)
Device IN endpoint transmit FIFO status register

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	INEPTxFSpcAvail IN Endpoint TxFIFO Space Avail Indicates the amount of free space available in the Endpoint TxFIFO.Values in terms of 32-bit words. 16'h0: Endpoint TxFIFO is full 16'h1: 1 word available 16'h2: 2 words available 16'hn: n words available (where 0 . n . 32,768) 16'h8000: 32,768 words available Others: Reserved

USBOTG_DIEPDMABn
Address: Operational Base + offset (0x091c)
Device endpoint-n DMA buffer address register

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	DMABufferAddr DMA Buffer Address Holds the current buffer address. This register is updated as and when the data transfer for the corresponding end point is in progress. This register is present only in Scatter/Gather DMA mode. Otherwise this field is reserved.

USBOTG_DIEPCTLn
Address: Operational Base + offset (0x0920)
Device endpoint-n control register

Bit	Attr	Reset Value	Description
31	R/W SC	0x0	EPEna Endpoint Enable Applies to IN and OUT endpoints. When Scatter/Gather DMA mode is enabled, For IN endpoints this bit indicates that the descriptor structure and data buffer with data ready to transmit is setup. For OUT endpoint it indicates that the descriptor structure and data buffer to receive data is setup. When Scatter/Gather DMA mode is enabled-such as for buffer-pointer based DMA mode: For IN endpoints, this bit indicates that data is ready to be transmitted on the endpoint ; For OUT endpoints, this bit indicates that the application has allocated the memory to start receiving data from the USB. The core clears this bit before setting any of the following interrupts on this endpoint: SETUP Phase Done, Endpoint Disabled, Transfer Completed. Note: For control endpoints in DMA mode, this bit must be set to be able to transfer SETUP data packets in memory.

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Bit	Attr	Reset Value	Description
30	R/WSC	0x0	EPDis Endpoint Disable Applies to IN and OUT endpoints. The application sets this bit to stop transmitting/receiving data on an endpoint, even before the transfer for that endpoint is complete. The application must wait for the Endpoint Disabled interrupt before treating the endpoint as disabled. The core clears this bit before setting the Endpoint Disabled interrupt. The application must set this bit only if Endpoint Enable is already set for this endpoint.
29	WO	0x0	SetD1PID Set DATA1 PID Applies to interrupt/bulk IN and OUT endpoints only. Writing to this field sets the Endpoint Data PID (DPID) field in this register to DATA1.This field is applicable both for Scatter/Gather DMA mode and non-Scatter/Gather DMA mode. Set Odd (micro) frame (SetOddFr). Applies to isochronous IN and OUT endpoints only. Writing to this field sets the Even/Odd (micro) frame (EO_FrNum) field to odd (micro)frame. This field is not applicable for Scatter/Gather DMA mode.
28	WO	0x0	SetD0PID Set DATA0 PID Applies to interrupt/bulk IN and OUT endpoints only. Writing to this field sets the Endpoint Data PID (DPID) field in this register to DATA0.This field is applicable both for Scatter/Gather DMA mode and non-Scatter/Gather DMA mode. In non-Scatter/Gather DMA mode: Set Even (micro) frame (SetEvenFr) Applies to isochronous IN and OUT endpoints only. Writing to this field sets the Even/Odd (micro) frame (EO_FrNum) field to even (micro) frame. When Scatter/Gather DMA mode is enabled, this field is reserved. The frame number in which to send data is in the transmit descriptor structure. The frame in which to receive data is updated in received descriptor structure.
27	WO	0x0	SNAK Set NAK Applies to IN and OUT endpoints. A write to this bit sets the NAK bit for the endpoint. Using this bit, the application can control the transmission of NAK handshakes on an endpoint. The core can also set this bit for OUT endpoints on a Transfer Completed interrupt, or after a SETUP is received on the endpoint.
26	WO	0x0	CNAK Clear NAK Applies to IN and OUT endpoints. A write to this bit clears the NAK bit for the endpoint.

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Bit	Attr	Reset Value	Description
25:22	RW	0x0	TxFNum TxFIFO Number Shared FIFO Operation: non-periodic endpoints must set this bit to zero. Periodic endpoints must map this to the corresponding Periodic TxFIFO number. 4'h0: Non-Periodic TxFIFO; Others: Specified Periodic TxFIFO number. Note: An interrupt IN endpoint can be configured as a non-periodic endpoint for applications such as mass storage. The core treats an IN endpoint as a non-periodic endpoint if the TxFNum field is set to 0. Otherwise, a separate periodic FIFO must be allocated for an interrupt IN endpoint using coreConsultant, and the number of this FIFO must be programmed into the TxFNum field. Configuring an interrupt IN endpoint as a non-periodic endpoint saves the extra periodic FIFO area. Dedicated FIFO Operation: these bits specify the FIFO number associated with this endpoint. Each active IN endpoint must be programmed to a separate FIFO number. This field is valid only for IN endpoints.
21	RW	0x0	Stall STALL Handshake Applies to non-control, non-isochronous IN and OUT endpoints only. The application sets this bit to stall all tokens from the USB host to this endpoint. If a NAK bit, Global Non-periodic IN NAK, or Global OUT NAK is set along with this bit, the STALL bit takes priority. Only the application can clear this bit, never the core. Applies to control endpoints only. The application can only set this bit, and the core clears it, when a SETUP token is received for this endpoint. If a NAK bit, Global Non-periodic IN NAK, or Global OUT NAK is set along with this bit, the STALL bit takes priority. Irrespective of this bit's setting, the core always responds to SETUP data packets with an ACK handshake.
20	RW	0x0	Snp Snoop Mode Applies to OUT endpoints only. This bit configures the endpoint to Snoop mode. In Snoop mode, the core does not check the correctness of OUT packets before transferring them to application memory.
19:18	RW	0x0	EPType Endpoint Type Applies to IN and OUT endpoints. This is the transfer type supported by this logical endpoint. 2'b00: Control 2'b01: Isochronous 2'b10: Bulk 2'b11: Interrupt

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Bit	Attr	Reset Value	Description
17	RO	0x0	NAKSts NAK Status Applies to IN and OUT endpoints. Indicates the following: 1'b0: The core is transmitting non-NAK handshakes based on the FIFO status. 1'b1: The core is transmitting NAK handshakes on this endpoint. When either the application or the core sets this bit: The core stops receiving any data on an OUT endpoint, even if there is space in the RxFIFO to accommodate the incoming packet. For non-isochronous IN endpoints: The core stops transmitting any data on an IN endpoint, even if there data is available in the TxFIFO. For isochronous IN endpoints: The core sends out a zero-length data packet, even if there data is available in the TxFIFO. Irrespective of this bit's setting, the core always responds to SETUP data packets with an ACK handshake.
16	RO	0x0	DPID Endpoint Data PID Applies to interrupt/bulk IN and OUT endpoints only. Contains the PID of the packet to be received or transmitted on this endpoint. The application must program the PID of the first packet to be received or transmitted on this endpoint, after the endpoint is activated. The applications use the SetD1PID and SetD0PID fields of this register to program either DATA0 or DATA1 PID. 1'b0: DATA0 1'b1: DATA1 This field is applicable both for Scatter/Gather DMA mode and non-Scatter/Gather DMA mode.Even/Odd (Micro)Frame (EO_FrNum) In non-Scatter/Gather DMA mode: Applies to isochronous IN and OUT endpoints only.Indicates the (micro) frame number in which the core transmits/receives isochronous data for this endpoint. The application must program the even/odd (micro) frame number in which it intends to transmit/receive isochronous data for this endpoint using the SetEvnFr and SetOddFr fields in this register. 1'b0: Even (micro)frame 1'b1: Odd (micro)frame When Scatter/Gather DMA mode is enabled, this field is reserved. The frame number in which to send data is provided in the transmit descriptor structure. The frame in which data is received is updated in receive descriptor structure.

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Bit	Attr	Reset Value	Description
15	R/WSC	0x0	USBActEP USB Active Endpoint Applies to IN and OUT endpoints. Indicates whether this endpoint is active in the current configuration and interface. The core clears this bit for all endpoints (other than EP 0) after detecting a USB reset. After receiving the SetConfiguration and SetInterface commands, the application must program endpoint registers accordingly and set this bit.
14:11	RW	0x0	NextEp Next Endpoint Applies to non-periodic IN endpoints only. Indicates the endpoint number to be fetched after the data for the current endpoint is fetched. The core can access this field, even when the Endpoint Enable (EPEna) bit is low. This field is not valid in Slave mode operation. Note: This field is valid only for Shared FIFO operations.
10:0	RW	0x000	MPS Maximum Packet Size Applies to IN and OUT endpoints. The application must program this field with the maximum packet size for the current logical endpoint. This value is in bytes.

USBOTG_DOEPCTL0
Address: Operational Base + offset (0x0b00)
Device control OUT endpoint 0 control register

Bit	Attr	Reset Value	Description
31	R/WSC	0x0	EPEna Endpoint Enable When Scatter/Gather DMA mode is enabled, for OUT endpoints this bit indicates that the descriptor structure and data buffer to receive data is setup. When Scatter/Gather DMA mode is disabled (such as for buffer-pointer based DMA mode)-this bit indicates that the application has allocated the memory to start receiving data from the USB. The core clears this bit before setting any of the following interrupts on this endpoint: SETUP Phase Done, Endpoint Disabled, Transfer Completed. Note: In DMA mode, this bit must be set for the core to transfer SETUP data packets into memory.
30	WO	0x0	EPDis Endpoint Disable The application cannot disable control OUT endpoint 0.
29:28	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
27	WO	0x0	SNAK Set NAK A write to this bit sets the NAK bit for the endpoint. Using this bit, the application can control the transmission of NAK handshakes on an endpoint. The core can also set bit on a Transfer Completed interrupt, or after a SETUP is received on the endpoint.
26	WO	0x0	CNAK Clear NAK A write to this bit clears the NAK bit for the endpoint.
25:22	RO	0x0	reserved
21	R/WSC	0x0	Stall STALL Handshake The application can only set this bit, and the core clears it, when a SETUP token is received for this endpoint. If a NAK bit or Global OUT NAK is set along with this bit, the STALL bit takes priority. Irrespective of this bit's setting, the core always responds to SETUP data packets with an ACK handshake.
20	RW	0x0	Snp Snoop Mode This bit configures the endpoint to Snoop mode. In Snoop mode, the core does not check the correctness of OUT packets before transferring them to application memory.
19:18	RO	0x0	EPType Endpoint Type Hardcoded to 2'b00 for control.
17	RO	0x0	NAKSts NAK Status Indicates the following: 1'b0: The core is transmitting non-NAK handshakes based on the FIFO status. 1'b1: The core is transmitting NAK handshakes on this endpoint. When either the application or the core sets this bit, the core stops receiving data, even if there is space in the RxFIFO to accommodate the incoming packet. Irrespective of this bit setting, the core always responds to SETUP data packets with an ACK handshake.
16	RO	0x0	reserved
15	RO	0x0	USBActEP USB Active Endpoint This bit is always set to 1, indicating that a control endpoint 0 is always active in all configurations and interfaces.
14:2	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
1:0	RO	0x0	MPS Maximum Packet Size The maximum packet size for control OUT endpoint 0 is the same as what is programmed in control IN Endpoint 0. 2'b00: 64 bytes 2'b01: 32 bytes 2'b10: 16 bytes 2'b11: 8 bytes

USBOTG_DOEPINTn
Address: Operational Base + offset (0x0b08)
Device endpoint-n control register

Bit	Attr	Reset Value	Description
31:15	RO	0x0	reserved
14	W1C	0x0	NYETIntrpt NYET interrupt The core generates this interrupt when a NYET response is transmitted for a non-isochronous OUT endpoint.
13	W1C	0x0	NAKIntrpt NAK interrupt The core generates this interrupt when a NAK is transmitted or received by the device.In case of isochronous IN endpoints the interrupt gets generated when a zero length packet is transmitted due to un-availability of data in the TXFifo.
12	W1C	0x0	BbleErrIntrpt BbleErr (Babble Error) interrupt The core generates this interrupt when babble is received for the endpoint.
11	W1C	0x0	PktDrpSts Packet Dropped Status This bit indicates to the application that an ISOC OUT packet has been dropped. This bit does not have an associated mask bit and does not generate an interrupt. Dependency: This bit is valid in non-Scatter/Gather DMA mode when periodic transfer interrupt feature is selected.
10	RO	0x0	reserved
9	W1C	0x0	BNAIntr BNA (Buffer Not Available) Interrupt The core generates this interrupt when the descriptor accessed is not ready for the Core to process, such as Host busy or DMA done. Dependency: This bit is valid only when Scatter/Gather DMA mode is enabled.

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Bit	Attr	Reset Value	Description
8	W1C	0x0	TxfifoUndrn FIFO Underrun Applies to IN endpoints only. The core generates this interrupt when it detects a transmit FIFO under-run condition for this endpoint. Dependency: This interrupt is valid only when both of the following conditions are true: Parameter OTG_EN_DED_TX_FIFO==1, Threshold is enabled, OUT Packet Error (OutPktErr). Applies to OUT endpoints only. This interrupt is asserted when the core detects an overflow or a CRC error for an OUT packet. Dependency: This interrupt is valid only when both of the following conditions are true: Parameter OTG_EN_DED_TX_FIFO==1, Threshold is enabled.
7	W1C	0x0	TxFEmp Transmit FIFO Empty This bit is valid only for IN Endpoints. This interrupt is asserted when the TxFIFO for this endpoint is either half or completely empty. The half or completely empty status is determined by the TxFIFO Empty Level bit in the Core AHB Configuration register (GAHBCFG.NPTxFEmpLvl)).
6	W1C	0x0	INEPNakEff IN Endpoint NAK Effective Applies to periodic IN endpoints only. This bit can be cleared when the application clears the IN endpoint NAK by writing to DIEPCTLn.CNAK. This interrupt indicates that the core has sampled the NAK bit set (either by the application or by the core). The interrupt indicates that the IN endpoint NAK bit set by the application has taken effect in the core. This interrupt does not guarantee that a NAK handshake is sent on the USB. A STALL bit takes priority over a NAK bit. This bit is applicable only when the endpoint is enabled. Back-to-Back SETUP Packets Received (Back2BackSETup) Applies to Control OUT endpoints only. This bit indicates that the core has received more than three back-to-back SETUP packets for this particular endpoint.
5	W1C	0x0	INTknEPMis IN Token Received with EP Mismatch Applies to non-periodic IN endpoints only. Indicates that the data in the top of the non-periodic TxFIFO belongs to an endpoint other than the one for which the IN token was received. This interrupt is asserted on the endpoint for which the IN token was received. Status Phase Received For Control Write (StsPhseRcvd) This interrupt is valid only for Control OUT endpoints and only in Scatter Gather DMA mode.

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Bit	Attr	Reset Value	Description
4	W1C	0x0	INTknTXFEmp IN Token Received When TxFIFO is Empty Indicates that an IN token was received when the associated TxFIFO periodic/non-periodic) was empty. This interrupt is asserted on the endpoint for which the IN token was received. OUT Token Received When Endpoint Disabled (OUTTknEPdis) Indicates that an OUT token was received when the endpoint was not yet enabled. This interrupt is asserted on the endpoint for which the OUT token was received.
3	W1C	0x0	TimeOUT Timeout Condition In shared TX FIFO mode, applies to non-isochronous IN endpoints only. In dedicated FIFO mode, applies only to Control IN endpoints. In Scatter/Gather DMA mode, the TimeOUT interrupt is not asserted.Indicates that the core has detected a timeout condition on the USB for the last IN token on this endpoint. SETUP Phase Done (SetUp). Applies to control OUT endpoints only. Indicates that the SETUP phase for the control endpoint is complete and no more back-to-back SETUP packets were received for the current control transfer. On this interrupt, the application can decode the received SETUP data packet.
2	W1C	0x0	AHBErr AHB Error Applies to IN and OUT endpoints. This is generated only in Internal DMA mode when there is an AHB error during an AHB read/write. The application can read the corresponding endpoint DMA address register to get the error address.
1	W1C	0x0	EPDisbld Endpoint Disabled Interrupt Applies to IN and OUT endpoints. This bit indicates that the endpoint is disabled per the application's request.
0	W1C	0x0	XferCompl Transfer Completed Interrupt Applies to IN and OUT endpoints. When Scatter/Gather DMA mode is enabled. For IN endpoint this field indicates that the requested data from the descriptor is moved from external system memory to internal FIFO. For OUT endpoint this field indicates that the requested data from the internal FIFO is moved to external system memory. This interrupt is generated only when the corresponding endpoint descriptor is closed, and the IOC bit for the corresponding descriptor is set. When Scatter/Gather DMA mode is disabled, this field indicates that the programmed transfer is complete on the AHB as well as on the USB, for this endpoint.

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USBOTG_DOEPTSIZn

Address: Operational Base + offset (0x0b10)

Device endpoint n transfer size register

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:29	RW	0x0	MC Multi Count Applies to IN endpoints only. For periodic IN endpoints, this field indicates the number of packets that must be transmitted per microframe on the USB. The core uses this field to calculate the data PID for isochronous IN endpoints. 2'b01: 1 packet 2'b10: 2 packets 2'b11: 3 packets For non-periodic IN endpoints, this field is valid only in Internal DMA mode. It specifies the number of packets the core must fetch for an IN endpoint before it switches to the endpoint pointed to by the Next Endpoint field of the Device Endpoint-n Control register (DIEPCTLn.NextEp). Received Data PID (RxDPID) Applies to isochronous OUT endpoints only. This is the data PID received in the last packet for this endpoint. 2'b00: DATA0 2'b01: DATA2 2'b10: DATA1 2'b11: MDATA SETUP Packet Count (SUPCnt).Applies to control OUT Endpoints only. This field specifies the number of back-to-back SETUP data packets the endpoint can receive. 2'b01: 1 packet 2'b10: 2 packets 2'b11: 3 packets
28:19	RW	0x000	PktCnt Packet Count Indicates the total number of USB packets that constitute the Transfer Size amount of data for this endpoint. The power-on value is specified for Width of Packet Counters during coreConsultant configuration (parameter OTG_PACKET_COUNT_WIDTH). IN Endpoints: This field is decremented every time a packet (maximum size or short packet) is read from the TxFIFO. OUT Endpoints: This field is decremented every time a packet (maximum size or short packet) is written to the RxFIFO.

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Bit	Attr	Reset Value	Description
18:0	RW	0x00000	XferSize Transfer Size This field contains the transfer size in bytes for the current endpoint. The power-on value is specified for Width of Transfer Size Counters during coreConsultant configuration (parameter OTG_TRANS_COUNT_WIDTH). The core only interrupts the application after it has exhausted the transfer size amount of data. The transfer size can be set to the maximum packet size of the endpoint, to be interrupted at the end of each packet. IN Endpoints: The core decrements this field every time a packet from the external memory is written to the TxFIFO. OUT Endpoints: The core decrements this field every time a packet is read from the RxFIFO and written to the external memory.

USBOTG_DOEPDMAn
Address: Operational Base + offset (0x0b14)
Device Endpoint-n DMA Address Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	DMAAddr DMA Address Holds the start address of the external memory for storing or fetching endpoint data. Note: For control endpoints, this field stores control OUT data packets as well as SETUP transaction data packets. When more than three SETUP packets are received back-to-back, the SETUP data packet in the memory is overwritten. This register is incremented on every AHB transaction. The application can give only a DWORD-aligned address. When Scatter/Gather DMA mode is not enabled, the application programs the start address value in this field. When Scatter/Gather DMA mode is enabled, this field indicates the base pointer for the descriptor list.

USBOTG_DOEPDMABn
Address: Operational Base + offset (0x0b1c)
Device endpoint-n DMA buffer address register

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	DMABufferAddr DMA Buffer Address Holds the current buffer address. This register is updated as and when the data transfer for the corresponding end point is in progress. This register is present only in Scatter/Gather DMA mode. Otherwise this field is reserved.

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USBOTG_DOEPCTLn
Address: Operational Base + offset (0x0b20)
Device endpoint-n control register

Bit	Attr	Reset Value	Description
31	R/WSC	0x0	EPEna Endpoint Enable Applies to IN and OUT endpoints. When Scatter/Gather DMA mode is enabled, For IN endpoints this bit indicates that the descriptor structure and data buffer with data ready to transmit is setup. For OUT endpoint it indicates that the descriptor structure and data buffer to receive data is setup. When Scatter/Gather DMA mode is enabled-such as for buffer-pointer based DMA mode: For IN endpoints, this bit indicates that data is ready to be transmitted on the endpoint; For OUT endpoints, this bit indicates that the application has allocated the memory to start receiving data from the USB. The core clears this bit before setting any of the following interrupts on this endpoint: SETUP Phase Done, Endpoint Disabled, Transfer Completed. Note: For control endpoints in DMA mode, this bit must be set to be able to transfer SETUP data packets in memory.
30	R/WSC	0x0	EPDis Endpoint Disable Applies to IN and OUT endpoints. The application sets this bit to stop transmitting/receiving data on an endpoint, even before the transfer for that endpoint is complete. The application must wait for the Endpoint Disabled interrupt before treating the endpoint as disabled. The core clears this bit before setting the Endpoint Disabled interrupt. The application must set this bit only if Endpoint Enable is already set for this endpoint.
29	RO	0x0	SetD1PID Field0001 Abstract Applies to interrupt/bulk IN and OUT endpoints only. Writing to this field sets the Endpoint Data PID (DPID) field in this register to DATA1.This field is applicable both for Scatter/Gather DMA mode and non-Scatter/Gather DMA mode. Set Odd (micro) frame (SetOddFr). Applies to isochronous IN and OUT endpoints only. Writing to this field sets the Even/Odd (micro) frame (EO_FrNum) field to odd (micro) frame. This field is not applicable for Scatter/Gather DMA mode.

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Bit	Attr	Reset Value	Description
28	WO	0x0	SetD0PID Set DATA0 PID Applies to interrupt/bulk IN and OUT endpoints only.Writing to this field sets the Endpoint Data PID (DPID) field in this register to DATA0.This field is applicable both for Scatter/Gather DMA mode and non-Scatter/Gather DMA mode. In non-Scatter/Gather DMA mode: Set Even (micro) frame (SetEvenFr) Applies to isochronous IN and OUT endpoints only. Writing to this field sets the Even/Odd (micro) frame (EO_FrNum) field to even (micro) frame. When Scatter/Gather DMA mode is enabled, this field is reserved. The frame number in which to send data is in the transmit descriptor structure. The frame in which to receive data is updated in received descriptor structure.
27	WO	0x0	SNAK Set NAK Applies to IN and OUT endpoints. A write to this bit sets the NAK bit for the endpoint. Using this bit, the application can control the transmission of NAK handshakes on an endpoint. The core can also set this bit for OUT endpoints on a Transfer Completed interrupt, or after a SETUP is received on the endpoint.
26	WO	0x0	CNAK Clear NAK Applies to IN and OUT endpoints. A write to this bit clears the NAK bit for the endpoint.
25:22	RW	0x0	TxFNum TxFIFO Number Shared FIFO Operation: non-periodic endpoints must set this bit to zero. Periodic endpoints must map this to the corresponding Periodic TxFIFO number. 4'h0: Non-Periodic TxFIFO; Others: Specified Periodic TxFIFO number. Note: An interrupt IN endpoint can be configured as a non-periodic endpoint for applications such as mass storage. The core treats an IN endpoint as a non-periodic endpoint if the TxFNum field is set to 0. Otherwise, a separate periodic FIFO must be allocated for an interrupt IN endpoint using coreConsultant, and the number of this FIFO must be programmed into the TxFNum field. Configuring an interrupt IN endpoint as a non-periodic endpoint saves the extra periodic FIFO area. Dedicated FIFO Operation: these bits specify the FIFO number associated with this endpoint. Each active IN endpoint must be programmed to a separate FIFO number. This field is valid only for IN endpoints.

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Bit	Attr	Reset Value	Description
21	RW	0x0	Stall STALL Handshake Applies to non-control, non-isochronous IN and OUT endpoints only. The application sets this bit to stall all tokens from the USB host to this endpoint. If a NAK bit, Global Non-periodic IN NAK, or Global OUT NAK is set along with this bit, the STALL bit takes priority. Only the application can clear this bit, never the core. Applies to control endpoints only. The application can only set this bit, and the core clears it, when a SETUP token is received for this endpoint. If a NAK bit, Global Non-periodic IN NAK, or Global OUT NAK is set along with this bit, the STALL bit takes priority. Irrespective of this bit's setting, the core always responds to SETUP data packets with an ACK handshake.
20	RW	0x0	Snp Snoop Mode Applies to OUT endpoints only. This bit configures the endpoint to Snoop mode. In Snoop mode, the core does not check the correctness of OUT packets before transferring them to application memory.
19:18	RW	0x0	EPType Endpoint Type Applies to IN and OUT endpoints. This is the transfer type supported by this logical endpoint. 2'b00: Control 2'b01: Isochronous 2'b10: Bulk 2'b11: Interrupt
17	RO	0x0	NAKSts NAK Status Applies to IN and OUT endpoints. Indicates the following: 1'b0: The core is transmitting non-NAK handshakes based on the FIFO status. 1'b1: The core is transmitting NAK handshakes on this endpoint. When either the application or the core sets this bit: The core stops receiving any data on an OUT endpoint, even if there is space in the RxFIFO to accommodate the incoming packet.

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Bit	Attr	Reset Value	Description
16	RO	0x0	DPID Endpoint Data PID Applies to interrupt/bulk IN and OUT endpoints only. Contains the PID of the packet to be received or transmitted on this endpoint. The application must program the PID of the first packet to be received or transmitted on this endpoint, after the endpoint is activated. The applications use the SetD1PID and SetD0PID fields of this register to program either DATA0 or DATA1 PID. 1'b0: DATA0 1'b1: DATA1 This field is applicable both for Scatter/Gather DMA mode and non-Scatter/Gather DMA mode. Even/Odd (Micro) Frame (EO_FrNum). In non-Scatter/Gather DMA mode: Applies to isochronous IN and OUT endpoints only. Indicates the (micro)frame number in which the core transmits/receives isochronous data for this endpoint. The application must program the even/odd (micro) frame number in which it intends to transmit/receive isochronous data for this endpoint using the SetEvnFr and SetOddFr fields in this register. 1'b0: Even (micro)frame 1'b1: Odd (micro)frame When Scatter/Gather DMA mode is enabled, this field is reserved. The frame number in which to send data is provided in the transmit descriptor structure. The frame in which data is received is updated in receive descriptor structure.
15	R/WSC	0x0	USBActEP USB Active Endpoint Applies to IN and OUT endpoints. Indicates whether this endpoint is active in the current configuration and interface. The core clears this bit for all endpoints (other than EP 0) after detecting a USB reset. After receiving the SetConfiguration and SetInterface commands, the application must program endpoint registers accordingly and set this bit.
14:11	RW	0x0	NextEp Next Endpoint Applies to non-periodic IN endpoints only. Indicates the endpoint number to be fetched after the data for the current endpoint is fetched. The core can access this field, even when the Endpoint Enable (EPEna) bit is low. This field is not valid in Slave mode operation. Note: This field is valid only for Shared FIFO operations.

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Bit	Attr	Reset Value	Description
10:0	RW	0x000	MPS Maximum Packet Size Applies to IN and OUT endpoints. The application must program this field with the maximum packet size for the current logical endpoint. This value is in bytes.

USBOTG_PCGCR
Address: Operational Base + offset (0x0b24)
Power and clock gating control register

Bit	Attr	Reset Value	Description
31:14	RW	0x0802e	RestoreValue Restore Value (Applicable only when Hibernation is enabled (OTG_EN_PWROPT=2). Defines port clock select for different speeds. [31] if_dev_mode - 1: Device mode, core restored as device - 0: Host mode, core restored as host [30:29] p2hd_prt_spd (PRT speed) - 00: HS - 01: FS - 10: LS - 11: Reserved [28:27] p2hd_dev_enum_spd (Device enumerated speed) - 00: HS - 01: FS (30/60 MHz clk) - 10: LS - 11: FS (48 MHz clk) [26:20] mac_dev_addr (MAC device address) Device address [19] mac_termselect (Termination selection) - 0: HS_TERM (Program for High Speed) - 1: FS_TERM (Program for Full Speed) [18:17] mac_xcvrselect (Transceiver select) - 00: HS_XCVR (High Speed) - 01: FS_XCVR (Full Speed) - 10: LS_XCVR (Low Speed) - 11: LFS_XCVR (Reserved) [16] sh2pl_prt_ctl[0] - 1: prt_power enabled - 0: prt_power disabled [15:14] prt_clk_sel (Refer prt_clk_sel table)

Bit	Attr	Reset Value	Description
13	RW	0x0	EssRegRestored Essential Register Values Restored (Applicable only when Hibernation is enabled (OTG_EN_PWROPT=2). When a value of 1 is written to this field, it indicates that register values of essential registers have been restored.
12:10	RO	0x0	reserved
9	RO	0x0	RestoreMode Restore Mode (Applicable only when Hibernation is enabled (OTG_EN_PWROPT=2). The application should program this bit to specify the restore mode during RESTORE POINT before programming PCGCCTL.EssRegRest bit is set. Host Mode: 1'b0: Host Initiated Resume, Host Initiated Reset 1'b1: Device Initiated Remote Wake up Device Mode: 1'b0: Device Initiated Remote Wake up 1'b1: Host Initiated Resume, Host Initiated Reset
8	RW	0x0	ResetAfterSusp Reset After Suspend Applicable in Partial power-down mode. In partial power-down mode of operation, this bit needs to be set in host mode before clamp is removed if the host needs to issue reset after suspend. If this bit is not set, then the host issues resume after suspend. This bit is not applicable in device mode and non-partial power-down mode. In Hibernation mode, this bit needs to be set at RESTORE_POINT before PCGCCTL.EssRegRestored is set. In this case, PCGCCTL.restore_mode needs to be set to wait_restore.
7	RO	0x0	L1Suspended Deep Sleep This bit indicates that the PHY is in deep sleep when in L1 state.
6	RO	0x0	PhySleep PHY in Sleep This bit indicates that the PHY is in the Sleep state.
5	RW	0x0	Enbl_L1Gating Enable Sleep Clock Gating When this bit is set, core internal clock gating is enabled in Sleep state if the core cannot assert utmi_l1_suspend_n. When this bit is not set, the PHY clock is not gated in Sleep state.
4	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
3	RW	0x0	RstPdwnModule Reset Power-Down Modules This bit is valid only in Partial Power-Down mode. The application sets this bit when the power is turned off. The application clears this bit after the power is turned on and the PHY clock is up.
2	RW	0x0	PwrClmp Power Clamp This bit is valid only in Partial Power-Down mode (OTG_EN_PWROPT = 1). The application sets this bit before the power is turned off to clamp the signals between the power-on modules and the power-off modules. The application clears the bit to disable the clamping before the power is turned on.
1	RW	0x0	GateHclk Gate Hclk The application sets this bit to gate hclk to modules other than the AHB Slave and Master and wakeup logic when the USB is uspended or the session is not valid. The application clears this bit when the USB is resumed or a new session starts.
0	RW	0x0	StopPclk Stop Pclk The application sets this bit to stop the PHY clock (phy_clk) when the USB is suspended, the session is not valid, or the device is disconnected. The application clears this bit when the USB is resumed or a new session starts.

USBOTG_EPBUF0
Address: Operational Base + offset (0x1000)
Device endpoint 0 / host out channel 0 address

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	EPBUF0 From0x1000 to 0x2000, EPBUF for endport0

USBOTG_EPBUF1
Address: Operational Base + offset (0x2000)
Device endpoint 1 / host out channel 1 address

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	EPBUF1 From0x2000 to 0x3000, EPBUF for endport1

USBOTG_EPBUF2
Address: Operational Base + offset (0x3000)
Device endpoint 2 / host out channel 2 address

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Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	EPBUF2 From0x3000 to 0x4000, EPBUF for endport2

USBOTG_EPBUF3
Address: Operational Base + offset (0x4000)
Device endpoint 3 / host out channel 3 address

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	EPBUF3 From0x4000 to 0x5000, EPBUF for endport3

USBOTG_EPBUF4
Address: Operational Base + offset (0x5000)
Device endpoint 4 / host out channel 4 address

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	EPBUF4 From0x5000 to 0x6000, EPBUF for endport4

USBOTG_EPBUF5
Address: Operational Base + offset (0x6000)
Device endpoint 5 / host out channel 5 address

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	EPBUF5 From0x6000 to 0x7000, EPBUF for endport5

USBOTG_EPBUF6
Address: Operational Base + offset (0x7000)
Device endpoint 6 / host out channel 6 address

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	EPBUF6 From0x7000 to 0x8000, EPBUF for endport6

USBOTG_EPBUF7
Address: Operational Base + offset (0x8000)
Device endpoint 7 / host out channel 7 address

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	EPBUF7 From0x8000 to 0x9000, EPBUF for endport7

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11.7 Interface description

Table 11-1 USB OTG 2.0 Interface Description

Module Pin	Direction	Pad Name	pinmux
USB0PN	A	IO_USB0_PN	-
USBRBIAS	A	IO_USB_RBIAS_0	-
USB0PP	A	IO_USB0_PP	-
VBUS	A	IO_USB_VBUS_0	-
USB0ID	A	IO_USB0_ID	-
DRVVBUS	DP	IO_PWM0_OTGdrv_GPIO0N7pmuio2	GRF_GPIO0B_IOMUX[15:14]=2

***Note**: **A**—Analog pad ;**AP**—Analog power; **AG**—Analog ground ;**DP**—Digital power ;**DG**–Digital ground;*

11.8 Application Note

11.8.1 Suspend Mode

When PHY is in suspend state

- COMMONONN = 1'b1, 480M clock invalid
- COMMONONN = 1'b0, 480M clock output available.

Please refer to "Chapter GRF" for configuration details

11.8.2 Relative GRF Registers

USBPHY contains 284 bit registers to configure USB PHY. These bits are used to adjust DP/DM SI. Please refer to "Chapter GRF" for more details.

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Chapter 12 MIPI DSI HOST Controller

12.1 Overview

The Display Serial Interface (DSI) is part of a group of communication protocols defined by the MIPI Alliance. The MIPI DSI HOST Controller is a digital core that implements all protocol functions defined in the MIPI DSI Specification. The MIPI DSI HOST Controller provides an interface between the system and the MIPI D-PHY, allowing the communication with a DSI-compliant display. The MIPI DSI HOST Controller supports one to four lanes for data transmission with MIPI D-PHY.

The MIPI DSI HOST Controller supports the following features:

- Compliant with MIPI Alliance standards
- Support the DPI interface color coding mappings into 24-bit Interface
  - 16 bits per pixel, configurations 1,2,and 3
  - 18 bits per pixel, configurations 1 and 2
  - 24 bits per pixel
- Programmable polarity of all DPI interface signals
- Extended resolutions beyond the DPI standard maximum resolution of 800x480 pixels:
  - Up to 2047 vertical active lines
  - Up to 63 vertical back porch lines
  - Up to 63 vertical front porch lines
  - Maximum resolution is limited by available DSI Physical link bandwidth which depends on the number of lanes and maximum speed per lane
- Interface with MIPI D-PHY following PHY Protocol Interface (PPI), as defined in MIPI Alliance Specification for D-PHY
- Up to four D-PHY Data Lanes
- Bidirectional communication and escape mode support through data lane 0
- Transmission of all generic commands
- ECC and Checksum capabilities
- End of Transmission Packet(EOTp)
- Ultra Low-Power mode
- Fault recovery schemes

12.2 Block Diagram

The following diagram shows the MIPI DSI HOST Controller architecture.

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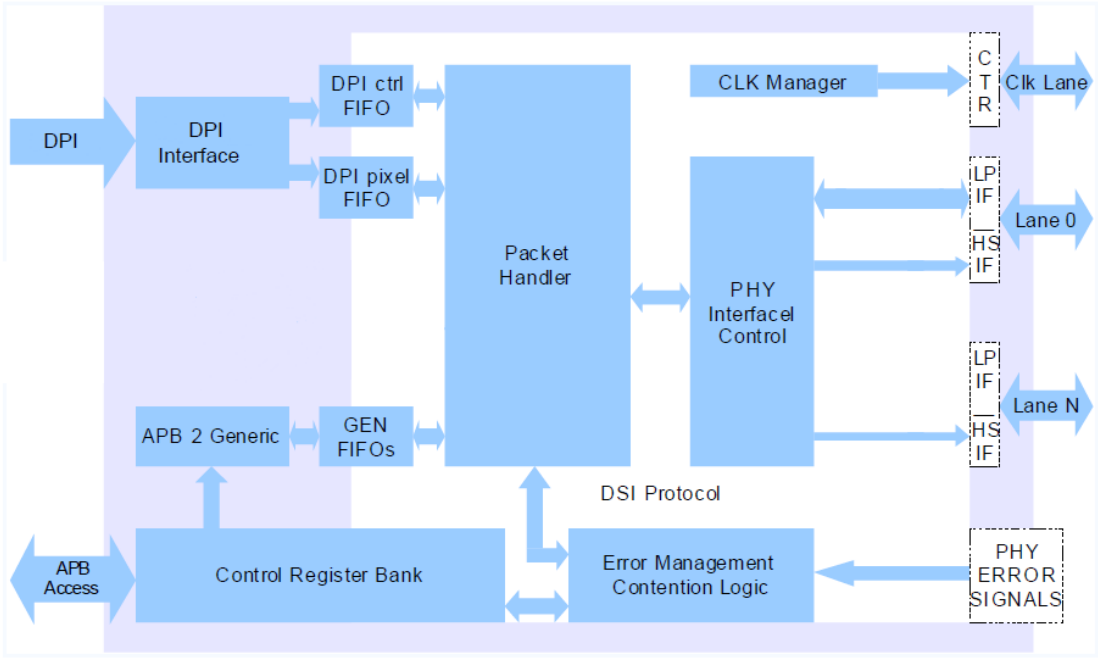


Fig. 12-1 MIPI DSI HOST Controller architecture

The DPI interface captures the data and control signals and conveys them to a FIFO for video control signals and another one for pixel data. This data is then used to build Video packets, hen in Video mode.

The Register Bank is accessible through a standard AMBA-APB slave interface, providing access to the MIPI DSI HOST Controller registers for configuration and control. There is also a fully programmable interrupt generator to inform the system about certain events.

The PHY Interface Control is responsible for managing the D-PHY PPI interface. It acknowledges the current operation and enables low-power transmission/reception or a high-speed transmission. It also performs data splitting between available D-PHY lanes for high-speed transmission.

The Packet Handler schedules the activities inside the link. It performs several functions based on the interfaces that are currently DPI and the video transmission mode that is used (burst mode or non-burst mode with sync pulse or sync events). It builds long or short packet generating correspondent ECC and CRC codes. This block also performs the following functions: Packet reception, Validation of packet header by checking the ECC, Header correction and notification for single-bit errors, Termination of reception, Multiple header error notification.

The APB-to-Generic block bridges the APB operations into FIFOs holding the Generic commands. The block interfaces with the following FIFOS: Command FIFO, Write payload FIFO, Read payload FIFO.

The Error Management notifies and monitors the error conditions on the DSI link. It controls the timers used to determine if a timeout condition occurred, performing an internal soft reset and triggering an interruption notification.

12.3 Function Description

12.3.1 DPI interface function

The DPI interface follows the MIPI DPI specification with pixel data bus width up to 24 bits. It is used to transmit the information in Video mode in which the transfers from the host processor to the peripheral take the form of a real-time pixel stream. This interface allows sending ShutDown (SD) and ColorMode (CM) commands, which are triggered directly by writing to the register of CFG_MISC_CON[2:1]. To transfer additional commands(for example, to initialize the display), use another interface such as APB Slave Generic Interface to complement the DPI interface.

The DPI interface captures the data and control signals and conveys them to the FIFO interfaces that transmit them to the DSI link. Two different streams of data are presented at

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the interface; video control signals and pixel data. Depending on the interface color coding, the pixel data is disposed differently throughout the dpipixdata bus. The following table shows the Interface pixel color coding.

Table 12-1 Color table

Signal Line	16-bit			18-bit		24-bit
	Config1	Config2	Config3	Config1	Config2	
dpipixdata23	Not used	Not used	Not used	Not used	Not used	R7
dpipixdata22	Not used	Not used	Not used	Not used	Not used	R6
dpipixdata21	Not used	Not used	R4	Not used	R5	R5
dpipixdata20	Not used	R4	R3	Not used	R4	R4
dpipixdata19	Not used	R3	R2	Not used	R3	R3
dpipixdata18	Not used	R2	R1	Not used	R2	R2
dpipixdata17	Not used	R1	R0	R5	R1	R1
dpipixdata16	Not used	R0	Not used	R4	R0	R0
dpipixdata15	R4	Not used	Not used	R3	Not used	G7
dpipixdata14	R3	Not used	Not used	R2	Not used	G6
dpipixdata13	R2	G5	G5	R1	G5	G5
dpipixdata12	R1	G4	G4	R0	G4	G4
dpipixdata11	R0	G3	G3	G5	G3	G3
dpipixdata10	G5	G2	G2	G4	G2	G2
dpipixdata9	G4	G1	G1	G3	G1	G1
dpipixdata8	G3	G0	G0	G2	G0	G0
dpipixdata7	G2	Not used	Not used	G1	Not used	B7
dpipixdata6	G1	Not used	Not used	G0	Not used	B6
dpipixdata5	G0	Not used	B5	B5	B5	B5
dpipixdata4	B4	B4	B4	B4	B4	B4
dpipixdata3	B3	B3	B3	B3	B3	B3
dpipixdata2	B2	B2	B2	B2	B2	B2
dpipixdata1	B1	B1	B1	B1	B1	B1
dpipixdata0	B0	B0	Not used	B0	B0	B0

The DPI interface can be configured to increase flexibility and promote correct usage of this interface for several systems. These configuration options are as follows:Polarity control: All the control signals are programmable to change the polarity depending on system requirements.

After the MIPI DSI HOST Controller reset, DPI waits for the first VSYNC active transition to start signal sampling, including pixel data, and preventing image transmission in the middle of a frame.

If interface pixel color coding is 18 bits and the 18-bit loosely packed stream is disabled, the number of lines programmed in the pixels per lines configuration is a multiple of four. This means that in this mode, the two LSBs in the configuration are always inferred as zero. The specification states that in this mode, the pixel line size should be a multiple of four.

12.3.2 APB Slave Generic Interface

The APB Slave interface allows the transmission of generic information in Command mode, and follows the proprietary register interface. Commands sent through this interface are not constrained to comply with the DCS specification, and can include generic commands described in the DSI specification as manufacturer-specific.

The MIPI DSI HOST Controller supports the transmission or write and read command mode packets as described in the DSI specification. These packets are built using the APB register access. The GEN_PLD_DATA register has two distinct functions based on the operation. Writing to this register sends the data as payload when sending a Command mode packet. Reading this register returns the payload of a read back operation. The GEN_HDR register contains the Command mode packet header type and header data. Writing to this register

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triggers the transmission of the packet implying that for a long Command mode packet, the packet's payload needs to be written in advance in the GEN_PLD_DATA register.
The valid packets available to be transmitted through the Generic interface are as follows:

- Generic Write Short Packet 0 Parameters
- Generic Write Short Packet 1 Parameters
- Generic Write Short Packet 2 Parameter
- Generic Write Short Packet 0 Parameter
- Generic Write Short Packet 1 Parameters
- Generic Write Short Packet 2 Parameter
- Maximum Read Packet Configuration
- Generic Long Write Packet
- DCS Write Short Packet 0 Parameter
- DCS Write Short Packet 1 Parameter
- DCS Write Short Packet 0 Parameter
- DCS Write Long Packet

A set of bits in the CMD_PKT_STATUS register report the status of the FIFOs associated with APB interface support.
Generic interface packets are always transported using one of the DSI transmission modes; Video mode or Command mode. If neither of these mode are selected, the packets are not transmitted through the link and the released FIFOs eventually get overflowed.
The transfer of packets through the APB bus is based on the following conditions:
The APB protocol defines that the write and read procedure takes two clock cycles each to be executed. This means that the maximum input data rate through the APB interfaces is always half the speed of the APB clock.
The data input bus has a maximum width of 32 bits. This allows for a relation to be defined between the input APB clock frequency and maximum bi rate achievable by the APB interface.
The DSI link bit rate when using solely APB is equal to (APB clock frequency) *16 Mbps.
The bandwidth is dependent on the APB clock frequency; the available bandwidth increases with the clock frequency.
To drive the APB interface to achieve high bandwidth Command mode traffic transported by the DSI link, the MIPI DSI HOST Controller should operate in the Command mode only and the APB interface should be the only data source that is currently in use. Thus, the APB interface has the entire bandwidth of the DSI link and does not share it with any another input interface source.
The memory write commands require maximum throughout from the APB interface, because they contain the most amount of data conveyed by the DSI link. While writing the packet information, first write the payload of a given packet into the payload FIFO using the GEN_PLD_DATA register. When the payload data is for the command parameters, place the first byte to be transmitted in the least sgnificant byte position of the APB data bus.
After writing the payload, write the packet header into the command FIFO. For more information and it should follow the pixel to byte conversion organization referred in the Annexure A of the DCS specification. The follow figures show how the pixel data should be orgavized in the APB data write bus. The memory write commands are conveyed in DCS long packets. DCS long packets are encapsulated in a DSI packet. The DSI included in the diagrams.In the follow figures, the Write Memory Command can be replaced by the DCS command Write Memory Start and Write Memory Continue.

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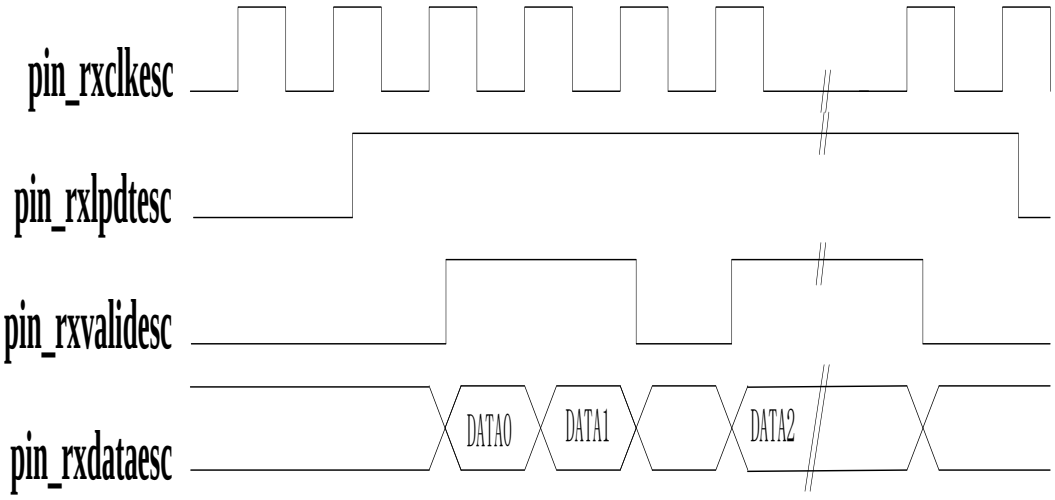


Fig. 12-2 24bpp APB Pixel to Byte Organization

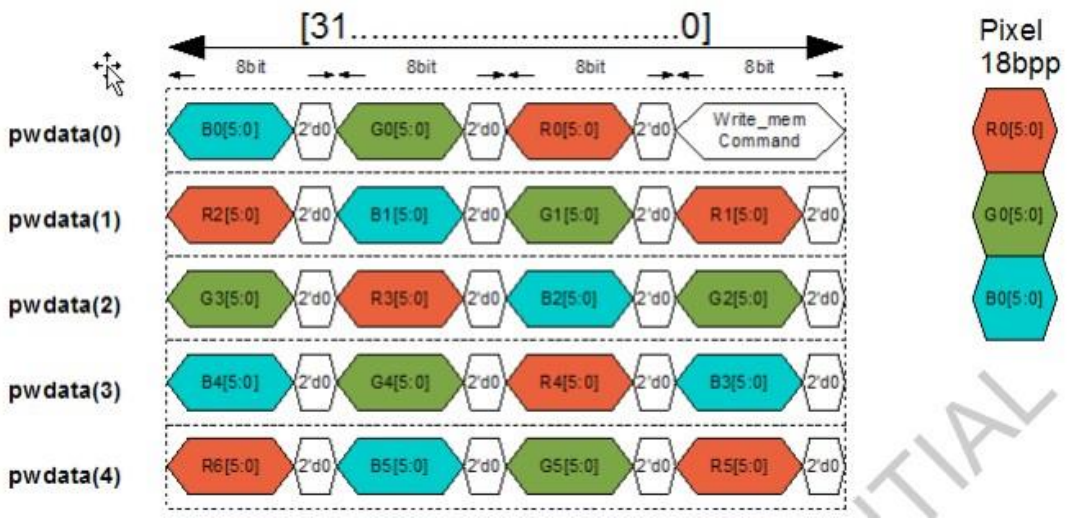


Fig. 12-3 18 bpp APB Pixel to Byte Organization

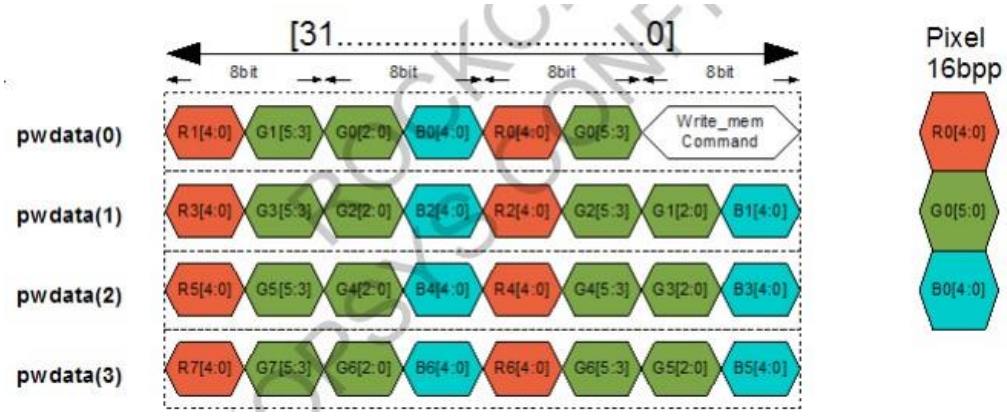


Fig. 12-4 16 bpp APB Pixel to Byte Organization

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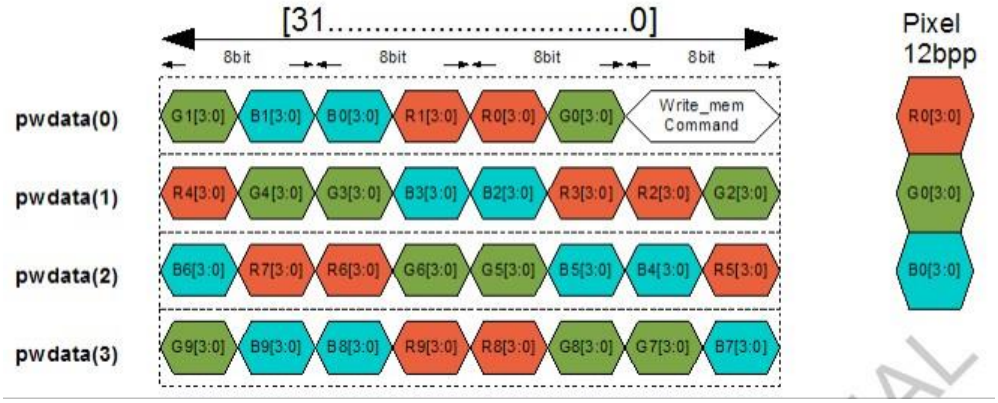


Fig. 12-5 12 bpp APB Pixel to Byte Organization



Fig. 12-6 8bpp APB Pixel to Byte Organization

12.3.3 Transmission of Commands in Video Mode

The MIPI DSI HOST Controller supports the transmission of commands, both in high-speed and low-power, while in Video mode. The DSI controller uses Blanking or Low-Power(BLLP) periods to transmit commands inserted through the APB Generic interface. Those periods correspond to the shaded areas of the following figure.

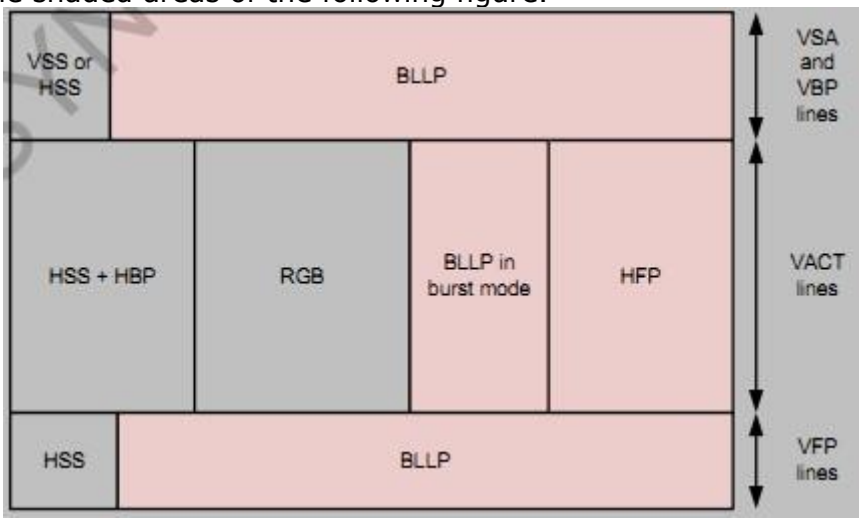


Fig. 12-7 Command Transmission Periods within the Image Area

Commands are transmitted in the blanking periods after the following packet/states:

- Bertical Sync Start (VSS) packets, if the Video Sync pulses are not enabled
- Horizontal Sync End (HSE) packets, in the VSA, VBP, and VFP regions
- Horizontal Sync Start (HSS) packets, if the Video Sync pulses are not enabled in the VSA, VBP, and VFP regions
- Horizontal Active (HACT) state

Only one command is transmitted per line, even in the case of the last line of a frame but one command is possible for each line.

The MIPI DSI HOST Controller avoids sending commands in the last line because it is possible that the last line is shorter than the other ones. For instance, the line time (tL) could be half a cycle longer than the tL on the DPI interface, that is, each line in the frame taking half a cycle from time for the last line. This results in the last line being (1/2 cycle) *

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(number of lines -1) shorter than tL.
The dpicolorm and dpishutdn input signals are also able to trigger the sending of command packets. The commands are DSI data types Color Mode On, Color Mode Off, Shut Down Peripheral, and Turn on Peripheral. These commands are not sent in the VACT region. If the lpcmden bit of the VID_MODE_CFG register is 1, these commands are sent in LP mode. In LP mode, the ouvact_lpcmd_time field of the LP_CMD_TIM register is used to determine if these commands can be transmitted. It is assumed that outvact_lpcmd_time is greater than or equal to 4 bytes (number of bytes in a short packet), because the DSI HOST does not transmit these commands on the last line.
If the frame_BTA_ack field is set in the VID_MODE_CFG register, a BTA is generated by DSI HOST after the last line of a frame. This may coincide with a write command or a read command. In either case, the edpihalt signal is held asserted until an acknowledge has been received (control of the DSI bus is returned to the host).
If the lpcmden bit of the VID_MODE_CFG register is set to 1, the commands are sent in low-power in Video mode. In this case, it is necessary to calculate the time available, in bytes, to transmit a command in LP mode for Horizontal Front Porch (HFP), Vertical Sync Active (VSA), Vertical Back Porch (VBP), and Vertical Front Porch(VFP) regions.
The outvact_lpcmd_time field of the LP_CMD_TIM register indicates the time available (in bytes) to transmit a command in LP mode, based on the escape clock, on a line during the VSA, VBP, and the VFP
Outvact_lpcmd_time=(tL-(Time to transmit HSS and HSE frames +tHSA+Time to enter and leave LP mode+Time to send the D-PHY LPDT command)) / escape clock period / 8 / 2
Where,
tL=Line time
tHSA=Time to send a short packet (for sync events) or time of the HAS pulse (for sync pulses)
In the above equation, division by eight is done to convert the time available to bytes and division by two is done because one bit is transmitted once in every two escape clock cycles.
The outvact_lpcmd_time filed can be compared directly with the size of the command to be transmitted to determine if there is enough time to transmit the command. The maximum size of a command that can be transmitted in LP mode is limited to 255 bytes by this field.
This register must be programmed to a value greater than or equal to 4 bytes for the transmission of the DCTRL commands such as shutdown and colorm in LP mode.
Consider an example with 12.6 μs per line and assume an escape clock frequency of 15 MHz. In this case, 189 escape clock cycles are available to enter and exit LP mode and transmit command. The following are assumed:
Sync pulses are not being transmitted
Two lane byte clock ticks are required to transmit a short packet
phy_lp2hs_time=16
phy_lp2p_time=20
In this example, a 11-byte command can be transmitted as follows:
outvact_lpcmd_time=(12.6μs-(2*10 ns)-(16*10 ns)-(20*10 ns)-(8*66 ns)) / 66 ns / 8 / 2 = 11 bytes
The invact_lpcmd_time field of the LP_CMD_TIM register indicates the time available (in bytes) to transmite a command in LP mode (based on the escape clock) in the Vertical Active (VACT) region. This time is calculated as follows:
Invact_lpcmd_time=((tHFP-Time to enter and leave low-power mode + Blanking period before the HFP when in Burst mode- Time to send the D-PHY LPDT command) / escape clock period) / 8
Where,
tHFP=line time-tHSA-tHBP-tHACT
tHACT=vid_pkt_size*bits_per_pixel*lane_byte_clock_period / num_lanes
The invact_lpcmd_time field can be compared directly with the size of the command to be transmitted to determined if there is time to transmit the command.
Consider an example where the refresh rate is 60 Hz. The number of lines is 1320 (typical). The tL in this case is 12.6μs. With a lane byte clock of 100 MHz, 1260 clock ticks are availabel to transmit a single frame. If 800 ticks are used for pixel data then 460 ticks

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(4.6μs) are available for Horizontal Sync Start (HSS), HFP, and HBP. Assuming that 2.3μs is available for HFP and the escape clock is 15MHz, only 34 LP clock ticks are available to enter LP, transmit a command, and return from LP mode. Approximately 12 escape clock ticks are required to enter and leave LP mode. Therefore, only 1 byte could be transmitted in this period.
A short packet (for example, generic short write) requires a minimum of 4 bytes. Therefore, in this exampled, commands are not sent in the VACT region. If Burst mode is enabled, more time is available to transmit commands in the VACT region. The following are assumed:
The controller is not in Burst mode
phy_lp2hs_time=16
phy_lp2hs_time=16
In this examplem invact_lpcmd_time is calculated as follows:
Invact_lpcmd_time = (2.3μs –(16*10 ns)-(20*10 ns)-(8*66 ns)) /66 ns / 8 = 2 bytes
The outvact_lpcmd_time and invact_lpcmd_time fields allow a simple comparision to determine if a command can be transmitted in any of the BLLP periods.
Following figure illustrates the meaning of invact_lpcmd_time and outvact_lpcmd_time, matching them with the shaded areas and the VACT region.

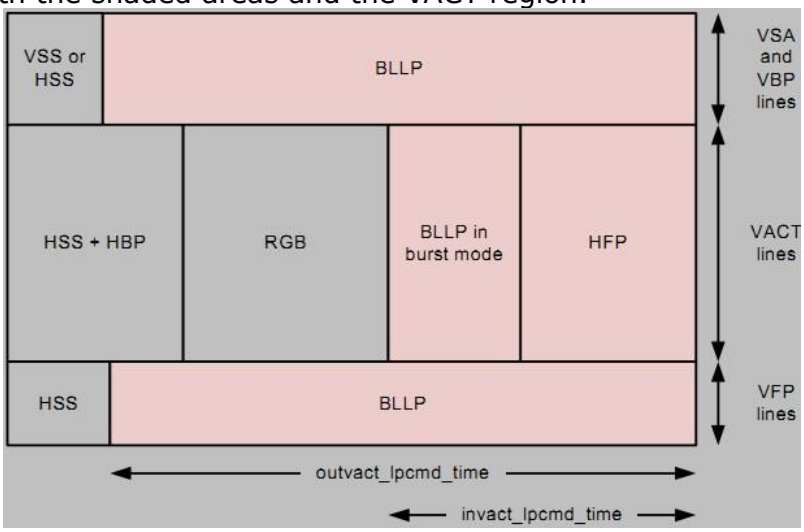


Fig. 12-8 Location in the Image Area

If the lpcmden bit of the VID_MODE_CFG register is 0, the commands are sent in high_speed in Video Mode. In this case, the DSI HOST automatically determines the area where each command can be sent and no programming or calculation is requied.
On read command Transmission, the max_rd_time field of the PHY_TMR_CFG register configures the maximum amount of time required to perform a read command in lane byte clock cycles.
The maximum time required to perform a read command in Lane byte clock cycles (max_rd_time) =Time to transmit the read command in LP mode + Time to enter and leave LP mode + Time to return the read data packet from the peripheral device.
The time to return the read data packet from the pripheral depends on the number of bytes read and the escape clock frequency of the peripheal; not the escape clock of the host. The max_rd_time field is used in both HS and LP mode to determine if there is time to complete a read command in a BLLP period.
In high-speed mode (lpcmden=0), max_rd_time is calculated as follows:
max_rd_time = phy_hs2lp_time + Time to return the read data packet from the peripheral device + phy_hs2hs_time
In low-power mode (lpcmden = 1), max_rd_time is calculated as follows:
max_rd_time = phy_hs2lp_time +LPDT command time + Read command time in LP mode + Time to return the data read from the peripheral device + phy_lp2hs_time
Where,
LPDT command time = (8*Host escape clock period) / Lane byte clock period
Read command time in LP mode = (32 * host escape clock period) / lane byte clock period
It is recommended to keep the maximum number of bytes read from the peripheral to a

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minimum to have sufficient time available to issue the read commands on a line. Ensure that max_rd_time* Lane byte clock period is less than outvact_lpcmd_time *8*Escape clock period of the host.
Otherwise, the read commands are serviced on the last line of a frame and the edpihalt signal may be asserted. If it is necessary to read a large number of parameters (＞16), increase the max_rd_time while the read command is being executed. When the read has completed, decrease the max_rd_time to a lower value.

12.4 Register Description

12.4.1 Internal Address Mapping

Slave address can be divided into different length for different usage, which is shown as follows.

12.4.2 Registers Summary

Name	Offset	Size	Reset Value	Description
MIPI_DSI_HOST_VERSION	0x0000	W	0x3133302a	VERSION
MIPI_DSI_HOST_PWR_UP	0x0004	W	0x00000000	power-up of the mipi dsi controller
MIPI_DSI_HOST_CLKMGR_CFG	0x0008	W	0x00000000	Clock mgr
MIPI_DSI_HOST_DPI_VCID	0x000c	W	0x00000000	DPI_VCID
MIPI_DSI_HOST_DPI_COLOR_CODING	0x0010	W	0x00000000	DPI_COLOR_CODING
MIPI_DSI_HOST_DPI_CFG_POL	0x0014	W	0x00000000	polarity of the DPI signals
MIPI_DSI_HOST_DPI_LP_CMD_TIM	0x0018	W	0x00000000	DPI_LP_CMD_TIM
MIPI_DSI_HOST_PCKHDL_CFG	0x002c	W	0x00000000	Register0000 Description
MIPI_DSI_HOST_GEN_VCID	0x0030	W	0x00000000	GEN_VCID
MIPI_DSI_HOST_MODE_CFG	0x0034	W	0x00000001	This register configures the mode of operation - Video mode or Command mode(Commands can be sent even in video mode too)
MIPI_DSI_HOST_VID_MODE_CFG	0x0038	W	0x00000000	VID_MODE_CFG
MIPI_DSI_HOST_VID_PKT_SIZE	0x003c	W	0x00000000	VID_PKT_SIZE
MIPI_DSI_HOST_VID_NUM_CHUNKS	0x0040	W	0x00000000	VID_NUM_CHUNKS
MIPI_DSI_HOST_VID_NULL_SIZE	0x0044	W	0x00000000	VID_NULL_SIZE

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Name	Offset	Size	Reset Value	Description
MIPI_DSI_HOST_VID_HSA_TIME	0x0048	W	0x00000000	VID_HSA_TIME
MIPI_DSI_HOST_VID_HBP_TIME	0x004c	W	0x00000000	VID_HBP_TIME
MIPI_DSI_HOST_VID_HLINE_TIME	0x0050	W	0x00000000	VID_HLINE_TIME
MIPI_DSI_HOST_VID_VSA_LINES	0x0054	W	0x00000000	VID_VSA_LINES
MIPI_DSI_HOST_VID_VBP_LINES	0x0058	W	0x00000000	VID_VBP_LINES
MIPI_DSI_HOST_VID_VFP_LINES	0x005c	W	0x00000000	VID_VFP_LINES
MIPI_DSI_HOST_VID_VACTIVE_LINES	0x0060	W	0x00000000	VID_VACTIVE_LINES
MIPI_DSI_HOST_EDPI_CMD_SIZE	0x0064	W	0x00000000	EDPI_CMD_SIZE
MIPI_DSI_HOST_CMD_MODE_CFG	0x0068	W	0x00000000	CMD_MODE_CFG
MIPI_DSI_HOST_GEN_HDR	0x006c	W	0x00000000	GEN_HDR
MIPI_DSI_HOST_GEN_PLD_DATA	0x0070	W	0x00000000	GEN_PLD_DATA
MIPI_DSI_HOST_CMD_PKT_STATUS	0x0074	W	0x00000000	CMD_PKT_STATUS
MIPI_DSI_HOST_TO_CNT_CFG	0x0078	W	0x00000000	TO_CNT_CFG
MIPI_DSI_HOST_HS_RD_TO_CNT	0x007c	W	0x00000000	HS_RD_TO_CNT
MIPI_DSI_HOST_LP_RD_TO_CNT	0x0080	W	0x00000000	LP_RD_TO_CNT
MIPI_DSI_HOST_HS_WR_TO_CNT	0x0084	W	0x00000000	HS_WR_TO_CNT
MIPI_DSI_HOST_LP_WR_TO_CNT	0x0088	W	0x00000000	LP_WR_TO_CNT
MIPI_DSI_HOST_BTA_TO_CNT	0x008c	W	0x00000000	BTA_TO_CNT
MIPI_DSI_HOST_SDF_3D	0x0090	W	0x00000000	SDF_3D
MIPI_DSI_HOST_LPCLK_CTRL	0x0094	W	0x00000000	LPCLK_CTRL
MIPI_DSI_HOST_PHY_TMR_LPCLK_CFG	0x0098	W	0x00000000	PHY_TMR_LPCLK_CFG
MIPI_DSI_HOST_PHY_TMR_CFG	0x009c	W	0x00000000	PHY_TMR_CFG

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Name	Offset	Size	Reset Value	Description
MIPI_DSI_HOST_PHY_RSTZ	0x00a0	W	0x00000000	PHY_RSTZ
MIPI_DSI_HOST_PHY_IF_CFG	0x00a4	W	0x00000003	PHY_IF_CFG
MIPI_DSI_HOST_PHY_STATUS	0x00b0	W	0x00000000	PHY_STATUS
MIPI_DSI_HOST_INT_ST0	0x00bc	W	0x00000000	INT_ST0
MIPI_DSI_HOST_INT_ST1	0x00c0	W	0x00000000	INT_ST1
MIPI_DSI_HOST_INT_MSK0	0x00c4	W	0x00000000	INT_ST0
MIPI_DSI_HOST_INT_MSK1	0x00c8	W	0x00000000	INT_MSK1
MIPI_DSI_HOST_INT_FORCE0	0x00d8	W	0x00000000	INT_FORCE0
MIPI_DSI_HOST_INT_FORCE1	0x00dc	W	0x00000000	INT_FORCE1
MIPI_DSI_HOST_VID_SHADOW_CTRL	0x0100	W	0x00000000	VID_SHADOW_CTRL
MIPI_DSI_HOST_DPI_VCID_ACT	0x010c	W	0x00000000	DPI_VCID_ACT
MIPI_DSI_HOST_DPI_COLOR_CODING_ACT	0x0110	W	0x00000000	DPI_COLOR_CODING_ACT
MIPI_DSI_HOST_DPI_LP_CMD_TIM_ACT	0x0118	W	0x00000000	DPI_LP_CMD_TIM_ACT
MIPI_DSI_HOST_VID_MODE_CFG_ACT	0x0138	W	0x00000000	VID_MODE_CFG_ACT
MIPI_DSI_HOST_VID_PKT_SIZE_ACT	0x013c	W	0x00000000	VID_PKT_SIZE_ACT
MIPI_DSI_HOST_VID_NUM_CHUNKS_ACT	0x0140	W	0x00000000	VID_NUM_CHUNKS_ACT
MIPI_DSI_HOST_VID_NULL_SIZE_ACT	0x0144	W	0x00000000	VID_NULL_SIZE_ACT
MIPI_DSI_HOST_VID_HSA_TIME_ACT	0x0148	W	0x00000000	VID_HSA_TIME_ACT
MIPI_DSI_HOST_VID_HBP_TIME_ACT	0x014c	W	0x00000000	VID_HBP_TIME_ACT
MIPI_DSI_HOST_VID_HLINE_TIME_ACT	0x0150	W	0x00000000	VID_HLINE_TIME_ACT
MIPI_DSI_HOST_VID_VSA_LINES_ACT	0x0154	W	0x00000000	VID_VSA_LINES_ACT
MIPI_DSI_HOST_VID_VBP_LINES_ACT	0x0158	W	0x00000000	VID_VBP_LINES_ACT

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Name	Offset	Size	Reset Value	Description
MIPI_DSI_HOST_VID_VFP_LINES_ACT	0x015c	W	0x00000000	VID_VFP_LINES_ACT
MIPI_DSI_HOST_VID_VACTIVE_LINES_ACT	0x0160	W	0x00000000	VID_VACTIVE_LINES_ACT
MIPI_DSI_HOST_SDF_3D_ACT	0x0190	W	0x00000000	SDF_3D_ACT

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

12.4.3 Detail Register Description

MIPI_DSI_HOST_VERSION

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:0	RW	0x3133302a	VERSION VERSION

MIPI_DSI_HOST_PWR_UP

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	shutdownz This bit configures the core either to power up or to reset. shutdownz is the soft reset register. Its default value is 0. After the core configuration, to enable the DWC_mipi_dsi_host, set this register to 1. 0: Reset 1: Power-up

MIPI_DSI_HOST_CLKMGR_CFG

Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
15:8	RW	0x00	to_clk_division This field indicates the division factor for the Time Out clock used as the timing unit in the configuration of HS to LP and LP to HS transition error
7:0	RW	0x00	tx_esc_clk_division This field indicates the division factor for the TX Escape clock source (lanebyteclk). The values 0 and 1 stop the TX_ESC clock generation

MIPI_DSI_HOST_DPI_VCID

Address: Operational Base + offset (0x000c)

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1:0	RW	0x0	dpi_vcid This field configures the DPI virtual channel id that is indexed to the Video mode packets

MIPI_DSI_HOST_DPI_COLOR_CODING

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:9	RO	0x0	reserved
8	RW	0x0	loosely18_en When set to 1, this bit activates loosely packed variant to 18-bit configurations
7:4	RO	0x0	reserved

Bit	Attr	Reset Value	Description
3:0	RW	0x0	dpi_color_coding This field configures the DPI color coding as follows: 0000: 16-bit configuration 1 0001: 16-bit configuration 2 0010: 16-bit configuration 3 0011: 18-bit configuration 1 0100: 18-bit configuration 2 0101: 24-bit 0110: 20-bit YCbCr 4:2:2 loosely packed 0111: 24-bit YCbCr 4:2:2 1000: 16-bit YCbCr 4:2:2 1001: 30-bit 1010: 36-bit 1011-1111: 12-bit YCbCr 4:2:0

MIPI_DSI_HOST_DPI_CFG_POL

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4	RW	0x0	colorm_active_low When set to 1, this bit configures the color mode pin (dpicolorm) as active low
3	RW	0x0	shutd_active_low When set to 1, this bit configures the shutdown pin (dpishutdn) as active low
2	RW	0x0	hsync_active_low When set to 1, this bit configures the horizontal synchronism pin (dpihsync) as active low

Bit	Attr	Reset Value	Description
1	RW	0x0	vsync_active_low When set to 1, this bit configures the vertical synchronism pin (dpivsync) as active low
0	RW	0x0	dataen_active_low When set to 1, this bit configures the data enable pin (dpidataen) as active low

MIPI_DSI_HOST_DPI_LP_CMD_TIM

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:16	RW	0x00	outvact_lpcmd_time This field is used for the transmission of commands in low-power mode. It defines the size, in bytes, of the largest packet that can fit in a line during the VSA, VBP, and VFP regions
15:8	RO	0x0	reserved
7:0	RW	0x00	invact_lpcmd_time This field is used for the transmission of commands in low-power mode. It defines the size, in bytes, of the largest packet that can fit in a line during the VACT region

MIPI_DSI_HOST_PCKHDL_CFG

Address: Operational Base + offset (0x002c)

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4	RW	0x0	crc_rx_en When set to 1, this bit enables the CRC reception and error reporting

Bit	Attr	Reset Value	Description
3	RW	0x0	ecc_rx_en When set to 1, this bit enables the ECC reception, error correction, and reporting
2	RW	0x0	bta_en When set to 1, this bit enables the Bus Turn-Around (BTA) request
1	RW	0x0	eotp_rx_en When set to 1, this bit enables the EoTp reception
0	RW	0x0	eotp_tx_en When set to 1, this bit enables the EoTp transmission

MIPI_DSI_HOST_GEN_VCID

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1:0	RW	0x0	gen_vcid_rx This field indicates the Generic interface read-back virtual channel identification

MIPI_DSI_HOST_MODE_CFG

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x1	cmd_video_mode This bit configures the operation mode: ■0: Video mode ■1: Command mode

MIPI_DSI_HOST_VID_MODE_CFG

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Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24	RW	0x0	vpg_orientation This field indicates the color bar orientation as follows: 0: Vertical mode 1: Horizontal mode
23:21	RO	0x0	reserved
20	RW	0x0	vpg_mode This field is to select the pattern: 0: Color bar (horizontal or vertical) 1: BER pattern (vertical only)
19:17	RO	0x0	reserved
16	RW	0x0	vpg_en When set to 1, this bit enables the video mode pattern generator
15	RW	0x0	lp_cmd_en When set to 1, this bit enables the command transmission only in lowpower mode
14	RW	0x0	frame_bta_ack_en When set to 1, this bit enables the request for an acknowledge response at the end of a frame
13	RW	0x0	lp_hfp_en When set to 1, this bit enables the return to low-power inside the Horizontal Front Porch (HFP) period when timing allows
12	RW	0x0	lp_hbp_en When set to 1, this bit enables the return to low-power inside the Horizontal Back Porch (HBP) period when timing allows

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Bit	Attr	Reset Value	Description
11	RW	0x0	lp_vact_en When set to 1, this bit enables the return to low-power inside the Vertical Active (VACT) period when timing allows
10	RW	0x0	lp_vfp_en When set to 1, this bit enables the return to low-power inside the Vertical Front Porch (VFP) period when timing allows
9	RW	0x0	lp_vbp_en When set to 1, this bit enables the return to low-power inside the Vertical Back Porch (VBP) period when timing allows
8	RW	0x0	lp_vsa_en When set to 1, this bit enables the return to low-power inside the Vertical Sync Time (VSA) period when timing allows
7:2	RO	0x0	reserved
1:0	RW	0x0	vid_mode_type This field indicates the video mode transmission type as follows: 2'b00: Non-burst with sync pulses 2'b01: Non-burst with sync events 2'b10 and 2'b11: Burst mode

MIPI_DSI_HOST_VID_PKT_SIZE

Address: Operational Base + offset (0x003c)

Bit	Attr	Reset Value	Description
31:14	RO	0x0	reserved

Bit	Attr	Reset Value	Description
13:0	RW	0x0000	vid_pkt_size This field configures the number of pixels in a single video packet. For 18-bit not loosely packed data types, this number must be a multiple of 4. For YCbCr data types, it must be a multiple of 2, as described in the DSI specification

MIPI_DSI_HOST_VID_NUM_CHUNKS

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12:0	RW	0x0000	vid_num_chunks This register configures the number of chunks to be transmitted during a Line period (a chunk consists of a video packet and a null packet). If set to 0 or 1, the video line is transmitted in a single packet. If set to 1, the packet is part of a chunk, so a null packet follows it if vid_null_size > 0. Otherwise, multiple chunks are used to transmit each video line

MIPI_DSI_HOST_VID_NULL_SIZE

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12:0	RW	0x0000	vid_null_size This register configures the number of bytes inside a null packet. Setting it to 0 disables the null packets

MIPI_DSI_HOST_VID_HSA_TIME

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Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0x000	vid_hsa_time This field configures the Horizontal Synchronism Active period in lane byte clock cycles

MIPI_DSI_HOST_VID_HBP_TIME

Address: Operational Base + offset (0x004c)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0x000	vid_hsa_time This field configures the Horizontal Synchronism Active period in lane byte clock cycles

MIPI_DSI_HOST_VID_HLINE_TIME

Address: Operational Base + offset (0x0050)

Bit	Attr	Reset Value	Description
31:15	RO	0x0	reserved
14:0	RW	0x0000	vid_hline_time This field configures the size of the total line time (HSA+HBP+HACT+HFP) counted in lane byte clock cycles

MIPI_DSI_HOST_VID_VSA_LINES

Address: Operational Base + offset (0x0054)

Bit	Attr	Reset Value	Description
31:10	RO	0x0	reserved
9:0	RW	0x000	vsa_lines This field configures the Vertical Synchronism Active period measured in number of horizontal lines

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MIPI_DSI_HOST_VID_VBP_LINES

Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31:10	RO	0x0	reserved
9:0	RW	0x000	vbp_lines This field configures the Vertical Back Porch period measured in number of horizontal lines

MIPI_DSI_HOST_VID_VFP_LINES

Address: Operational Base + offset (0x005c)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	vfp_lines This field configures the Vertical Front Porch period measured in number of horizontal lines

MIPI_DSI_HOST_VID_VACTIVE_LINES

Address: Operational Base + offset (0x0060)

Bit	Attr	Reset Value	Description
31:14	RO	0x0	reserved
13:0	RW	0x0000	v_active_lines This field configures the Vertical Active period measured in number of horizontal lines

MIPI_DSI_HOST_EDPI_CMD_SIZE

Address: Operational Base + offset (0x0064)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0000	edpi_allowed_cmd_size This field configures the maximum allowed size for an eDPI write memory command, measured in pixels. Automatic partitioning of data obtained from eDPI is permanently enabled

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MIPI_DSI_HOST_CMD_MODE_CFG

Address: Operational Base + offset (0x0068)

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24	RW	0x0	max_rd_pkt_size This bit configures the maximum read packet size command transmission type: 1'b0: High-speed 1'b1: Low-power
23:20	RO	0x0	reserved
19	RW	0x0	dcs_lw_tx This bit configures the DCS long write packet command transmission type: 1'b0: High-speed 1'b1: Low-power
18	RW	0x0	dcs_sr_0p_tx This bit configures the DCS short read packet with zero parameter command transmission type: 1'b0: High-speed 1'b1: Low-power
17	RW	0x0	dcs_sw_1p_tx This bit configures the DCS short write packet with one parameter command transmission type: 1'b0: High-speed 1'b1: Low-power

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Bit	Attr	Reset Value	Description
16	RW	0x0	dcs_sw_0p_tx This bit configures the DCS short write packet with zero parameter command transmission type: 1'b0: High-speed 1'b1: Low-power
15	RO	0x0	reserved
14	RW	0x0	gen_lw_tx This bit configures the Generic long write packet command transmission type: 1'b0: High-speed 1'b1: Low-power
13	RW	0x0	gen_sr_2p_tx This bit configures the Generic short read packet with two parameters command transmission type: 1'b0: High-speed 1'b1: Low-power
12	RW	0x0	gen_sr_1p_tx This bit configures the Generic short read packet with one parameter command transmission type: 1'b0: High-speed 1'b1: Low-power

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Bit	Attr	Reset Value	Description
11	RW	0x0	gen_sr_0p_tx This bit configures the Generic short read packet with zero parameter command transmission type: 1'b0: High-speed 1'b1: Low-power
10	RW	0x0	gen_sw_2p_tx This bit configures the Generic short write packet with two parameters command transmission type: 1'b0: High-speed 1'b1: Low-power
9	RW	0x0	gen_sw_1p_tx This bit configures the Generic short write packet with one parameter command transmission type: 1'b0: High-speed 1'b1: Low-power
8	RW	0x0	gen_sw_0p_tx This bit configures the Generic short write packet with zero parameter command transmission type: 1'b0: High-speed 1'b1: Low-power
7:2	RO	0x0	reserved
1	RW	0x0	ack_rqst_en When set to 1, this bit enables the acknowledge request after each packet transmission

Bit	Attr	Reset Value	Description
0	RW	0x0	tear_fx_en When set to 1, this bit enables the tearing effect acknowledge request

MIPI_DSI_HOST_GEN_HDR

Address: Operational Base + offset (0x006c)

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:16	RW	0x00	gen_wc_msbyte gen_wc_msbyte
15:8	RW	0x00	gen_wc_lsbyte This field configures the least significant byte of the header packet's Word count for long packets or data 0 for short packets
7:6	RW	0x0	gen_vc This field configures the virtual channel id of the header packet
5:0	RW	0x00	gen_dt This field configures the packet data type of the header packet

MIPI_DSI_HOST_GEN_PLD_DATA

Address: Operational Base + offset (0x0070)

Bit	Attr	Reset Value	Description
31:24	RW	0x00	gen_pld_b4 This field indicates byte 4 of the packet payload
23:16	RW	0x00	gen_pld_b3 This field indicates byte 3 of the packet payload
15:8	RW	0x00	gen_pld_b2 This field indicates byte 2 of the packet payload

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Bit	Attr	Reset Value	Description
7:0	RW	0x00	gen_pld_b1 This field indicates byte 1 of the packet payload

MIPI_DSI_HOST_CMD_PKT_STATUS

Address: Operational Base + offset (0x0074)

Bit	Attr	Reset Value	Description
31:15	RO	0x0	reserved
14	RW	0x0	dbi_rd_cmd_busy This bit is set when a read command is issued and cleared when the entire response is stored in the FIFO
13	RO	0x0	dbi_pld_r_full This bit indicates the full status of the DBI read payload FIFO
12	RO	0x0	dbi_pld_r_empty This bit indicates the empty status of the DBI read payload FIFO
11	RO	0x0	dbi_pld_w_full This bit indicates the full status of the DBI write payload FIFO
10	RO	0x0	dbi_pld_w_empty This bit indicates the empty status of the DBI write payload FIFO
9	RO	0x0	dbi_cmd_full This bit indicates the full status of the DBI command FIFO
8	RO	0x0	dbi_cmd_empy This bit indicates the empty status of the DBI command FIFO
7	RO	0x0	reserved
6	RO	0x0	gen_rd_cmd_busy This bit is set when a read command is issued and cleared when the entire response is stored in the FIFO
5	RO	0x0	gen_pld_r_full This bit indicates the full status of the generic read payload FIFO

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Bit	Attr	Reset Value	Description
4	RO	0x0	gen_pld_r_empty This bit indicates the empty status of the generic read payload FIFO
3	RO	0x0	gen_pld_w_full This bit indicates the full status of the generic write payload FIFO
2	RO	0x0	gen_pld_w_empty This bit indicates the empty status of the generic write payload FIFO
1	RO	0x0	gen_cmd_full This bit indicates the full status of the generic command FIFO
0	RO	0x0	gen_cmd_empty This bit indicates the empty status of the generic command FIFO

MIPI_DSI_HOST_TO_CNT_CFG
Address: Operational Base + offset (0x0078)

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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	hstx_to_cnt This field configures the timeout counter that triggers a high-speed transmission timeout contention detection (measured in TO_CLK_DIVISION cycles). If using the non-burst mode and there is no sufficient time to switch from HS to LP and back in the period which is from one line data finishing to the next line sync start, the DSI link returns the LP state once per frame, then you should configure the TO_CLK_DIVISION and hstx_to_cnt to be in accordance with: hstx_to_cnt * lanebyteclkperiod * TO_CLK_DIVISION >= the time of one FRAME data transmission * (1 + 10%) In burst mode, RGB pixel packets are time-compressed, leaving more time during a scan line. Therefore, if in burst mode and there is sufficient time to switch from HS to LP and back in the period of time from one line data finishing to the next line sync start, the DSI link can return LP mode and back in this time interval to save power. For this, configure the TO_CLK_DIVISION and hstx_to_cnt to be in accordance with: hstx_to_cnt * lanebyteclkperiod * TO_CLK_DIVISION >= the time of one LINE data transmission * (1 + 10%)

15:0	RW	0x0000	lprx_to_cnt This field configures the timeout counter that triggers a low-power reception timeout contention detection (measured in TO_CLK_DIVISION cycles)

MIPI_DSI_HOST_HS_RD_TO_CNT

Address: Operational Base + offset (0x007c)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0000	hs_rd_to_cnt This field sets a period for which the DWC_mipi_dsi_host keeps the link still, after sending a high-speed read operation. This period is measured in cycles of lanebyteclk. The counting starts when the D-PHY enters the Stop state and causes no interrupts

MIPI_DSI_HOST_LP_RD_TO_CNT

Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0000	lp_rd_to_cnt This field sets a period for which the DWC_mipi_dsi_host keeps the link still, after sending a low-power read operation. This period is measured in cycles of lanebyteclk. The counting starts when the D-PHY enters the Stop state and causes no interrupts

MIPI_DSI_HOST_HS_WR_TO_CNT

Address: Operational Base + offset (0x0084)

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
24	RW	0x0	presp_to_mode When set to 1, this bit ensures that the peripheral response timeout caused by hs_wr_to_cnt is used only once per eDPI frame, when both the following conditions are met: dpivsync_edpiwms has risen and fallen. Packets originated from eDPI have been transmitted and its FIFO is empty again. In this scenario no non-eDPI requests are sent to the D-PHY, even if there is traffic from generic or DBI ready to be sent, making it return to stop state. When it does so, PRESP_TO counter is activated and only when it finishes does the controller send any other traffic that is ready
23:16	RO	0x0	reserved
15:0	RW	0x0000	hs_wr_to_cnt This field sets a period for which the DWC_mipi_dsi_host keeps the link inactive after sending a high-speed write operation. This period is measured in cycles of lanebyteclk. The counting starts when the D-PHY enters the Stop state and causes no interrupts

MIPI_DSI_HOST_LP_WR_TO_CNT

Address: Operational Base + offset (0x0088)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	lp_wr_to_cnt This field sets a period for which the DWC_mipi_dsi_host keeps the link still, after sending a low-power write operation. This period is measured in cycles of lanebyteclk. The counting starts when the D-PHY enters the Stop state and causes no interrupts

MIPI_DSI_HOST_BTA_TO_CNT

Address: Operational Base + offset (0x008c)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	bta_to_cnt This field sets a period for which the DWC_mipi_dsi_host keeps the link still, after completing a Bus Turn-Around. This period is measured in cycles of lanebyteclk. The counting starts when the D-PHY enters the Stop state and causes no interrupts

MIPI_DSI_HOST_SDF_3D

Address: Operational Base + offset (0x0090)

Bit	Attr	Reset Value	Description
31:17	RO	0x0	reserved
16	RW	0x0	send_3d_cfg When set, causes the next VSS packet to include 3D control payload in every VSS packet
15:6	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
5	RW	0x0	right_first This bit defines the left or right order: 1'b0: Left eye data is sent first, and then the right eye data is sent. 1'b1: Right eye data is sent first, and then the left eye data is sent
4	RW	0x0	second_vsync This field defines whether there is a second VSYNC pulse between Left and Right Images, when 3D Image Format is Frame-based: 1'b0: No sync pulses between left and right data 1'b1: Sync pulse (HSYNC, VSYNC, blanking) between left and right data
3:2	RW	0x0	format_3d This field defines the 3D image format: 2'b00: Line (alternating lines of left and right data) 2'b01: Frame (alternating frames of left and right data) 2'b10: Pixel (alternating pixels of left and right data) 2'b11: Reserved
1:0	RW	0x0	mode_3d This field defines the 3D mode on/off and display orientation: 2'b00: 3D mode off (2D mode on) 2'b01: 3D mode on, portrait orientation 2'b10: 3D mode on, landscape orientation 2'b11: Reserved

MIPI_DSI_HOST_LPCLK_CTRL
Address: Operational Base + offset (0x0094)

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Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x0	auto_clklane_ctrl This bit enables the automatic mechanism to stop providing clock in the clock lane when time allows
0	RW	0x0	phy_txrequestclkhs This bit controls the D-PHY PPI txrequestclkhs signal

MIPI_DSI_HOST_PHY_TMR_LPCLK_CFG
Address: Operational Base + offset (0x0098)

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:16	RW	0x000	phy_clkhs2lp_time This field configures the maximum time that the D-PHY clock lane takes to go from high-speed to low-power transmission measured in lane byte clock cycles
15:10	RO	0x0	reserved
9:0	RW	0x000	phy_clklp2hs_time This field configures the maximum time that the D-PHY clock lane takes to go from low-power to high-speed transmission measured in lane byte clock cycles

MIPI_DSI_HOST_PHY_TMR_CFG
Address: Operational Base + offset (0x009c)

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Bit	Attr	Reset Value	Description
31:24	RW	0x00	phy_hs2lp_time This field configures the maximum time that the D-PHY data lanes take to go from high-speed to low-power transmission measured in lane byte clock cycles
23:16	RW	0x00	phy_lp2hs_time This field configures the maximum time that the D-PHY data lanes take to go from low-power to high-speed transmission measured in lane byte clock cycles
15	RO	0x0	reserved
14:0	RW	0x0000	max_rd_time This field configures the maximum time required to perform a read command in lane byte clock cycles. This register can only be modified when no read command is in progress

MIPI_DSI_HOST_PHY_RSTZ

Address: Operational Base + offset (0x00a0)

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3	RW	0x0	phy_forcepll When the D-PHY is in ULPS, this bit enables the D-PHY PLL. Dependency: DSI_HOST_FPGA = 0. Otherwise, this bit is reserved
2	RW	0x0	phy_enableclk When set to1, this bit enables the D-PHY Clock Lane module

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Bit	Attr	Reset Value	Description
1	RW	0x0	phy_rstz When set to 0, this bit places the digital section of the D-PHY in the reset state
0	RW	0x0	phy_shutdownz When set to 0, this bit places the D-PHY macro in power-down state

MIPI_DSI_HOST_PHY_IF_CFG

Address: Operational Base + offset (0x00a4)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:8	RW	0x00	phy_stop_wait_time This field configures the minimum wait period to request a high-speed transmission after the Stop state
7:2	RO	0x0	reserved
1:0	RW	0x3	n_lanes This field configures the number of active data lanes: 2'b00: One data lane (lane 0) 2'b01: Two data lanes (lanes 0 and 1) 2'b10: Three data lanes (lanes 0, 1, and 2) 2'b11: Four data lanes (lanes 0, 1, 2, and 3)

MIPI_DSI_HOST_PHY_STATUS

Address: Operational Base + offset (0x00b0)

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12	RO	0x0	phy_ulpsactivenot3lane This bit indicates the status of ulpsactivenot3lane D-PHY signal

Bit	Attr	Reset Value	Description
11	RO	0x0	phy_stopstate3lane This bit indicates the status of phystopstate3lane D-PHY signal
10	RO	0x0	phy_ulpsactivenot2lane This bit indicates the status of ulpsactivenot2lane D-PHY signal
9	RO	0x0	phy_stopstate2lane This bit indicates the status of phystopstate2lane D-PHY signal
8	RO	0x0	phy_ulpsactivenot1lane This bit indicates the status of ulpsactivenot1lane D-PHY signal
7	RO	0x0	phy_stopstate1lane This bit indicates the status of phystopstate1lane D-PHY signal
6	RO	0x0	phy_rxulpsesc0lane This bit indicates the status of rxulpsesc0lane D-PHY signal
5	RO	0x0	phy_ulpsactivenot0lane This bit indicates the status of ulpsactivenot0lane D-PHY signal
4	RO	0x0	phy_stopstate0lane This bit indicates the status of phystopstate0lane D-PHY signal
3	RO	0x0	phy_ulpsactivenotclk This bit indicates the status of phyulpsactivenotclk D-PHY signal
2	RO	0x0	phy_stopstateclklane This bit indicates the status of phystopstateclklane D-PHY signal
1	RO	0x0	phy_direction This bit indicates the status of phydirection D-PHY signal
0	RO	0x0	phy_lock This bit indicates the status of phylock D-PHY signal

MIPI_DSI_HOST_INT_ST0

Address: Operational Base + offset (0x00bc)

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Bit	Attr	Reset Value	Description
31:21	RO	0x0	reserved
20	RO	0x0	dphy_errors_4 This bit indicates the LP1 contention error ErrContentionLP1 from Lane 0
19	RW	0x0	dphy_errors_3 This bit indicates the LP0 contention error ErrContentionLP0 from Lane 0
18	RO	0x0	dphy_errors_2 This bit indicates the ErrControl error from Lane 0
17	RO	0x0	dphy_errors_1 This bit indicates ErrSyncEsc low-power data transmission synchronization error from Lane 0
16	RO	0x0	dphy_errors_0 This bit indicates ErrEsc escape entry error from Lane 0
15	RO	0x0	ack_with_err_15 This bit retrieves the DSI protocol violation from the Acknowledge error report
14	RO	0x0	ack_with_err_14 This bit retrieves the reserved (specific to device) from the Acknowledge error report
13	RO	0x0	ack_with_err_13 This bit retrieves the invalid transmission length from the Acknowledge error report
12	RO	0x0	ack_with_err_12 This bit retrieves the DSI VC ID Invalid from the Acknowledge error report
11	RO	0x0	ack_with_err_11 This bit retrieves the not recognized DSI data type from the Acknowledge error report

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Bit	Attr	Reset Value	Description
10	RO	0x0	ack_with_err_10 This bit retrieves the checksum error (long packet only) from the Acknowledge error report
9	RO	0x0	ack_with_err_9 This bit retrieves the ECC error, multi-bit (detected, not corrected) from the Acknowledge error
8	RO	0x0	ack_with_err_8 This bit retrieves the ECC error, single-bit (detected and corrected) from the Acknowledge error
7	RO	0x0	ack_with_err_7 This bit retrieves the reserved (specific to device) from the Acknowledge error report
6	RO	0x0	ack_with_err_6 This bit retrieves the False Control error from the Acknowledge error report
5	RO	0x0	ack_with_err_5 This bit retrieves the Peripheral Timeout error from the Acknowledge Error report
4	RO	0x0	ack_with_err_4 This bit retrieves the LP Transmit Sync error from the Acknowledge error report
3	RO	0x0	ack_with_err_3 This bit retrieves the Escape Mode Entry Command error from the Acknowledge error report
2	RO	0x0	ack_with_err_2 This bit retrieves the EoT Sync error from the Acknowledge error report
1	RO	0x0	ack_with_err_1 This bit retrieves the SoT Sync error from the Acknowledge error report

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Bit	Attr	Reset Value	Description
0	RO	0x0	ack_with_err_0 This bit retrieves the SoT error from the Acknowledge error report

MIPI_DSI_HOST_INT_ST1

Address: Operational Base + offset (0x00c0)

Bit	Attr	Reset Value	Description
31:18	RO	0x0	reserved
17	RW	0x0	dbi_ilegal_comm_err This bit indicates that an attempt to write an illegal command on the DBI interface is made and the core is blocked by transmission
16	RO	0x0	dbi_pld_recv_err This bit indicates that during a DBI read back packet, the payload FIFO becomes full and the received data is corrupted
15	RO	0x0	dbi_pld_rd_err This bit indicates that during a DCS read data, the payload FIFO goes empty and the data sent to the interface is corrupted
14	RO	0x0	dbi_pld_wr_err This bit indicates that the system tried to write the payload data through the DBI interface and the FIFO is full. Therefore, the command is not written
13	RO	0x0	dbi_cmd_wr_err This bit indicates that the system tried to write a command through the DBI but the command FIFO is full. Therefore, the command is not written
12	RO	0x0	gen_pld_recev_err This bit indicates that during a generic interface packet read back, the payload FIFO becomes full and the received data is corrupted
11	RO	0x0	gen_pld_rd_err This bit indicates that during a DCS read data, the payload FIFO becomes empty and the data sent to the interface is corrupted

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Bit	Attr	Reset Value	Description
10	RO	0x0	gen_pld_send_err This bit indicates that during a Generic interface packet build, the payload FIFO becomes empty and corrupt data is sent
9	RO	0x0	gen_pld_wr_err This bit indicates that the system tried to write a payload data through the Generic interface and the FIFO is full. Therefore, the payload is not written
8	RO	0x0	gen_cmd_wr_err This bit indicates that the system tried to write a command through the Generic interface and the FIFO is full. Therefore, the command is not written
7	RO	0x0	dpi_pld_wr_err This bit indicates that during a DPI pixel line storage, the payload FIFO becomes full and the data stored is corrupted
6	RO	0x0	eopt_err This bit indicates that the EoTp packet is not received at the end of the incoming peripheral transmission
5	RO	0x0	pkt_size_err This bit indicates that the packet size error is detected during the packet reception
4	RO	0x0	crc_err This bit indicates that the CRC error is detected in the received packet payload
3	RO	0x0	ecc_multi_err This bit indicates that the ECC multiple error is detected in a received packet
2	RO	0x0	ecc_single_err This bit indicates that the ECC single error is detected and corrected in a received packet

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Bit	Attr	Reset Value	Description
1	RO	0x0	to_lp_rx This bit indicates that the low-power reception timeout counter reached the end and contention is detected
0	RO	0x0	to_hs_tx This bit indicates that the high-speed transmission timeout counter reached the end and contention is detected

MIPI_DSI_HOST_INT_MSK0

Address: Operational Base + offset (0x00c4)

Bit	Attr	Reset Value	Description
31:21	RO	0x0	reserved
20	RW	0x0	dphy_errors_4 This bit indicates the LP1 contention error ErrContentionLP1 from Lane 0
19	RW	0x0	dphy_errors_3 This bit indicates the LP0 contention error ErrContentionLP0 from Lane 0
18	RW	0x0	dphy_errors_2 This bit indicates the ErrControl error from Lane 0
17	RW	0x0	dphy_errors_1 This bit indicates ErrSyncEsc low-power data transmission synchronization error from Lane 0
16	RW	0x0	dphy_errors_0 This bit indicates ErrEsc escape entry error from Lane 0
15	RW	0x0	ack_with_err_15 This bit retrieves the DSI protocol violation from the Acknowledge error report
14	RW	0x0	ack_with_err_14 This bit retrieves the reserved (specific to device) from the Acknowledge error report

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Bit	Attr	Reset Value	Description
13	RW	0x0	ack_with_err_13 This bit retrieves the invalid transmission length from the Acknowledge error report
12	RW	0x0	ack_with_err_12 This bit retrieves the DSI VC ID Invalid from the Acknowledge error report
11	RW	0x0	ack_with_err_11 This bit retrieves the not recognized DSI data type from the Acknowledge error report
10	RW	0x0	ack_with_err_10 This bit retrieves the checksum error (long packet only) from the Acknowledge error report
9	RW	0x0	ack_with_err_9 This bit retrieves the ECC error, multi-bit (detected, not corrected) from the Acknowledge error
8	RW	0x0	ack_with_err_8 This bit retrieves the ECC error, single-bit (detected and corrected) from the Acknowledge error
7	RW	0x0	ack_with_err_7 This bit retrieves the reserved (specific to device) from the Acknowledge error report
6	RW	0x0	ack_with_err_6 This bit retrieves the False Control error from the Acknowledge error report
5	RW	0x0	ack_with_err_5 This bit retrieves the Peripheral Timeout error from the Acknowledge Error report
4	RW	0x0	ack_with_err_4 This bit retrieves the LP Transmit Sync error from the Acknowledge error report

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Bit	Attr	Reset Value	Description
3	RW	0x0	ack_with_err_3 This bit retrieves the Escape Mode Entry Command error from the Acknowledge error report
2	RW	0x0	ack_with_err_2 This bit retrieves the EoT Sync error from the Acknowledge error report
1	RW	0x0	ack_with_err_1 This bit retrieves the SoT Sync error from the Acknowledge error report
0	RW	0x0	ack_with_err_0 This bit retrieves the SoT error from the Acknowledge error report

MIPI_DSI_HOST_INT_MSK1

Address: Operational Base + offset (0x00c8)

Bit	Attr	Reset Value	Description
31:18	RO	0x0	reserved
17	RW	0x0	dbi_ilegal_comm_err This bit indicates that an attempt to write an illegal command on the DBI interface is made and the core is blocked by transmission
16	RW	0x0	dbi_pld_recv_err This bit indicates that during a DBI read back packet, the payload FIFO becomes full and the received data is corrupted
15	RW	0x0	dbi_pld_rd_err This bit indicates that during a DCS read data, the payload FIFO goes empty and the data sent to the interface is corrupted
14	RW	0x0	dbi_pld_wr_err This bit indicates that the system tried to write the payload data through the DBI interface and the FIFO is full. Therefore, the command is not written

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Bit	Attr	Reset Value	Description
13	RW	0x0	dbi_cmd_wr_err This bit indicates that the system tried to write a command through the DBI but the command FIFO is full. Therefore, the command is not written
12	RW	0x0	gen_pld_recev_err This bit indicates that during a generic interface packet read back, the payload FIFO becomes full and the received data is corrupted
11	RW	0x0	gen_pld_rd_err This bit indicates that during a DCS read data, the payload FIFO becomes empty and the data sent to the interface is corrupted
10	RW	0x0	gen_pld_send_err This bit indicates that during a Generic interface packet build, the payload FIFO becomes empty and corrupt data is sent
9	RW	0x0	gen_pld_wr_err This bit indicates that the system tried to write a payload data through the Generic interface and the FIFO is full. Therefore, the payload is not written
8	RW	0x0	gen_cmd_wr_err This bit indicates that the system tried to write a command through the Generic interface and the FIFO is full. Therefore, the command is not written
7	RW	0x0	dpi_pld_wr_err This bit indicates that during a DPI pixel line storage, the payload FIFO becomes full and the data stored is corrupted
6	RW	0x0	eopt_err This bit indicates that the EoTp packet is not received at the end of the incoming peripheral transmission
5	RW	0x0	pkt_size_err This bit indicates that the packet size error is detected during the packet reception

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Bit	Attr	Reset Value	Description
4	RW	0x0	crc_err This bit indicates that the CRC error is detected in the received packet payload
3	RW	0x0	ecc_multi_err This bit indicates that the ECC multiple error is detected in a received packet
2	RW	0x0	ecc_single_err This bit indicates that the ECC single error is detected and corrected in a received packet
1	RW	0x0	to_lp_rx This bit indicates that the low-power reception timeout counter reached the end and contention is detected
0	RW	0x0	to_hs_tx This bit indicates that the high-speed transmission timeout counter reached the end and contention is detected

MIPI_DSI_HOST_INT_FORCE0

Address: Operational Base + offset (0x00d8)

Bit	Attr	Reset Value	Description
31:21	RO	0x0	reserved
20	RW	0x0	dphy_errors_4 This bit indicates the LP1 contention error ErrContentionLP1 from Lane 0
19	RW	0x0	dphy_errors_3 This bit indicates the LP0 contention error ErrContentionLP0 from Lane 0
18	RW	0x0	dphy_errors_2 This bit indicates the ErrControl error from Lane 0

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Bit	Attr	Reset Value	Description
17	RW	0x0	dphy_errors_1 This bit indicates ErrSyncEsc low-power data transmission synchronization error from Lane 0
16	RW	0x0	dphy_errors_0 This bit indicates ErrEsc escape entry error from Lane 0
15	RW	0x0	ack_with_err_15 This bit retrieves the DSI protocol violation from the Acknowledge error report
14	RW	0x0	ack_with_err_14 This bit retrieves the reserved (specific to device) from the Acknowledge error report
13	RW	0x0	ack_with_err_13 This bit retrieves the invalid transmission length from the Acknowledge error report
12	RW	0x0	ack_with_err_12 This bit retrieves the DSI VC ID Invalid from the Acknowledge error report
11	RW	0x0	ack_with_err_11 This bit retrieves the not recognized DSI data type from the Acknowledge error report
10	RW	0x0	ack_with_err_10 This bit retrieves the checksum error (long packet only) from the Acknowledge error report
9	RW	0x0	ack_with_err_9 This bit retrieves the ECC error, multi-bit (detected, not corrected) from the Acknowledge error
8	RW	0x0	ack_with_err_8 This bit retrieves the ECC error, single-bit (detected and corrected) from the Acknowledge error

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Bit	Attr	Reset Value	Description
7	RW	0x0	ack_with_err_7 This bit retrieves the reserved (specific to device) from the Acknowledge error report
6	RW	0x0	ack_with_err_6 This bit retrieves the False Control error from the Acknowledge error report
5	RW	0x0	ack_with_err_5 This bit retrieves the Peripheral Timeout error from the Acknowledge Error report
4	RW	0x0	ack_with_err_4 This bit retrieves the LP Transmit Sync error from the Acknowledge error report
3	RW	0x0	ack_with_err_3 This bit retrieves the Escape Mode Entry Command error from the Acknowledge error report
2	RW	0x0	ack_with_err_2 This bit retrieves the EoT Sync error from the Acknowledge error report
1	RW	0x0	ack_with_err_1 This bit retrieves the SoT Sync error from the Acknowledge error report
0	RW	0x0	ack_with_err_0 This bit retrieves the SoT error from the Acknowledge error report

MIPI_DSI_HOST_INT_FORCE1

Address: Operational Base + offset (0x00dc)

Bit	Attr	Reset Value	Description
31:18	RO	0x0	reserved

Bit	Attr	Reset Value	Description
17	RW	0x0	dbi_ilegal_comm_err This bit indicates that an attempt to write an illegal command on the DBI interface is made and the core is blocked by transmission
16	RW	0x0	dbi_pld_recv_err This bit indicates that during a DBI read back packet, the payload FIFO becomes full and the received data is corrupted
15	RW	0x0	dbi_pld_rd_err This bit indicates that during a DCS read data, the payload FIFO goes empty and the data sent to the interface is corrupted
14	RW	0x0	dbi_pld_wr_err This bit indicates that the system tried to write the payload data through the DBI interface and the FIFO is full. Therefore, the command is not written
13	RW	0x0	dbi_cmd_wr_err This bit indicates that the system tried to write a command through the DBI but the command FIFO is full. Therefore, the command is not written
12	RW	0x0	gen_pld_recev_err This bit indicates that during a generic interface packet read back, the payload FIFO becomes full and the received data is corrupted
11	RW	0x0	gen_pld_rd_err This bit indicates that during a DCS read data, the payload FIFO becomes empty and the data sent to the interface is corrupted
10	RW	0x0	gen_pld_send_err This bit indicates that during a Generic interface packet build, the payload FIFO becomes empty and corrupt data is sent
9	RW	0x0	gen_pld_wr_err This bit indicates that the system tried to write a payload data through the Generic interface and the FIFO is full. Therefore, the payload is not written

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Bit	Attr	Reset Value	Description
8	RW	0x0	gen_cmd_wr_err This bit indicates that the system tried to write a command through the Generic interface and the FIFO is full. Therefore, the command is not written
7	RW	0x0	dpi_pld_wr_err This bit indicates that during a DPI pixel line storage, the payload FIFO becomes full and the data stored is corrupted
6	RW	0x0	eopt_err This bit indicates that the EoTp packet is not received at the end of the incoming peripheral transmission
5	RW	0x0	pkt_size_err This bit indicates that the packet size error is detected during the packet reception
4	RW	0x0	crc_err This bit indicates that the CRC error is detected in the received packet payload
3	RW	0x0	ecc_multi_err This bit indicates that the ECC multiple error is detected in a received packet
2	RW	0x0	ecc_single_err This bit indicates that the ECC single error is detected and corrected in a received packet
1	RW	0x0	to_lp_rx This bit indicates that the low-power reception timeout counter reached the end and contention is detected
0	RW	0x0	to_hs_tx This bit indicates that the high-speed transmission timeout counter reached the end and contention is detected

MIPI_DSI_HOST_VID_SHADOW_CTRL

Address: Operational Base + offset (0x0100)

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Bit	Attr	Reset Value	Description
31:17	RO	0x0	reserved
16	RW	0x0	vid_shadow_pin_req When set to 1, the video request is done by external pin. In this mode, vid_shadow_req is ignored
15:9	RO	0x0	reserved
8	RW	0x0	vid_shadow_req When set to 1, the DPI registers are copied to the auxiliary registers. After copying, this bit is auto cleared
7:1	RO	0x0	reserved
0	RW	0x0	vid_shadow_en When set to 1, DPI receives the active configuration from the auxiliary registers. When this bit is set along with the vid_shadow_req bit, the auxiliary registers are automatically updated

MIPI_DSI_HOST_DPI_VCID_ACT

Address: Operational Base + offset (0x010c)

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1:0	RW	0x0	dpi_vcid This field configures the DPI virtual channel id that is indexed to the Video mode packets

MIPI_DSI_HOST_DPI_COLOR_CODING_ACT

Address: Operational Base + offset (0x0110)

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Bit	Attr	Reset Value	Description
31:9	RO	0x0	reserved
8	RW	0x0	loosely18_en When set to 1, this bit activates loosely packed variant to 18-bit configurations
7:4	RO	0x0	reserved
3:0	RW	0x0	dpi_color_coding This field configures the DPI color coding as follows: 0000: 16-bit configuration 1 0001: 16-bit configuration 2 0010: 16-bit configuration 3 0011: 18-bit configuration 1 0100: 18-bit configuration 2 0101: 24-bit 0110: 20-bit YCbCr 4:2:2 loosely packed 0111: 24-bit YCbCr 4:2:2 1000: 16-bit YCbCr 4:2:2 1001: 30-bit 1010: 36-bit 1011-1111: 12-bit YCbCr 4:2:0

MIPI_DSI_HOST_DPI_LP_CMD_TIM_ACT

Address: Operational Base + offset (0x0118)

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:16	RO	0x00	outvact_lpcmd_time This field is used for the transmission of commands in low-power mode. It defines the size, in bytes, of the largest packet that can fit in a line during the VSA, VBP, and VFP regions
15:8	RO	0x0	reserved

Bit	Attr	Reset Value	Description
7:0	RO	0x00	invact_lpcmd_time This field is used for the transmission of commands in low-power mode. It defines the size, in bytes, of the largest packet that can fit in a line during the VACT region

MIPI_DSI_HOST_VID_MODE_CFG_ACT

Address: Operational Base + offset (0x0138)

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24	RW	0x0	vpg_orientation This field indicates the color bar orientation as follows: 0: Vertical mode 1: Horizontal mode
23:21	RO	0x0	reserved
20	RO	0x0	vpg_mode This field is to select the pattern: 0: Color bar (horizontal or vertical) 1: BER pattern (vertical only)
19:17	RO	0x0	reserved
16	RO	0x0	vpg_en When set to 1, this bit enables the video mode pattern generator
15	RO	0x0	lp_cmd_en When set to 1, this bit enables the command transmission only in lowpower mode
14	RO	0x0	frame_bta_ack_en When set to 1, this bit enables the request for an acknowledge response at the end of a frame

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Bit	Attr	Reset Value	Description
13	RO	0x0	lp_hfp_en When set to 1, this bit enables the return to low-power inside the Horizontal Front Porch (HFP) period when timing allows
12	RO	0x0	lp_hbp_en When set to 1, this bit enables the return to low-power inside the Horizontal Back Porch (HBP) period when timing allows
11	RO	0x0	lp_vact_en When set to 1, this bit enables the return to low-power inside the Vertical Active (VACT) period when timing allows
10	RO	0x0	lp_vfp_en When set to 1, this bit enables the return to low-power inside the Vertical Front Porch (VFP) period when timing allows
9	RO	0x0	lp_vbp_en When set to 1, this bit enables the return to low-power inside the Vertical Back Porch (VBP) period when timing allows
8	RO	0x0	lp_vsa_en When set to 1, this bit enables the return to low-power inside the Vertical Sync Time (VSA) period when timing allows
7:2	RO	0x0	reserved
1:0	RO	0x0	vid_mode_type This field indicates the video mode transmission type as follows: 2'b00: Non-burst with sync pulses 2'b01: Non-burst with sync events 2'b10 and 2'b11: Burst mode

MIPI_DSI_HOST_VID_PKT_SIZE_ACT
Address: Operational Base + offset (0x013c)

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Bit	Attr	Reset Value	Description
31:14	RO	0x0	reserved
13:0	RO	0x0000	vid_pkt_size This field configures the number of pixels in a single video packet. For 18-bit not loosely packed data types, this number must be a multiple of 4. For YCbCr data types, it must be a multiple of 2, as described in the DSI specification

MIPI_DSI_HOST_VID_NUM_CHUNKS_ACT

Address: Operational Base + offset (0x0140)

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12:0	RO	0x0000	vid_num_chunks This register configures the number of chunks to be transmitted during a Line period (a chunk consists of a video packet and a null packet). If set to 0 or 1, the video line is transmitted in a single packet. If set to 1, the packet is part of a chunk, so a null packet follows it if vid_null_size > 0. Otherwise, multiple chunks are used to transmit each video line

MIPI_DSI_HOST_VID_NULL_SIZE_ACT

Address: Operational Base + offset (0x0144)

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12:0	RW	0x0000	vid_null_size This register configures the number of bytes inside a null packet. Setting it to 0 disables the null packets

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MIPI_DSI_HOST_VID_HSA_TIME_ACT

Address: Operational Base + offset (0x0148)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RO	0x000	vid_hsa_time This field configures the Horizontal Synchronism Active period in lane byte clock cycles

MIPI_DSI_HOST_VID_HBP_TIME_ACT

Address: Operational Base + offset (0x014c)

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0x000	vid_hsa_time This field configures the Horizontal Synchronism Active period in lane byte clock cycles

MIPI_DSI_HOST_VID_HLINE_TIME_ACT

Address: Operational Base + offset (0x0150)

Bit	Attr	Reset Value	Description
31:15	RO	0x0	reserved
14:0	RO	0x0000	vid_hline_time This field configures the size of the total line time (HSA+HBP+HACT+HFP) counted in lane byte clock cycles

MIPI_DSI_HOST_VID_VSA_LINES_ACT

Address: Operational Base + offset (0x0154)

Bit	Attr	Reset Value	Description
31:10	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
9:0	RO	0x000	vsa_lines This field configures the Vertical Synchronism Active period measured in number of horizontal lines

MIPI_DSI_HOST_VID_VBP_LINES_ACT
Address: Operational Base + offset (0x0158)

Bit	Attr	Reset Value	Description
31:10	RO	0x0	reserved
9:0	RW	0x000	vbp_lines This field configures the Vertical Back Porch period measured in number of horizontal lines

MIPI_DSI_HOST_VID_VFP_LINES_ACT
Address: Operational Base + offset (0x015c)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RO	0x0	vfp_lines This field configures the Vertical Front Porch period measured in number of horizontal lines

MIPI_DSI_HOST_VID_VACTIVE_LINES_ACT
Address: Operational Base + offset (0x0160)

Bit	Attr	Reset Value	Description
31:14	RO	0x0	reserved
13:0	RO	0x0000	v_active_lines This field configures the Vertical Active period measured in number of horizontal lines

MIPI_DSI_HOST_SDF_3D_ACT
Address: Operational Base + offset (0x0190)

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Bit	Attr	Reset Value	Description
31:17	RO	0x0	reserved
16	RW	0x0	send_3d_cfg When set, causes the next VSS packet to include 3D control payload in every VSS packet
15:6	RO	0x0	reserved
5	RO	0x0	right_first This bit defines the left or right order: 1'b0: Left eye data is sent first, and then the right eye data is sent. 1'b1: Right eye data is sent first, and then the left eye data is sent
4	RO	0x0	second_vsync This field defines whether there is a second VSYNC pulse between Left and Right Images, when 3D Image Format is Frame-based: 1'b0: No sync pulses between left and right data 1'b1: Sync pulse (HSYNC, VSYNC, blanking) between left and right data
3:2	RO	0x0	format_3d This field defines the 3D image format: 2'b00: Line (alternating lines of left and right data) 2'b01: Frame (alternating frames of left and right data) 2'b10: Pixel (alternating pixels of left and right data) 2'b11: Reserved

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Bit	Attr	Reset Value	Description
1:0	RO	0x0	mode_3d This field defines the 3D mode on/off and display orientation: 2'b00: 3D mode off (2D mode on) 2'b01: 3D mode on, portrait orientation 2'b10: 3D mode on, landscape orientation 2'b11: Reserved

12.5 Application Notes

12.5.1 COMMON CONFIGURATION (DEFAULT IN MIPI MODE)

Step1: Enable reference clock.

Step2: Wait a period after reference clock have been enabled.

Step3: Send 0xe4 to register MIPI_DSI_DPHY_CTRL_PWRCTL. Enable PLL and LDO.

Step4: Send 0x7d to register MIPI_DSI_DPHY_CTRL_LANE_ENABLE. Enable all lanes on analog part.

Step5: Send 0xe0 to register MIPI_DSI_DPHY_CTRL_PWRCTL. Reset analog.

Step6: Wait a period after analog has been reset.

Step7: Send 0x1e to register MIPI_DSI_DPHY_CTRL_DIG_RST. Reset digital.

Step8: Send 0x1f to register MIPI_DSI_DPHY_CTRL_DIG_RST. Reset digital.

Step9: Wait a period until pll locked. Run in MIPI mode.

12.5.2 LOW POWER MODE (FOR DSI ONLY)

Low Power Mode is a special feature for D-PHY. You can control this function by using proper registers from the D-PHY with few operations. The following is a step by step instruction for low power mode in and out.

Perform the following steps to configure the DPI packet transmission:

Step1:Global configuration:

Configure n_lanes (PHY_IF_CFG-[1:0]) to define the number of lanes in which the controller has to perform high-speed transmissions.

Step2:Configure the DPI Interface to define how the DPI interface interacts with the controller.

Configure dpi_vid (DPI_CFG-[1:0]): This field configures the virtual channel that the packet generated by the DPI interface is indexed to.

Configure dpi_color_coding (DPI_CFG-[4:2]): This field configures the bits per pixels that the interface transmits and also the variant configuration of each bpp. If you select 18 bpp, and the Enable_18_loosely_packed is not active, the number or pixels per line should be a multiple of four.

Configure dataen_active_low (DPI_CFG-[5]): This bit configures the polarity of the

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dpidataen signal and enables if it is active low.

Configure vsync_active_low(DPI_CFG-[6]): This bit configures the polarity of the dpivsync signal and enables if it is active low.

Configure vsync_active_low(DPI_CFG-[7]): This bit configures the polarity of the dpivsync signal and enables if it is active low.

Configure vsync_active_low(DPI_CFG-[8]): This bit configures the polarity of the dpishutdn signal and enables if it is active low.

Configure vsync_active_low(DPI_CFG-[9]): This bit configures the polarity of the dpicolorm signal and enables if it is active low.

Configure en18_loosely(DPI_CFG-[10]): This bit configures if the pixel packing is done loosely or packed when dpi_color_coding is 18 bpp. This bit enables loosely packing.

Step3: Select the Video Transmission Mode to define how the processor requires the video line to be transported through the DSI link.

Configure low-power transitions (VID_MODE_CFG-[8:3]): This defines the video line to be transported through the DSI link.

Configure low-power transitions (VID_MODE_CFG-[8:3]): This defines the video periods which are permitted to go to low-power if there is available time to do so.

Configure frame_BTA_ack (VID_MODE_CFG-[11]): This specifies if the controller should request the peripheral acknowledge message at the end of frames.

Burst mode: In this mode, the entire active pixel line is buffered into a FIFO and transmitted in a single packed with no interruptions. This transmission mode requires that the DPI Pixel FIFO has the capacity to store a full line of active pixel data inside it. This mode is optimally used if the difference between pixel required bandwidth and DSI link bandwidth is very different. This enables the DWC_mipi_dsi_host to quickly dispatch the entire active video line in a single burst of data and then return to low-power mode.

Configure the register fiedl vid_mode_type (VID_MODE_CFG-[10]), num_chunks (VID_PKT_CFG-[20:11]), and null_pkt_size (VID_PKT_CFG-[30:21]) are automatically ignored by the DWC_mipi_dsi_host.

Non-Burst mode: In this mode, the processor uses the partitioning properties of the DWC_mipi_dsi_host to divide the video line transmission into several DSI packets. This is done to match th pixel required bandwidth with the DSI link bandwidth. With this mode, the controller configuration dose not require a full line of pixel data to be stored inside the DPI Pixel FIFO. It requires only the content of one video packet.

Configure the vid_mode_type field (VID_MODE_CFG-[2:1]) with 2’b0x.

Configure the vid_mode_type field (VID_MODE_CFG-[2:1]) with 2’b00x to enable the transmission of sync pulses.

Configure the vid_mode_type field (VID_MODE_CFG-[2:1]) with 2’b01to enable the transmission of sync events.

Configure the vid_mode_type field (VID_MODE_CFG-[10:0]) with the number of pixels to be transmitted in a single packet.

Configure the en_multi_pkt field (VID_MODE_CFG-[9]) to enable the division of the active video transmission into more than one packet.

Configure the num_chunks field (VID_MODE_CFG-[20:11]) with the number of video chunks that the active video transmission is divided into.

Configure the en_null_pkt field (VID_MODE_CFG-[10]) to enable the insertion of null

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packets between video packets.

The field is effective only when en_multi_pkt field is activated, otherwise the controller ignores it and does not sent the null packets.

Configure the null_pkt_size field (VID_MODE_CFG-[30:21]) with the actual size of the inserted null packet.

Step4:Define the DPI Horizontal timing configuration as follows:

Configure the hline_time field (TMR_LINE_CFG-[31:18]) with the time taken by a DPI video line accounted in Clock Lane bytes clock cycles (for a clock lane at 500 MHz the Lane byte clock period is 8 ns). When the DPI clock and Clock Lane clock are not multiples, the hline_time is a result of a round of a number. If the DWC_mipi_dsi_host is configured to go to low-power, it is possible that the error included in a line is incremented with the next one. At the end of several lines, the DWC_mipi_dsi_host can have a number of errors that can cause a malfunction of the video transmission.

Configure the hsa_time field (TMR_LINE_CFG-[8:0]) with the time taken by a DPI Horizontal Sync Active period accounted in Clock Lane byte clock cycles (normally a period of 8ns).

Configure the hbp_time field (TMR_LINE_CFG-[17:9]) with the time taken by a DPI Horizontal Sync Active period accounted in Clock Lane byte clock cycles (normally a period of 8ns). Special attention should be given to the calculation of this parameter.

Step5:Define the Vertical line configuration:

Configure the vsa_lines field (VTIMING_CFG-[3:0]) with the number of lines existing in the DPI Vertical Sync Active period.

Configure the vbp_lines field (VTIMING_CFG-[9:4]) with the number of lines existing in the DPI Vertical Back Porch period.

Configure the vfp_lines field (VTIMING_CFG-[15:10]) with the number of lines existing in the DPI Vertical Front Porch period.

Configure the v_active_lines field (VTIMING_CFG-[26:16]) with the number of lines existing in the DPI Vertical Active period.

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Chapter 13 MIPI DSI D-PHY

13.1 Overview

The MIPI D-PHY integrates a MIPI® V1.0 compatible PHY that supports up to 1.0Gbps high speed data receiver, plus a MIPI® low-power low speed transceiver that supports data transfer in the bi-directional mode. The IP supports the full specifications described in V1.0 of the D-PHY spec. The D-PHY is built in with a standard digital interface to talk to any third party Host controller. The architecture supports connection of multiple data lanes in parallel – up to 4 data lanes can be connected to increase the total through-put, customizable to user determined configurations. The I/O and ESD are also built-in as one in a rectangular footprint for any configuration (one lane to 4 lanes or more). It is optimized for high speed applications with robust timing and small silicon area. The D-PHY supports the electrical portion of MIPI D-PHY V1.0 standard, covering all transmission modes (ULP/LP/HS).The MIPI D-PHY cost-effectively adds MIPI D-PHY V1.0 capability to any SOC used in communication and consumer electronics field.

The MIPI D-PHY supports the following features:

- Mixed-signal D-PHY mixed-signal hard-macro- HS/LS Transmitter and LS/HS Receiver solution
- Designed to MIPI® v1.0 Specifications
- Integrated PHY Protocol Interface (PPI) supports interface to CSI, DSI and UniPro™
- MIPI® protocols
- 1.0Gbps maximum data transfer rate per lane
- Expandable to support 4 data lanes, providing up to 4.0Gbps transfer rate
- MIPI-HS, MIPI-LP , LVDS, TTL modes supported
- 10Mbps per lane in low-power mode
- Unidirectional and bi-directional modes supported
- Automatic termination control for HS and LP modes
- Low-Power dissipation: less than 3mA/Lane in HS TX/RX mode
- Tx/Rx Buffers with tunable On-Die-Termination and advanced equalization.
- Embedded ESD, boundary scan support logic.

13.2 Block Diagram

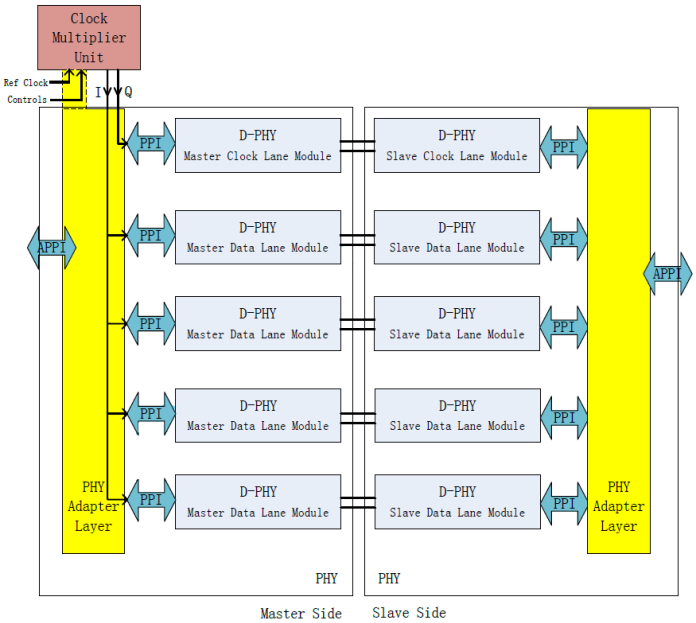


Fig. 13-1 MIPI DSI D-PHY detailed block diagram

MIPI D-PHY configuration contains one Clock Lane Module and four Data Lane Modules. Each

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of these PHY Lane Modules communicates via two Lines to a complementary part at the other side of the Lane Interconnect. Figure 1 shows the DPHY architecture.

13.3 Function Description

13.3.1 System Connection

The MIPI DSI DPHY supports MIPI/LVDS/TTL mode. VOP outputs data use different ports for MIPI and LVDS mode. The connection with VOP of three mode shows in following figure:

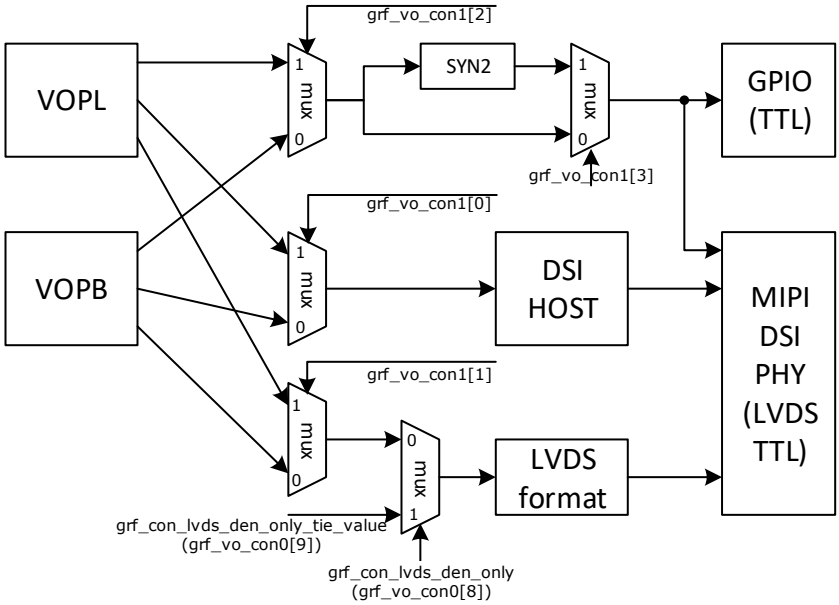


Fig. 13-2 MIPI DSI D-PHY and VOP connection

Note: The other selects and detail information of TTL signals is illustrated in chapter configuration for TTL MODE.

13.3.2 MIPI MODE

In MIPI mode, there are some functions of DPHY controlled by grf registers. These register bit and function is show in following table:

Table 13-1 function of grf bits in MIPI mode

register bit	function
grf_con_dsi_phy_lane0_frctxstpm	Force Lane Module Into Transmit mode / Generate Stop state. This signal allows the protocol to force a Lane Module into transmit mode and Stop state during initialization.
grf_con_dsi_phy_lane1_frctxstpm	Force Lane Module Into Transmit mode / Generate Stop state. This signal allows the protocol to force a Lane Module into transmit mode and Stop state during initialization.
grf_con_dsi_phy_lane2_frctxstpm	Force Lane Module Into Transmit mode / Generate Stop state. This signal allows the protocol to force a Lane Module into transmit mode and Stop state during initialization.
grf_con_dsi_phy_lane3_frctxstpm	Force Lane Module Into Transmit mode / Generate Stop state. This signal allows the protocol to force a Lane Module into transmit mode and Stop state during initialization.
grf_con_dsi_phy_lane0_turndisable	Disable Turn-around. This signal is used

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register bit	function
	to prevent a (bi-directional) Lane from going into transmit mode – even if it observes a turn-around request on the Lane interconnect.
grf_con_dsi_phy_forcerxmode	Force Lane Module Into Receive mode / Wait for Stop state. This signal allows the protocol to initialize a Lane Module, or force a bi-directional Lane Module, into receive mode.

13.3.3 Program PLL in MIPI mode

Frequency Calculating Formula
The PLL output frequency can be calculated using a simple formula:
PLL_Output_Frequency = (FREF/PREDIV*FBDIV)/2
PLL_Output_Frequency: It is equal to DDR_Clock_Frequency * 2
FREF: 24 Mhz
PREDIV: PLL input reference clock divider which can be configured by the register of prediv
FBDIV: Integer value programmed into feedback divider which can be configured by the register of fbdiv
Additional Programming Considerations
1. The divided reference frequency (FREF/PREDIV) should be less than 40MHz.
2. The all possible settings of feedback divider are 12, 13, 14, 16~511.

13.3.4 LVDS MODE

After video data is sent from VOP, it first goes into lvds_format block. Lvds_format block first maps video data to 4 types as show in 错误!未找到引用源。. This function is controlled by register grf_con_lvds_select[1:0]. After video data map, you can use grf_con_lvds_msbsel to revert data bits into MSB.

Table 13-2 LVDS map setting

grf_con_lvds_select	LVDS map when (grf_con_lvds_msbsel == 0) lvds_lane1 use IO_MIPI_DSI_DATAN0 and IO_MIPI_DSI_DATAP0 lvds_lane2 use IO_MIPI_DSI_DATAN1 and IO_MIPI_DSI_DATAP1 lvds_lane3 use IO_MIPI_DSI_DATAN2 and IO_MIPI_DSI_DATAP2 lvds_lane4 use IO_MIPI_DSI_DATAN3 and IO_MIPI_DSI_DATAP3	
0	lvds_lane1	{g_data[0],r_data[5:0]}
	lvds_lane2	{b_data[1:0],g_data[5:1]}
	lvds_lane3	{lcdc_den,lcdc_vsyncn,lcdc_hsyncn,b_data[5:2]}
	lvds_lane4	{1'b0,b_data[7:6],g_data[7:6],r_data[7:6]}
1	lvds_lane1	{g_data[2],r_data[7:2]}
	lvds_lane2	{b_data[3:2],g_data[7:3]}
	lvds_lane3	{lcdc_den,lcdc_vsyncn,lcdc_hsyncn,b_data[7:4]}
	lvds_lane4	{1'b0,b_data[1:0],g_data[1:0],r_data[1:0]}
2	lvds_lane1	{g_data[2],r_data[7:2]}
	lvds_lane2	{b_data[3:2],g_data[7:3]}
	lvds_lane3	{lcdc_den,lcdc_vsyncn,lcdc_hsyncn,b_data[7:4]}
	lvds_lane4	7'b0
3	lvds_lane1	{g_data[0],r_data[5:0]}
	lvds_lane2	{b_data[1:0],g_data[5:1]}
	lvds_lane3	{lcdc_den,lcdc_vsyncn,lcdc_hsyncn,b_data[5:2]}
	lvds_lane4	7'b0

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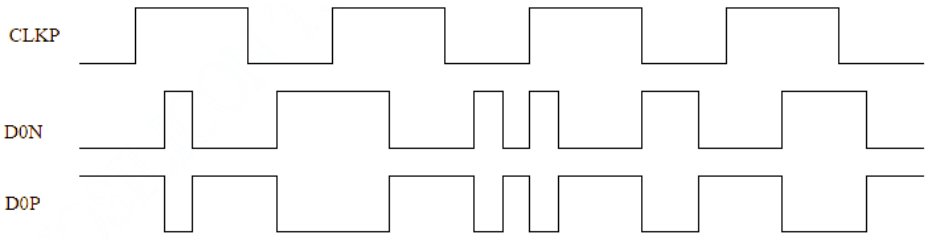


Fig. 13-3 LVDS mode clock timing

, When setting grf_con_lvds_msbsel to 0, the output serial data is transmitted as shown in figure bellow. The rising edge of the output clock is at the transition of bit2 and bit1 of the video_data(r_data,g_data,b_data).

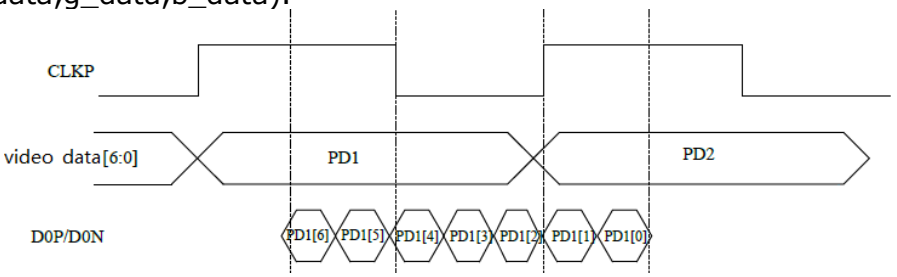


Fig. 13-4 LVDS mode lsb parallel data to serial data timing

13.3.5 TTL MODE

The TTL mapping of digital signals to analog pads is shown below.

Table 13-3 TTL mapping of digital signals to analog pads

Digital Signal	Analog PADS
lcdc_d8m1	DATAP0
lcdc_d11m1	DATAN0
lcdc_d10m1	DATAP1
lcdc_d1m1	DATAN1
lcdc_d5m1	DATAP2
lcdc_vsyncm1	DATAN2
lcdc_denm1	DATAP3
lcdc_hsyncm1	DATAP3
lcdc_d3m1	CLKP
lcdc_d4m1	CLKN

13.4 Register Description

DSI PHY registers are accessed by APB BUS. This section describes the control/status registers of the design.

13.4.1 Register Summary

Name	Offset	Size	Reset Value	Description
MIPI_DSIPHY_CTRL_LANE_ENABLE	0x0000	W	0x00000001	lane enable
MIPI_DSIPHY_CTRL_PWR_CTL	0x0004	W	0x00000003	power control
MIPI_DSIPHY_CTRL_PREDIV	0x000c	W	0x00000003	PLL PREDIV
MIPI_DSIPHY_CTRL_FBDIV	0x0010	W	0x0000007d	PLL FBDIV
MIPI_DSIPHY_CTRL_DIG_RST	0x0080	W	0x000000ff	digital logic reset

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Name	Offset	Size	Reset Value	Description
MIPI_DSIPHY_CTRL_SIG_INV	0x0084	W	0x00000002	signal revert

*Notes: Size : **B** - Byte (8 bits) access, **HW** - Half WORD (16 bits) access, **W** -WORD (32 bits) access.*

Name	Offset	Size	Reset Value	Description
MIPI_DSIPHY_LVDSTTL_ctrl	0x0380	W	0x00000001	control bit
MIPI_DSIPHY_LVDSTTL_digital_en	0x0384	W	0x00000012	digital logic enable
MIPI_DSIPHY_LVDSTTL_mode_en	0x038c	W	0x00000001	model selection
MIPI_DSIPHY_LVDSTTL_lane_en	0x03ac	W	0x00000004	lane enable

*Notes: Size : **B** - Byte (8 bits) access, **HW** - Half WORD (16 bits) access, **W** -WORD (32 bits) access*

Following table shows registers for 5 lanes. They have same registers but use different address bases. So their final address is lane_base_address + offset.

lane	lane_base_address
clock_lane	0x100
Data0_lane	0x180
Data1_lane	0x200
Data2_lane	0x280
Data3_lane	0x300

Name	Offset	Size	Reset Value	Description
MIPI_DSIPHY_LANEX_Tlpx	0x0014	W	0x000000c5	Tlpx
MIPI_DSIPHY_LANEX_SHSTXTHSPRPR	0x0018	W	0x00000024	HSTXTHSPRPR
MIPI_DSIPHY_LANEX_SHSTXTHSZERO	0x001c	W	0x00000000	HSTXTHSZERO
MIPI_DSIPHY_LANEX_SHSTX	0x0020	W	0x00000027	HSTX
MIPI_DSIPHY_LANEX_Ths_exit	0x0024	W	0x0000000a	Ths_exit
MIPI_DSIPHY_LANEX_Tclk_post	0x0028	W	0x0000000f	Tclk_post
MIPI_DSIPHY_LANEX_LPDT_TX_PPI_SYN_EN	0x0030	W	0x00000000	LPDT_TX_PPI_SYN_EN
MIPI_DSIPHY_LANEX_Twakup	0x0034	W	0x00000000	Twakup
MIPI_DSIPHY_LANEX_Tclk_pre	0x0038	W	0x00000006	Tclk_pre
MIPI_DSIPHY_LANEX_Tta_go	0x0040	W	0x00000004	Tta_go

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Name	Offset	Size	Reset Value	Description
MIPI_DSIPHY_LANEX_Tta_sure	0x0044	W	0x00000001	Tta_sure
MIPI_DSIPHY_LANEX_Tta_wait	0x0048	W	0x00000032	Tta_wait

*Notes: Size : **B** - Byte (8 bits) access, **HW** - Half WORD (16 bits) access, **W** -WORD (32 bits) access*

13.4.2 MIPI DSIPHY CTRL Detail Register Description

MIPI_DSIPHY_CTRL_LANE_ENABLE

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:7	RO	0x0	reserved
6	RW	0x0	lane_en_ck lane clk enable
5	RW	0x0	lane_en_3 lane 3 enable
4	RW	0x0	lane_en_2 lane 2 enable
3	RW	0x0	lane_en_1 lane 1 enable
2	RW	0x0	lane_en_0 lane 0 enable
1:0	RO	0x0	reserved

MIPI_DSIPHY_CTRL_PWRCTL

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:3	RO	0x0	reserved
2	RW	0x0	SYNCRST analog reset
1	RW	0x1	LDO_PD ldo powerdown
0	RW	0x1	PLL_PD pll power down

MIPI_DSIPHY_CTRL_PREDIV

Address: Operational Base + offset (0x000c)

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5	RW	0x0	FBDIV_HI PREDIV
4:0	RW	0x03	PREDIV PREDIV

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MIPI_DSIPHY_CTRL_FBDIV

Address: Operational Base + offset (0x0010)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x7d	FBDIV_LO FBDIV_LO

MIPI_DSIPHY_CTRL_DIG_RST

Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x1	dig_rst digital logic reset

MIPI_DSIPHY_CTRL_SIG_INV

Address: Operational Base + offset (0x0084)

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x0	PIN_TXCLKESC_0_INV_EN inverting pin_txclkesc_0 enable
0	RW	0x0	PIN_TXBUTECLKHS_INV_EN inverting pin_txbyteclkhs enable

13.4.3 MIPI DSIPHY LANEx Detail Register Description

MIPI_DSIPHY_LANEX_Tlpx

Address: Operational Base + offset (0x0014)

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5:0	RW	0x00	Tlpx The value of counter for HS Tlpx Time （>=Tlpx） = Tpin_txbyteclkhs * (2+value)

MIPI_DSIPHY_LANEX_S_HSTXTHSPRPR

Address: Operational Base + offset (0x0018)

Bit	Attr	Reset Value	Description
31:7	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
6:0	RW	0x24	S_HSTXTHSPRPR The value of counter for HS Ths-prepare For clock lane, Ths-prepare(38ns~95ns) For data lane, Ths-prepare(40ns+4UI~85ns+6UI) For clock lane,S_HSTXTHSPRPR[6:0] = 7'b0100100 For data lane, S_HSTXTHSPRPR[6:0] = 7'b0100100 Frequency(1/UI) Value(HEX) 80-110MHz 20 110-150 MHz 06 150-200 MHz 18 200-250 MHz 05 250-300 MHz 51 300-400 MHz 64 400-500 MHz 59 500-600 MHz 6A 600-700 MHz 3E 700-800 MHz 21 800-1000 MHz 09

MIPI_DSIPHY_LANEX_S_HSTXTHSZERO

Address: Operational Base + offset (0x001c)

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved

Bit	Attr	Reset Value	Description
5:0	RW	0x00	S_HSTXTHSZERO For clock lane, Ths-prepare+Ths-zero (>=300ns) For data lane, Ths-prepare+Ths-zero (>= 145 ns + 10*UI) = Tpin_txbyteclkhs*(5+value) For clock lane, S_HSTXTHSZERO[5:0] = 6'b100000 Frequency(1/UI) Value(HEX) 80 -110 MHz 16 110-150 MHz 16 150-200 MHz 17 200-250 MHz 17 250-300 MHz 18 300-400 MHz 19 400-500 MHz 1B 500-600 MHz 1D 600-700 MHz 1E 700-800 MHz 1F 800-1000 MHz 20 For data lane,S_HSTXTHSZERO[5:0] = 6'b001001 Frequency(1/UI) Value(HEX) 80 -110 MHz 2 110-150 MHz 3 150-200 MHz 4 200-250 MHz 5 250-300 MHz 6 300-400 MHz 7 400-500 MHz 7 500-600 MHz 8 600-700 MHz 8 700-800 MHz 9 800-1000 MHz 9

MIPI_DSIPHY_LANEX_S_HSTX

Address: Operational Base + offset (0x0020)

Bit	Attr	Reset Value	Description
31:7	RO	0x0	reserved

Bit	Attr	Reset Value	Description
6:0	RW	0x27	S_HSTX The value of counter for HS Ths-trail For clock lane, Ths-trail (>=60ns) For data lane,Ths-trail (>=max(8UI, 60ns+4UI) For clock lane, S_HXTXTHSTRAIL[6:0] = 7'b0100111 For data lane, S_HXTXTHSTRAIL[6:0] = 7'b0100111 Frequency(1/UI) Value(HEX) 80 -110 MHz 22 110-150 MHz 45 150-200 MHz 0B 200-250 MHz 16 250-300 MHz 2C 300-400 MHz 33 400-500 MHz 4E 500-600 MHz 3A 600-700 MHz 6A 700-800 MHz 29 800-1000 MHz 27

MIPI_DSIPHY_LANEX_Ths_exit

Address: Operational Base + offset (0x0024)

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4:0	RW	0x0a	Ths_exit The value of counter for HS Ths-exit Ths-exit = Tpin_txbyteclkhs*value

MIPI_DSIPHY_LANEX_Tclk_post

Address: Operational Base + offset (0x0028)

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3:0	RW	0xf	Tclk_post The value of counter for HS Ths-exit Ths-exit = Tpin_txbyteclkhs*value

MIPI_DSIPHY_LANEX_LPDT_TX_PPI_SYN_EN

Address: Operational Base + offset (0x0030)

Bit	Attr	Reset Value	Description
31:3	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
2	RW	0x0	LPDT_TX_PPI_SYN_EN LPDT TX PPI signals internal synchronization enable. 1: enable 0: disable
1:0	RW	0x0	Twakup_H The value[9:8] of counter for HS Twakup

MIPI_DSIPHY_LANEX_Twakup

Address: Operational Base + offset (0x0034)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x00	Twakup The value[7:0] of counter for HS Twakup Twakup for ulpm, Twakup = Tpin_sys_clk*value[9:0]

MIPI_DSIPHY_LANEX_Tclk_pre

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3:0	RW	0x6	Tclk_pre Tclk_pre

MIPI_DSIPHY_LANEX_Tta_go

Address: Operational Base + offset (0x0040)

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5:0	RW	0x04	Tta_go The value of counter for HS Tta-go Tta-go for turnaround Tta-go = Ttxclkesc*value

MIPI_DSIPHY_LANEX_Tta_sure

Address: Operational Base + offset (0x0044)

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5:0	RW	0x01	Tta_sure The value of counter for HS Tta-sure Tta-sure for turnaround

MIPI_DSIPHY_LANEX_Tta_wait

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Address: Operational Base + offset (0x0048)

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5:0	RW	0x00	Tta_wait The value of counter for HS Tta-wait Tta-wait for turnaround Interval from receiving ppi turnaround request to sending esc request. Tta-wait = Ttxclkesc*value

13.4.4 MIPI DSIPHY LVDS/TTL Detail Register Description

MIPI_DSIPHY_LVDSTTL_ctrl

Address: Operational Base + offset (0x0380)

Bit	Attr	Reset Value	Description
31:3	RO	0x0	reserved
2	RW	0x0	digital_internal_reset digital logic reset
1	RO	0x0	reserved
0	RW	0x1	bit_order selection for MSB and LSB 1: MSB 0: LSB

MIPI_DSIPHY_LVDSTTL_digital_en

Address: Operational Base + offset (0x0384)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7	RW	0x0	digital_internal_en digital internal enable Active high. Default low
6:0	RO	0x0	reserved

MIPI_DSIPHY_LVDSTTL_mode_en

Address: Operational Base + offset (0x038c)

Bit	Attr	Reset Value	Description
31:3	RO	0x0	reserved
2	RW	0x0	ttl_mode_en TTL mode enable 1: enable TTL mode 0: disable TTL mode
1	RW	0x0	lvds_mode_en LVDS mode enable 1: enable LVDS mode 0: disable LVDS mode

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Bit	Attr	Reset Value	Description
0	RW	0x1	mipi_mode_en mipi mode enable 1: enable mipi mode 0: disable mipi mode

MIPI_DSIPHY_LVDSTTL_lane_en

Address: Operational Base + offset (0x03ac)

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7	RW	0x0	data_lane0_en Data Lane0 enable for LVDS mode 1: enable Data Lane0 1: disable Data Lane0
6	RW	0x0	data_lane1_en Data Lane1 enable for LVDS mode 1: enable Data Lane1 1: disable Data Lane1
5	RW	0x0	data_lane2_en Data Lane2 enable for LVDS mode 1: enable Data Lane2 1: disable Data Lane2
4	RW	0x0	data_lane3_en Data Lane3 enable for LVDS mode 1: enable Data Lane3 1: disable Data Lane3
3	RW	0x0	clk_lane_en Clock Lane enable for LVDS mode 1: enable Clock Lane 1: disable Clock Lane
2	RW	0x1	pll_powr_off PLL power off enable for LVDS mode 1: power off 0: power on
1:0	RO	0x0	reserved

13.5 Application Notes

13.5.1 COMMON CONFIGURATION (DEFAULT IN MIPI MODE)

Step1: Enable reference clock.
Step2: Wait a period after reference clock have been enabled.
Step3: Send 0xe4 to register MIPI_DSI_DPHY_CTRL_PWRCTL. Enable PLL and LDO.
Step4: Send 0x7d to register MIPI_DSI_DPHY_CTRL_LANE_ENABLE. Enable all lanes on analog part.
Step5: Send 0xe0 to register MIPI_DSI_DPHY_CTRL_PWRCTL. Reset analog.
Step6: Wait a period after analog has been reset.
Step7: Send 0x1e to register MIPI_DSI_DPHY_CTRL_DIG_RST. Reset digital.
Step8: Send 0x1f to register MIPI_DSI_DPHY_CTRL_DIG_RST. Reset digital.

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Step9: Wait a period until pll locked. Run in MIPI mode.

13.5.2 CONFIGURATION FOR LVDS MODE

Step1: Firstly perform common configuration.
Step2: Configure PLL.
Write 8'h01 to the register MIPI_DSI_DPHY_CTRL_PREDIV;
Write 8'h0e to the register MIPI_DSI_DPHY_CTRL_FBDIV;
Step3: (optional) Select lsb mode, default msb mode.
Write 8'h44 to the register DPHY_LVDS_TTL_SETTIING_ctrl;
Step4: Enable LVDS digital logic.
Write 8'h92 to the register DPHY_LVDS_TTL_SETTIING_digital_en;
Step5: Enable LVDS analog driver.
Write 8'h f8 to the register DPHY_LVDS_TTL_SETTIING_lane_en;
Step6: Select LVDS mode.
Write 8'h 02 to the register DPHY_LVDS_TTL_SETTIING_mode_en;
Step7: Wait a period until PLL locked. Run in LVDS mode.

13.5.3 CONFIGURATION FOR TTL MODE

Step1: Select TTL mode.
Write 8'h04 to the register DPHY_LVDS_TTL_SETTIING_mode_en;
Step2: Enable analog driver.
Write 8'hfd to the register DPHY_LVDS_TTL_SETTIING_lane_en;
Step3: Run in TTL mode.

13.5.4 LOW POWER MODE (FOR DSI ONLY)

Low Power Mode is a special feature for D-PHY. You can control this function by using proper registers from the D-PHY with few operations. The following is a step by step instruction for low power mode in and out.

- **Low Power in Steps:**

Step1: Send 0x01 to register MIPI_DSI_DPHY_CTRL_LANE_ENABLE. Disable all lanes on analog part.
Step2: Send 0xe3 to register MIPI_DSI_DPHY_CTRL_PWRCTL. Disable PLL and LDO.
Step3:Wait a period before reference clock have been disabled.
Step4: Disable reference clock.

- **Low Power out Steps:**

Step1: Enable reference clock.
Step2: Wait a period after reference clock have been enabled.
Step3: Send 0xe4 to register MIPI_DSI_DPHY_CTRL_PWRCTL. Enable PLL and LDO.
Step4: Send 0x7d to register MIPI_DSI_DPHY_CTRL_LANE_ENABLE. Enable all lanes on analog part.
Step5: Send 0xe0 to register MIPI_DSI_DPHY_CTRL_PWRCTL. Reset analog.
Step6:Wait a period after analog has been reset.
Step7: Send 0x1e to register MIPI_DSI_DPHY_CTRL_DIG_RST. Reset digital.
Step8: Send 0x1f to register MIPI_DSI_DPHY_CTRL_DIG_RST. Reset digital.

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Chapter 14 MIPI CSI D-PHY

14.1 Overview

The MIPI CSI D-PHY is compliant with the MIPI D-PHY interface specification, revision 1.0. The MIPI CSI D-PHY is used for slave applications. The MIPI CSI D-PHY is targeted for receive the camera video digital data in mobile applications, supporting a maximum effective bit rate of 1.0Gbps per lane. The assembled four-data-lane system enables up to 4Gbps aggregate communication throughputs, delivering the bandwidth needed for high-throughput data transfer.

The MIPI D-PHY supports the following features:

- Mixed-signal D-PHY mixed-signal hard-macro- HS/LS Transmitter and LS/HS Receiver solution
- Designed to MIPI® v1.0 Specifications
- Integrated PHY Protocol Interface (PPI) supports interface to CSI and UniPro™ MIPI® protocol
- 1.0GHz maximum data transfer rate per lane
- Expandable to support 4 data lanes, providing up to 4Gbps transfer rate
- 10Mbps per lane in low-power mode
- Unidirectional and bi-directional modes supported
- Automatic termination control for HS and LP modes
- Low-Power dissipation: less than 3mA/Lane in HS RX mode
- Rx Buffers with tunable On-Die-Termination and advanced equalization.
- Embedded ESD, boundary scan support logic.

14.2 Block Diagram

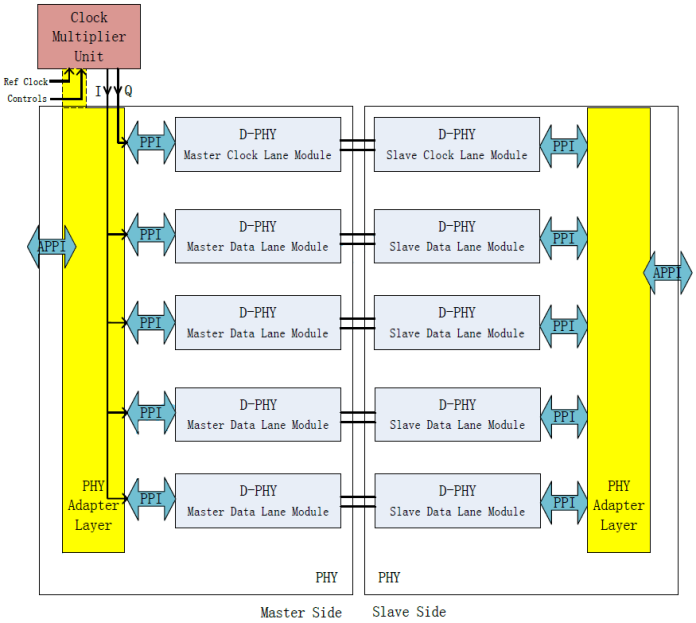


Fig. 14-1 MIPI CSI D-PHY detailed block diagram

MIPI CSI D-PHY configuration contains one Clock Lane Module and four Data Lane Modules. Each of these PHY Lane Modules communicates via two Lines to a complementary part at the other side of the Lane Interconnect.

14.3 Function Description

14.3.1 System Connection

MIPI CSI D-PHY registers are configured by software, but its input ports phy_forcerxmode, phy_datalane_en, phy_clklane_en are configured by grf register. D-PHY output video data feeds ISP. The connection shows in following figure:

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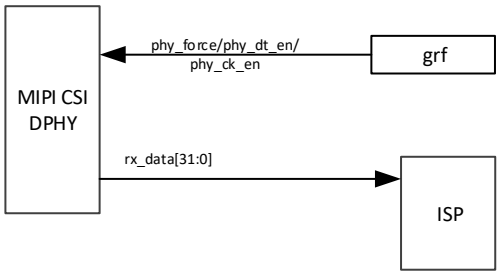


Fig. 14-2 MIPI CSI D-PHY and ISP connection

In MIPI mode, there are some functions of DPHY controlled by grf registers. These register bit and function is show in following table:

Table 14-1 function of grf bits in MIPI mode

register bit	function
grf_con_csiphy_clkinv_selection	Reverse for receive clock
grf_con_csiphy_clklane_en	Receiver Clock Active. This asynchronous, active high signal indicates that a Clock Lane is receiving a DDR clock signal.
grf_con_csiphy_datalane_en_3	Receiver Data Lane Active. This active low signal is asserted to indicate that the Lane is in ULP state.
grf_con_csiphy_datalane_en_2	Receiver Data Lane Active. This active low signal is asserted to indicate that the Lane is in ULP state.
grf_con_csiphy_datalane_en_1	Receiver Data Lane Active. This active low signal is asserted to indicate that the Lane is in ULP state.
grf_con_csiphy_datalane_en_0	Receiver Data Lane Active. This active low signal is asserted to indicate that the Lane is in ULP state.
grf_con_csiphy_forcerxmode_3	Force Lane Module Into Receive mode / Wait for Stop state. This signal allows the protocol to initialize a Lane Module, or force a bi-directional Lane Module, into receive mode.
grf_con_csiphy_forcerxmode_2	Force Lane Module Into Receive mode / Wait for Stop state. This signal allows the protocol to initialize a Lane Module, or force a bi-directional Lane Module, into receive mode.
grf_con_csiphy_forcerxmode_1	Force Lane Module Into Receive mode / Wait for Stop state. This signal allows the protocol to initialize a Lane Module, or force a bi-directional Lane Module, into receive mode.

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register bit	function
grf_con_csiphy_forcerxmode_0	Force Lane Module Into Receive mode / Wait for Stop state. This signal allows the protocol to initialize a Lane Module, or force a bi-directional Lane Module, into receive mode.

14.4 Register Description

This section describes the control/status registers of the design.

14.4.1 Register Summary

Name	Offset	Size	Reset Value	Description
MIPI_CSI_DPHY_CTRL_LANE_ENABLE	0x0000	W	0x00000001	lane enable
MIPI_CSI_DPHY_CTRL_PWRCTL	0x0004	W	0x00000003	power control
MIPI_CSI_DPHY_CTRL_DIG_RST	0x0080	W	0x000000ff	digital reset
MIPI_CSI_DPHY_CTRL_SIG_INV	0x0084	W	0x00000000	signal invert

*Notes: Size: **B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

Following table shows registers for 5 lanes. They have same registers but use different address bases. So their final address is lane_base_address + offset.

Table 14-2 registers address for 5 lanes table

lane	lane_base_address
clock_lane	0x100
Data0_lane	0x180
Data1_lane	0x200
Data2_lane	0x280
Data3_lane	0x300

Following table shows the registers for LANE configuration.

Table 14-3 registers configuration for 5 lanes table

Name	Offset	Size	Reset Value	Description
MIPI_CSI_DPHY_LANEX_THS_SETTLE	0x0000	W	0x0000000b	THS_SETTLE
MIPI_CSI_DPHY_LANEX_MSB_EN	0x0038	W	0x00000000	MSB_EN

*Notes: Size: **B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

14.4.2 Detail Register Description

MIPI_CSI_DPHY_CTRL_LANE_ENABLE

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:7	RO	0x0	reserved
6	RW	0x0	lane_en_ck lane clock enable
5	RW	0x0	lane_en_3 lane 3 enable

Bit	Attr	Reset Value	Description
4	RW	0x0	lane_en_2 lane 1 enable
3	RW	0x0	lane_en_1 lane 1 enable
2	RW	0x0	lane_en_0 lane 0 enable
1:0	RO	0x0	reserved

MIPI_CSI_DPHY_CTRL_PWRCTL

Address: Operational Base + offset (0x0004)

Bit	Attr	Reset Value	Description
31:3	RO	0x0	reserved
2	RW	0x0	SYNCRST reset phy
1	RW	0x1	LDO_PD ldo power down
0	RW	0x1	PLL_PD pll powerdown

MIPI_CSI_DPHY_CTRL_DIG_RST

Address: Operational Base + offset (0x0080)

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	dig_rst digtial logic reset

MIPI_CSI_DPHY_CTRL_SIG_INV

Address: Operational Base + offset (0x0084)

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3	RW	0x0	PIN_RXBYTECLKHS_INV_EN inverting pin_rxbyteclkhs enable
2:0	RO	0x0	reserved

MIPI_CSI_DPHY_LANEX_THS_SETTLE

Address: Operational Base + offset (0x0000)

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved

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Bit	Attr	Reset Value	Description
3:0	RW	0xb	Tlpx Configure the count time of the THS-SETTLE by protocol. After the count done, D-PHY will begin to receive the high speed data. (Can be configured from 4'h0 to 4'hd) 4'b0000 80-110 MHz 4'b0001 110-150 MHz 4'b0010 150-200 MHz 4'b0011 200-250 MHz 4'b0100 250-300 MHz 4'b0101 300-400 MHz 4'b0110 400-500 MHz 4'b0111 500-600 MHz 4'b1000 600-700 MHz 4'b1001 700-800 MHz 4'b1010 800-1000 MHz 4'b1011 additional adjust 4'b1100 additional adjust 4'b1101 additional adjust 4'b1110 additional adjust

MIPI_CSI_DPHY_LANEX_MSB_EN

Address: Operational Base + offset (0x0038)

Bit	Attr	Reset Value	Description
31:7	RO	0x0	reserved
6	RW	0x0	MSB_EN MSB enable for pin_rxdatahs_* 1: enable 0: disable
5:0	RO	0x0	reserved

14.5 Application Notes

14.5.1 LOW POWER MODE

Low Power Mode is a special feature for D-PHY. You can control this function by using proper registers from the D-PHY with few operations. The following is a step by step instruction for low power mode in and out.

- **Low Power in Steps:**

Step1: Send 0x01 to register MIPI_CSI_DPHY_CTRL_LANE_ENABLE. Disable all lanes on analog part.
Step2: Send 0xe3 to register MIPI_CSI_DPHY_CTRL_PWRCTL. Disable PLL and LDO.
Step3: Wait a period before reference clock have been disabled.
Step4: Disable reference clock.

- **Low Power out Steps:**

Step1: Enable reference clock.
Step2: Wait a period after reference clock have been enabled.
Step3: Send 0xe4 to register MIPI_CSI_DPHY_CTRL_PWRCTL. Enable PLL and LDO.
Step4: Send 0x7d to register MIPI_CSI_DPHY_CTRL_LANE_ENABLE. Enable all lanes on

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analog part.
Step5: Send 0xe0 to register MIPI_CSI_DPHY_CTRL_PWRCTL. Reset analog.
Step6: Wait a period after analog has been reset.
Step7: Send 0x1e to register MIPI_CSI_DPHY_CTRL_DIG_RST. Reset digital.
Step8: Send 0x1f to register MIPI_CSI_DPHY_CTRL_DIG_RST. Reset digital.
Step9: Wait a period before normal transmission.

14.5.2 COMMON CONFIGURATION (DEFAULT IN MIPI MODE)

Step1: Enable reference clock.
Step2: Wait a period after reference clock have been enabled.
Step3: Send 0xe4 to register MIPI_CSI_DPHY_CTRL_PWRCTL. Enable PLL and LDO.
Step4: Send 0x7d to register MIPI_CSI_DPHY_CTRL_LANE_ENABLE. Enable all lanes on analog part.
Step5: Send 0xe0 to register MIPI_CSI_DPHY_CTRL_PWRCTL. Reset analog.
Step6: Wait a period after analog has been reset.
Step7: Send 0x1e to register MIPI_CSI_DPHY_CTRL_DIG_RST. Reset digital.
Step8: Send 0x1f to register MIPI_CSI_DPHY_CTRL_DIG_RST. Reset digital.
Step9: Wait a period until pll locked. Run in MIPI mode.

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